APPLIED PHYSICS

CMOS-compatible electro-optical SRAM cavity device based on negative differential resistance

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The impending collapse of Moore-like growth of computational power has spurred the development of alternative computing architectures, such as optical or electro-optical computing. However, many of the current demonstrations in literature are not compatible with the dominant complementary metal-oxide semiconductor (CMOS) technology used in large-scale manufacturing today. Here, inspired by the famous Esaki diode demonstrating negative differential resistance (NDR), we show a fully CMOS-compatible electro-optical memory device, based on a new type of NDR diode. This new diode is based on a horizontal PN junction in silicon with a unique layout providing the NDR feature, and we show how it can easily be implemented into a photonic micro-ring resonator to enable a bistable device with a fully optical readout in the telecom regime. Our result is an important stepping stone on the way to new nonlinear electro-optic and neuromorphic computing structures based on this new NDR diode.

INTRODUCTION

Chasing the explosive growth of the demand for digital storage and processing constitutes one of the major challenges of modern computing. Our hunger for faster and larger data processing has been fed by the industry's capability to double the number of transistors in integrated circuits (ICs) every 2 years, known as Moore's law (*1*). Unfortunately, there are signs indicating that this era is coming to an end (*2*). One of the main obstacles in maintaining Moore-like growth is the density of electrical wires needed to connect the large number of transistors that exist in the processing core with their respective memory cells. These wires result in heat originated from ohmic losses and simultaneously carry undesired large capacitances, inducing a latency and energy cost. Hence, the limited connectivity is one of the reasons to the well-known "memory wall" problem. In the current design scheme of ICs, this problem is expected to be exacerbated by the growing number of processing cores (*3*–*5*).

It is therefore imperative to consider alternative technologies and processing architectures, such as optical memory and photonic computing (*6*–*8*). As the information in these architectures is carried by photons rather than by electrons, and since integrated photonic waveguides are nearly lossless, the problem of heating can be avoided. In particular, electro-optical memory units hold a great promise as an intermediary step toward a fully photonic computing solution. Electro-optical memory cells can be located far from a conventional processor and be accessed by optical signals through photonic bus interconnects, allowing minimal latency and high data throughput, fulfilling the continuous demands for speed and bandwidth growth (*9*).

Memory devices can be divided into two major categories coined as volatile and nonvolatile memory. Both have been demonstrated in the photonics domain using the emerging silicon photonics platforms (*10*–*24*). Electro-optical and optical nonvolatile memory devices that have the capability to hold and save data even without a continuous power supply were designed using different technologies, such as the integration of a phase-changing material (PCM), like germanium-antimony-tellurium (GST), on absorption-based devices. These devices present a large optical contrast, between the crystalline and the amorphous state of the embedded PCM (*10*–*14*). Likewise, the implementation of transparent conducting oxides presenting epsilon-near-zero effect in the telecommunication wavelength range can be used either as an electro-absorption switch (*15*) or modulator (*16*). Floating gate structure–based devices, using two-dimensional (2D) materials such as graphene, have also been shown. These devices exploit light propagation states that depend on the charge density trapped in a thin charge trapping layer (*17*, *18*, *25*). Nanoscale flash memory technologies relying on charge injection such as metal-oxide-nitride-oxide-silicon structures have also been integrated into an optical cavity resulting in a suitable nonvolatile optical memory device (*20*). Next to that, the most popular type of volatile memory device remains the RAM. This is due to the high speeds associated with accessing or changing the memory state of such memory cells. A considerable number of optical RAM and flip-flop devices have been developed. These are usually based on the combination of an optical amplifier with a Mach-Zehnder modulator or switch (*21*–*23*) or by the use of a microdisk laser demanding heterogeneous integration of materials like indium phosphide (*24*). Another approach is that of photonic memristors, offering a photonic readout of the change in the state of resistivity (*26*, *27*).

Nevertheless, most of the electro-optic and all-optical memory devices mentioned here suffer from the disadvantage of not being CMOS-compatible. CMOS, or complementary metal-oxide-semiconductor, is the standard fabrication process used today in the semiconductor industry. It is limited to a list of a few compatible materials, as some materials can cross-contaminate fabricated devices, reducing their performance. A CMOS-compatible process is robust and reliable, allowing the implementation of devices that can operate billions of times without being damaged. This is in contrast to PCM technology where the degradation is faster (*28*). Moreover, some optical memories rely on the nonlinear optical effect and thus require a substantialt optical power to operate. This requirement and the opportunity rooted in optical computing have led

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to the development of many CMOS-compatible optical devices such as modulators (*29*, *30*), detectors (*31*, *32*), filters (*33*), and switches (*34*), which are building blocks for future electro-optic computing. To optimize the electro-optical effects, it is beneficial to use an optical structure embedded with a PN junction where the light-plasma interaction can be maximized (*30*). Therefore, it is imperative to develop an optical memory fabricated by using CMOS-compatible materials and processes. Such a memory device could ease the integration of silicon photonics platforms with conventional computing architectures, which are all done in CMOS fabrication processes enabling cheap large-scale production.

Volatile memories rely on the generation of a physical system with two or more stable solutions (bistable) at a given time. One way to realize an electrical circuit with a bistable state is to use the negative resistance effect. The discovery of this effect is dated back to the seminal work of L. Esaki who originally demonstrated the negative differential resistance (NDR) effect using electrical diodes in 1958 (*35*). The NDR effect occurs when, counterintuitively, a decrease in electrical current is observed despite an increase of applied voltage over a junction. The phenomenon is most characteristically present in tunnel diodes, lambda diodes, and Gunn diodes (*36*–*38*). Besides memories, NDR can be used for applications such as oscillators, amplifiers (*39*, *40*), and switches. Lately, the rise of neuromorphic computing architectures (*41*) has also turned a large amount of attention to NDR devices, due to their ability to mimic biological neurons (*42*–*44*). SRAM (static RAM), based on the NDR effect, has been shown using various types of heterojunctions and 2D materials (*45*–*48*). In this work, we report the design and the experimental demonstration of a new type of negative resistance electro-optic memory device that we refer to as the NDR optical SRAM (NDR-OSRAM).

First, we have designed and experimentally demonstrated a new type of NDR diode optimized for later integration with photonic readout. We electrically characterize the device and show its NDR effect.

The new NDR diode is then integrated into an optical micro-ring resonator (MRR) such that the change in the electrical charge carrier density will have a maximal effect on the optical signal. We have measured the optical transmission of the device as we move from one state to the other and show a high optical extinction ratio. In addition, we have used the NDR diode to build the SRAM cell and demonstrate, write, and read operations. The NDR-OSRAM operates using a low-supply voltage of less than 2 V and is fabricated using the standard silicon on insulator (SOI) CMOS process, making it a useful building block for optical computation. The NDR-OSRAM's simple design can ease its integration in current communications and computation schemes and gives us the freedom to place memories far from the processors to enable new computation diagrams.

RESULTS

The NDR diode

Before discussing its optical properties, we first describe our NDR diode device as a two-terminal electronic device, as shown in Fig. 1A. The NDR diode is composed of a PN junction, with similar doping concentrations for the P and N layers. A specific section of the device has a region with higher acceptor concentration, P^+ (best viewed in Fig. 1D, bottom left), inducing a thinner N-type region near the top of the junction (Fig. 1D, upper left). As a result, the smallest distance between the depletion layer of the junction and the top of the device occurs near this region of the diode. In essence, our NDR operation concept resembles that of a junction field effect transistor (JFET) structure with two dedicated contacts for each P- and N-type layer of the vertical PN junction. These contacts force the two halves of the junction to be serially connected to the power supply, and each section of the diode, i.e., the N, P, and P^+ regions, behaves as a serially connected resistor, as shown in Fig. 1B.

A typical measured *I-V* (current-voltage relation) characteristic of our NDR diode is shown in Fig. 1C. From this measurement, we see that, initially, the current rises sublinearly with the increase in applied reverse bias, V_λ, until a critical point, $V_{\text{pinch off}}$ (point f in Fig. 1C), is reached. Beyond this point, the current starts to decrease with the increase in reverse bias, giving rise to an NDR region. This *I-V* curve resembles the bottom half of the Greek letter "λ," after which NDR devices are commonly referred to as lambda diodes. Additional measurements with different geometries are shown in the Supplementary Materials (fig. S3).

The NDR effect observed in our device is directly linked to an increase in resistance, occurring as a result of the thinning of the conductive layers in the junction. At zero-applied voltage (Fig. 1D), uniform depletion layers are formed horizontally along the junction, except for at the left side where the depletion layers are wider in the N-type layer and thinner at the P^+ layer because of the higher doping concentration there. Upon the application of voltage, V_λ, the depletion layers expand, however, due to the lower hole mobility, and since the same lateral current is flowing in all layers, the lateral electric field is larger in the P-type layer. The result is that the vertical voltage drop across the junction is getting smaller as one moves to the right side of the device. The resulting depletion layers can be seen in Fig. 1E. Further increase of the voltage causes the depletion layer region in the left side of the N part of the junction to reach the top of the silicon surface. This forms a pinch-off condition (similar in concept to the pinch off obtained in a MOS transistor); see Fig. 1F. In the pinch-off region, there are almost no free electrons; thus, its resistance becomes much higher than the other regions of the device. The result is that any further increase of the applied voltage will be dropped mostly on the narrow pinch-off region, with the result of a serial resistance increase overall for the device. Since there is almost no increase of the lateral electric field in the layers, and, at the same time, the resistance increases due to the widening of the depletion layers, as shown in Fig. 1G, the current through the device becomes lower. The end result is that at voltages $V_\lambda > V_{\text{pinch off}}$, the device exhibits negative resistance as evident by observing the shaded zone in Fig. 1C.

By combining the NDR device with a serial load resistor, one should expect a bistable nature for the circuit. Bistable circuits have previously been used for memory applications, such as those implemented in a standard flip-flop circuit. Basically, a memory cell with one NDR diode, one select transistor, and one load resistor, which is realized in a separate layer on top of the NDR diode, will result in an SRAM. From an electrical perspective, this SRAM would be a factor of ~2 smaller than the standard six-transistor cell seen in conventional devices. A schematic diagram of the two configurations is shown in the Supplementary Materials (section SV).

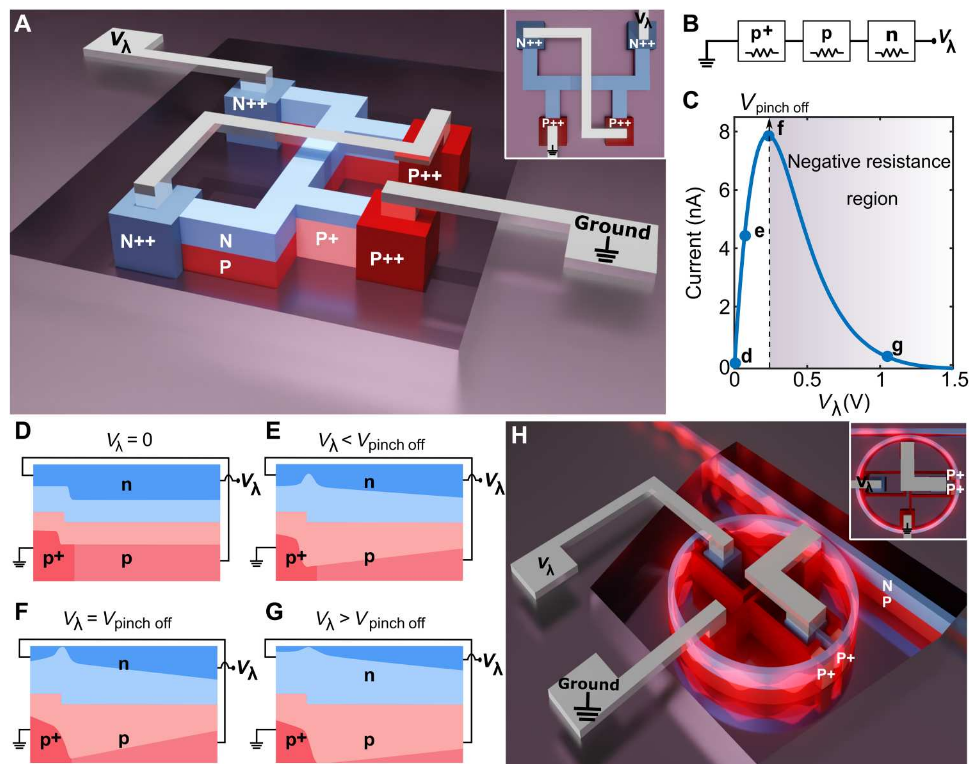

Fig. 1. Overview of the optical memory device, working principle, and characteristic of the NDR diode. (**A**) Schematic of the NDR diode showing the electrical connectivity with two wires to the ground and the voltage source. Also shown is the internal electrical wire connecting the p-type section on one side to the n-type section on the other side of the device. (**B**) Equivalent electrical circuit NDR diode. (**C**) Typical *I-V* (current-voltage relation) characteristics measured in our NDR diode. (**D** to **G**) Schematic illustrations of the varying depletion zones of the NDR diode under different V_λ biases applied on it. (**H**) Schematics of the optical memory device corresponding to the NDR diode junction integrated into an MRR electrically connected with two wires to electrodes. By applying a bias between these two electrodes, the optical resonance of the micro-ring is controlled, leading to bistable resonant states within the optical resonator.

Optical-SRAM

Motivated by the potential advantage of the NDR configuration for electronic SRAM applications, and considering the need for advanced optical memory devices, we move and integrated our NDR diode into a photonic structure to construct an NDR-OSRAM device. This has been achieved by realizing a silicon MRR in which we have embedded two NDR diodes, each of which occupies half of the micro-ring's circumference. The two diodes are electrically connected, sharing the same contacts as conceptually presented in Fig. 1H. Further details on the design of the optical memory device and the implementation of the NDR diodes are given in Materials and Methods.

The MRR is coupled to a single bus waveguide that feeds light into the resonator. The light is coupled into and out of the system by using dedicated grating couplers localized in both ends of the waveguide. By applying a voltage on the NDR diodes embedded into the MRR, the refractive index and correspondingly the resonant wavelength of the ring resonator can be modulated via the free-carrier dispersion effect. We measured the transmission of the optical mode into the micro-ring–coupled waveguide, with no bias and with the application of a 3-V reverse bias. The shift of the resonance frequency, under applied bias, is clearly observed in Fig. 2A. The measured wavelength shift as a function of the applied reverse bias is shown in Fig. 2B; the maximum resonant wavelength shift appears to be ~20 pm. The magnitude of the shift is related to the doping concentration of the junction. From Fig. 2B, we see that maximum carrier depletion is reached around 3 V, as the resonance of the micro-ring does not shift noticeably for higher voltages (section SIII). We now define two states for the MRR: (i) when no bias is applied on the device ('0' state) and (ii) when 3 V is applied at maximum resonance shift ('1' state). The optical transmission of the MRR as a function of wavelength has been measured for these two states (Fig. 2A). Consequently, our device's wavelength working point can be determined as the maximal optical transmission difference between the states of the optical cavity, i.e., at 0 and 3 V, which occurs at the slope of the resonance region of the transmission curve. At this wavelength, the largest hysteresis is expected to be obtained. Our wavelength working point is thus chosen to be λ = 1563.645 nm, corresponding to a change in the optical transmission of $\Delta T \sim -2.3$ dB, as shown in Fig. 2C.

Next, we characterize our NDR-OSRAM as a bistable device. To do so, a load resistor of 1 gigohm is connected to the device in series. In Fig. 2D, we plot the measured electrical *I-V* curve of the NDR-OSRAM device, when there is no light coupled into the MRR, alongside with the *I-V* load line resistance for several external biases (V_D) applied on the circuit. In the inset, a zoom of the plot is shown for a voltage range of V_λ = 0 V to V_λ = 1.5 V. It is quite clear, from Fig. 2D, that, for a wide range of applied voltage values, V_D, the circuit has more than one stable state (evident as the

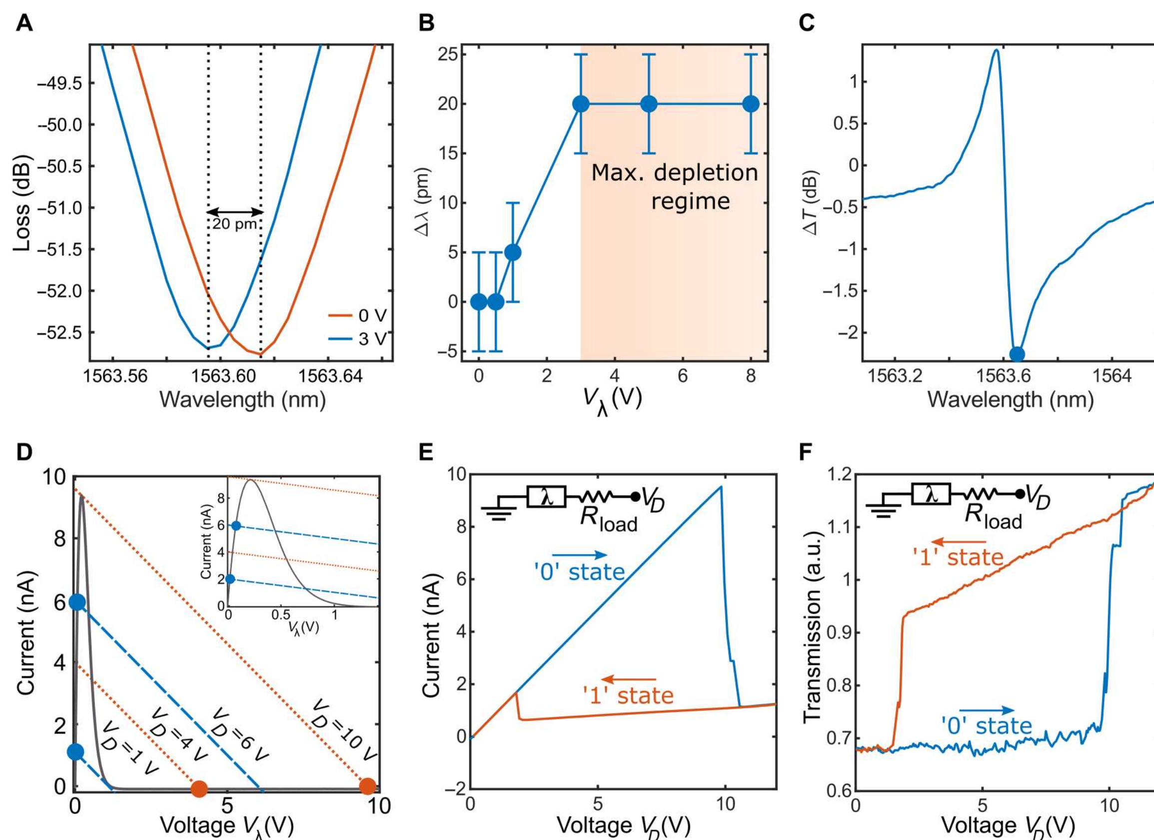

Fig. 2. Optical and electrical hysteresis behavior. (**A**) Optical transmission loss measurement at 0 V (red line) and 3 V (blue line). (**B**) Optical cavity resonance shift with respect to the applied bias on the device; the maximum resonance shift is reached around 3 V. The error bar corresponds to the experimentally determined error of the wavelength of the laser. (**C**) Working point identification by optical transmission loss measurement difference at 0 and 3 V as a function of the wavelength. (**D**) The optical cavity device's *I-V* curve and load line *I-V*s for applied bias on the circuit (V_D) of 1, 4, 6, and 10 V, respectively. The inset shows a zoom of the *I-V* curves. (**E** and **F**) Electrical and optical hysteresis. Current and optical transmission of the device as a function of the increasing (blue) and decreasing (red) bias applied. In the inset, a schematic of the corresponding electrical circuit is shown; the NDR-OSRAM device is represented by the Greek letter "λ."

intersection points between the device's *I-V* curve and the load line), leading to a bistability effect. From the optical point of view, the two stable states correspond to two distinct levels of optical transmission of the NDR-OSRAM cavity. These two levels of optical transmission occur due to the shift in resonance wavelength of the MRR, which, in turn, is the result of the change in free carrier concentration of the NDR diodes embedded in the micro-ring, as described above. In principle, we expected to observe another, third stable working point. However, we did not observe this point experimentally. We believe that this third point is probably less stable than the other two.

To capture the hysteresis curves, we have performed a bias sweep, V_D, back and forth, on the circuit shown in the insets of Fig. 2E (electrical signal) and Fig. 2F (optical signal). We first applied a low voltage on the circuit, ranging from V_D = 0 V to V_D = 1 V, for which only one stable state exists. Next, we gradually increased the applied voltage, and now the load line intercepts the device's *I-V* curve at two points, corresponding to the two stable states for the circuit, the '0' state and the '1' state. However, during the sweep of the voltage V_D, from 0 to 10 V, the system is stabilized only at the states set on the left part of the *I-V* curve, i.e., the '0' state, corresponding to the blue dots in Fig. 2D. Following the increase of the voltage, a sharp rise in the device current is observable (Fig. 2E). Hence, most of the voltage drops on the load resistor, while the voltage drop on the OSRAM device increases only slightly. By keeping the increase of the applied voltage V_D, the load line rises above the device's *I-V* peak, and the stability of the system switches to its second stable state, the '1' state at a higher voltage around 10 V. The switch to the '1' state is clearly seen in Fig. 2 (E and F) through the abrupt change of the blue lines. We swept back the applied voltage, and the system stabilizes now at the '1' state localized on the "tail" of the *I-V* curve. The current corresponding to the second stable state of the system is low all along the downward part of the voltage sweep, orange dots and line in Fig. 2 (D and E). The second stable point is obtained around the tail of the *I-V* curve, where the current is very low. This second stable state corresponds to the third intersection between the *I-V* curve and the load line, as shown in Fig 2D, rather than the second intersection (for which V_λ~0.5 V). As a result, large hysteresis can be obtained.

The optical hysteresis curve is shown in Fig. 2F. During the increase of the voltage on the circuit, the system stabilizes on the '0' state. At this state, the bias that drops on the optical microresonator bias does not change substantially, and thus, low and fairly stable optical transmission is maintained. Nevertheless, the applied voltage is increased beyond the critical point and then begins to decrease; the system stabilizes on the '1' state, corresponding to a

higher voltage drop on the MRR. During the course of voltage decrease, the diode is mainly depleted, and the optical transmission remains high.

The optical SRAM cell

Finally, we aim to use the bistable optical MRR device as an OSRAM cell. To demonstrate this functionality, we have connected a bit line between the load resistor and the NDR diode embedded in the MRR as depicted in Fig. 3A.

To test our device as a memory cell, a constant voltage V_D of 3 V is applied on the load resistor and the OSRAM device, such that two available stable states exist for this circuit (see section SIV). In addition, on the connected bit line, a writing voltage (V_w), varying from 0 to 2.5 V, is applied (Fig. 3B). This serves to bring the device in proximity to one of the stable states. A switch, represented here by the voltage V_s, is connected to the bit line and allows us to control the writing of a bit to the memory. Every 7 s, a bias of 5 V is applied on the switch, closing the switch for 3 s and forcing the applied bias V_w to drop on the device. The whole memory electric circuit design is illustrated in Fig. 3A. Each time the switch is closed, the writing voltage V_w is applied on the device, forcing the current I_D to flow through the bit line instead of through the device, thus shifting the optical transmission of the MRR according to the imposed writing voltage (Fig. 3C). When the switch is open, the system is stabilized on one of the two states imposed by the NDR device. However, when the switch is closed, the NDR is not affecting the circuit, and therefore, the current is simply given by the voltage difference between V_D and V_w. This is why the current I_D and the voltage V_λ vary with V_w when the switch is closed, whereas in the case of a closed switch, the value of V_w is not affecting the system performance, as long as it is not switched between a value lower than 1 V ('0' state) and a value larger than 1 V ('1' state). Correspondingly, the OSRAM device, being a bistable system, will stabilize at either one of its two stable states. We define the bit '0' to be the low optical transmission state and the bit '1' to be the high optical transmission state of our optical logic system. The state at which the system stabilizes is directly dependent on the constraint voltage V_w. At low writing voltages from 0 V to around 1 V, the system stabilizes at its low optical transmission state, i.e., the '0' state, whereas for higher writing voltages beyond 1 V, it is stabilized on the high transmission state, i.e., the '1' state. Further measurements have been done to also demonstrate the switching from state '1' back to state '0'; see fig. S9. We have measured the time response of the device to be around 30 ms, currently limited by the additional serial resistance that also results in the low current operation (see fig. S8).

DISCUSSION

In summary, inspired by the functionality of the "Esaki diode," we have demonstrated a new chip-scale electro-optic device that is fabricated in the widely used standard CMOS process and is presenting an NDR characteristic that we refer to as the NDR diode. Exploiting the tremendous advantage that our NDR diode is directly compatible with silicon photonics integration, we proposed and experimentally demonstrate an OSRAM device by combining the NDR diode design into an MRR. After we demonstrated the presence of an optical and electrical bistable effect in our device, we tested the OSRAM device as a memory cell by connecting it to a load resistor and to a bit line. A very low power consumption of about~200 pW and a low operating bias of 1 V are needed to switch between the '0' and '1' state of the memory. Furthermore, our device offers the important advantage of very short access time as a result of using optical readout. Note that we have measured the device over the span of a few months without notable degradation.

The OSRAM presented here serves as a proof of concept validating the feasibility of our approach. Future work including the integration of only one NDR diode, and a more optimal choice of the junction doping, is needed to further optimize the device performance as a memory cell. It will also be imperative to investigate the integration of the NDR diode in other modulator and nanophotonic devices such as Mach-Zehnder modulators and study

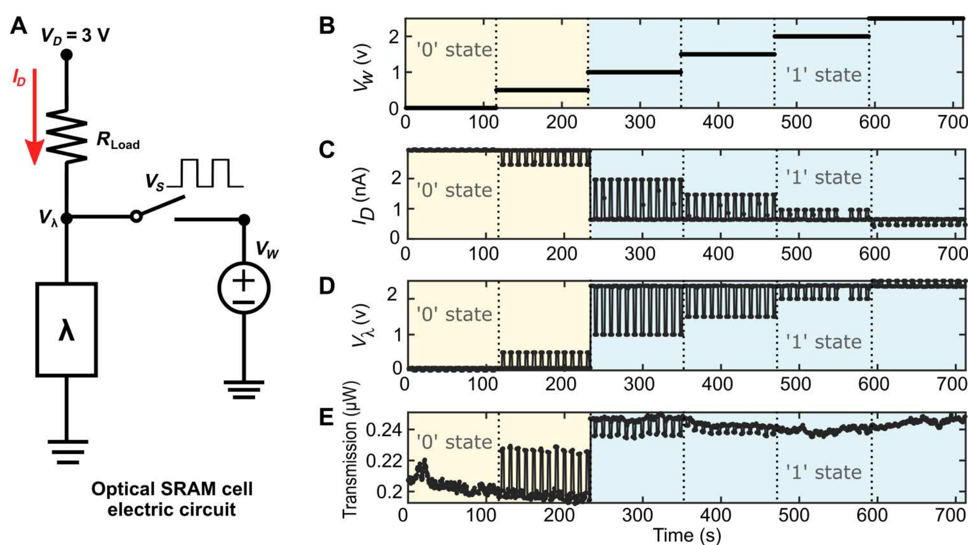

Fig. 3. Writing and reading of the optical SRAM. (**A**) Memory cell electric circuit illustration. For all the measurements presented here, the yellow and blue background corresponds to the '0' and '1' states of our logical system. (**B**) V_w is the applied writing voltage memory. (**C**) I_D is the current flowing through the optical memory device in the circuit. (**D**) V_λ is the voltage drop on the OSRAM device. (**E**) Optical transmission of the memory device.

potential applications in programmable neuromorphic computing architectures such as the photonic field programmable gate array (FPGA) processor and the quantum optical processor (*49*, *50*). The dimensions of the device can be further reduced by using other types of resonators, such as 1D photonic crystal, and perhaps even plasmonic resonators. Note, however, that because of the use of optical readout, extreme miniaturization is perhaps less critical, as the device can be located further away from the CPU, with optical communication being used to read and transfer the information.

Compared to electrical NDR implementations, our NDR device eliminates the need for optical to electrical to optical conversions and thus provides a substantial simplification of the system, reducing the usage of components such as photodetectors and lasers that are needed for such a conversion.

To conclude, the first CMOS-compatible "Esaki-like" NDR diode and its integration as an OSRAM has been demonstrated. We believe that our demonstrated concept holds a promise to revolutionize applications such as optical computing and communication, and it can be promoted as a great candidate for future electro-optic and neuromorphic computing systems.

MATERIALS AND METHODS

Device model

The device was fabricated by TowerJazz, on an SOI substrate of 220 nm. Two blanket implantations were performed on the entire silicon wafer, corresponding to the P and the N doping of the device. A third implantation of P^+ was performed using a mask. The different doping concentrations are 6×10^{17}, 3×10^{17}, and 3×10^{18} cm^{-3} for the N, the P, and the P+ side of the junction, respectively. We designed and fabricated first the only electrical structure of the NDR diode for different widths and lengths (see sections SI and SII), and then we design the mask to fabricate the electro-optical memory cell, corresponding to the NDR diode embedded in an MRR. The optical cavity was not designed as standard to maintain the confinement of the single optical mode that may be disturbed due to the integration of the NDR diode in it. The width of the waveguide ring changes all along its circumference, starting with a width of 450 nm, same as the width of the waveguide bus attached to the MRR, and gets wider, with a maximum width of about 1 μm at the azimuth of the MRR, and then the ring width was reduced back to its initial value of 450 nm. The radius of the MRR is 15 μm, and two electrical pads with a size of 80 × 80 μm connected to the OSRAM cavity were designed below the device.

Experimental setup

The optical setup is composed of collimated and linearly polarized light derived from a tunable laser source in the telecommunication wavelength. The laser beam was launched into dedicated grating couplers for the coupling of the light into the bus waveguide of the MRR using an optical fiber mounted on an XYZ stage. Our electrical setup is composed of two electrical mechanical tungsten probes connected to the signal measurement unit. Further details of the electro-optic setup are broadly described in our past work, cf. (*32*).

Supplementary Materials

This PDF file includes:
Figs. S1 to S9
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