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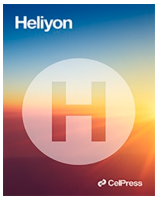

Research article

Pseudo random bit generator in QCA for high speed communications

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ABSTRACT

Quantum-dot cellular automata (QCA) technology is another new technology in the field of nanoelectronics and quantum. With the help of this technology, basic to advanced digital circuits can be designed and implemented with low energy consumption and small area. Therefore, in this paper, a new design for a four- and eight-bit Linear feedback shift register (LFSR) or random counter, as well as a rising-edge-sensitive D flip-flop with the least possible number of cells and the smallest area, was presented. This paper first designs the proposed D flip-flop with 24 cells and an area of 0.01 μm^2, so that with the help of this flip-flop it can design four and eight-bit LFSR. This flip-flop is one of the most optimal and suitable designs in terms of area and number of cells. Then, in the second step, a four-bit LFSR with 144 cells and an area of 0.2 μm^2 was designed with the help of the proposed flip-flop in the most optimal possible state. Also, in the third step, an eight-bit LFSR with 281 cells and an area of 0.4 μm^2 has been implemented for the first time in QCA technology, which is among the best possible designs. All the designs and simulations of this article were done in QCADesigner version 2.0.3 software and with QCAPro software, the energy consumption of the proposed circuits.

1. Introduction

In 1965, Moore was able to propose a silicon semiconductor technology's roadmap. This scientist realized that the number of transistors in small comparisons in integrated circuits is increasing. In fact, this is a law in the semiconductor industry known as Moore's Law. This rule is used not only in the manufacture of semiconductors, but also in counters, shift registers, memories, and other important parts of processors. After the creation of FET and MOSFET transistors, newer and more practical technologies were designed and invented in the world, including VLSI and nanoelectronics. After several years, nanoelectronics technology has become very famous in the world. Because this technology provides many applications in the field of clothing, electrical appliances, household, etc. Currently, the size of integrated and VLSI circuits has been reduced to 0.18 to 0.05 μm, and henceforth further miniaturization of transistors and circuits will not be possible due to limitations such as power consumption, welding of connections, etc. in quantum physics and electronics. For this reason, to have better performance of microprocessors, we should think about newer technologies in nano sizes. In the past few years, scientists have replaced CMOS and VLSI technology with a new technology called QCA [1–4].

QCA technology is a new technology in the field of integrated circuits and information technology, which is based on using the quantum properties of quantum dots to create logical structures and process information. In this technology, quantum dots are used as

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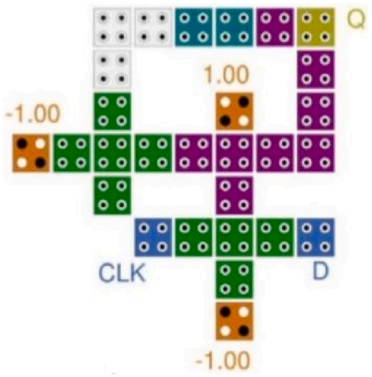

Fig. 1. D-type Latch structure in [10].

information bits, and information transfer is done using quantum effects such as connecting two quantum dots together. The advantages of QCA technology include high speed, low power consumption, small dimensions, and resistance to temperature changes and high temperatures. Due to its quantum features, this technology can be effective in designing high frequency circuits and data processing applications [5]. This technology consists of square shaped quantum cells. These cells are 18×18 nm in size and there are four holes inside these cells, when these cells are charged, the electrons inside are placed diagonally. These electrons inside the cell can never be placed next to each other. Because there is a repulsive force between electrons and holes, and for this reason, electrons are spaced apart. According to the placement of electrons in each of these cells, a polarity (1, 1+) is shown. In QCA technology, information transfer is done by the movement of electrons with a certain current. In fact, the cells should be placed in different clocks. Clocking in QCA is done in several steps. The clocking steps are switch, hold, release, relax. The circuit design rules in QCA technology say that clocking must be implemented on at least two cells, otherwise the design is flawed and does not deliver a stable output.

QCA circuits use the positions of electrons in quantum cells to represent binary information. This unique calculation method causes a significant reduction in energy consumption and the possibility of achieving higher operating frequencies. Also, QCA, with its miniaturization capability beyond the limitations of conventional transistors, is proposed as a suitable alternative for future nanoscale electronic systems. QCA technology, despite its impressive advantages, also has several challenges that have hindered its widespread adoption compared to traditional technologies such as CMOS. Some of these challenges are: stability and thermal noise, fabrication and manufacturing, clocking implementation, compatibility with existing technologies, simulation and design tools.

These challenges indicate that although QCA is considered a promising technology, it still requires further research and development of new technologies to overcome these obstacles. Also, QCA technology has certain advantages compared to memristors that can create superiority in certain applications: higher speed, lower power consumption and scalability. Also, in QCA technology, thermal management is complicated due to very low power consumption and high sensitivity to temperature changes. If the temperature goes out of a certain range, the performance of the QCA cells will be disrupted. On the other hand, circuit integration is also difficult due to the need for precise alignment of cells and the complexity in generating and controlling clock signals. These problems make it challenging to implement large and complex circuits in QCA. Also, the maintenance of QCA technology is challenging due to its sensitivity to environmental conditions such as temperature and electric and magnetic fields, and requires careful monitoring and the use of advanced materials and techniques to maintain stability. You can refer to Refs. [6–8] for further study.

Considering the importance of some digital circuits, researchers and scientists are looking for new and cost-effective designs to build these circuits in QCA technology. Circuits such as latches, flip-flops, counters, and larger circuits can be produced with this new technology. The production of electronic and digital circuits in this technology makes them have very high-power consumption, occupied area and also high speed. As a result, in this paper, for the first time, a new design of simple D flip-flop and random counter or LFSR circuits with the least number of cells and small area will be presented. A D flip-flop is a sequential circuit that acts as a single-bit memory. This flip-flop stores the input data on the rising (or falling) edge of the clock signal and displays its value at the output. The main feature of the D flip-flop is that its input is directly transferred to the output, provided that the clock signal is active. This flip-flop is used in digital circuits for storage, counters and registers. An LFSR, or linear feedback shift register, is a sequential circuit that shifts a string of bits based on a linear feedback function. This circuit is widely used in generating pseudo-random numbers, cryptography, testing digital circuits and generating unique sequences. In an LFSR, bits are shifted serially and new bits are generated by combining some of the previous bits. This method is used in many digital systems due to its simplicity and high efficiency.

The innovations of this article are.

- Presenting a new design of the rising edge sensitive D flip-flop with the least possible number of cells.
- New and precise design of four and eight-bit LFSR with very small area.

This article is divided into several sections. In the first part, it deals with past works on flip-flops and random counters. The second part presents the proposed designs. The third part is devoted to the results of the simulations to have a very good view of the random counter and flip-flops. Also, in the last part, the conclusion, and the suggestion to continue the work were discussed so that the readers

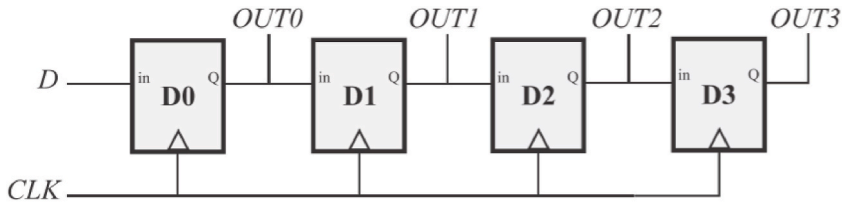

Fig. 2. Block diagram of 4-bit serial shift register

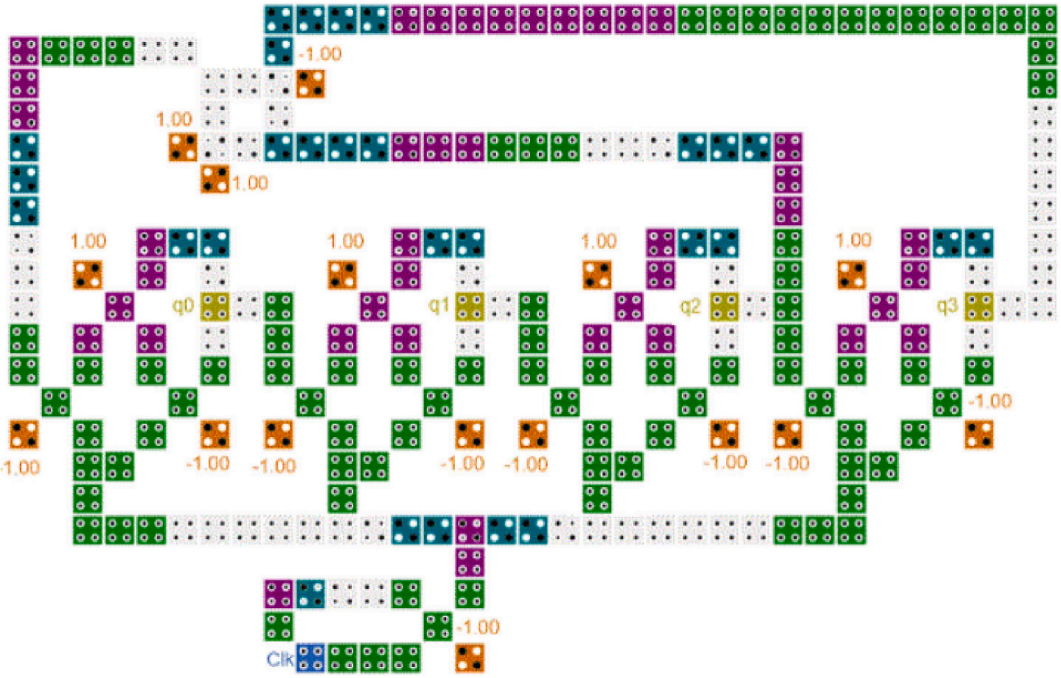

Fig. 3. four-bit LFSR in [19].

of this article in the future can provide innovations for themselves by using the proposed plans.

2. Related work

Latches and flip-flops are circuits that, if information is placed in their input, store that information in themselves. In latches, when the clock is 1, the data input value is directly transferred to the output, and if the clock becomes zero, the latch keeps its previous output value until the clock is 1. But the rising edge sensitive D flip-flop works by changing the clock level. That is, when the rising edge of the clock is seen, the data input is transferred to the output until the next edge of the clock. Now, if the data input is 1 during the rising edge, the output will be 1, and if the input is 0, the output will keep the value of 0 until the next edge of the clock. Several articles designed simple D latch, D latch with set and reset as well as flip-flops [9–14]. In 2012, Hashemi and his colleagues have been able to design a simple D latch with 48 cells, an area of 0.05 μm^2 and a delay of 1 Clock cycle [12]. With this design, the size of the D latch circuit as well as its price increases greatly. As a result, it is not economical to make and use. A few years later, in 2020, Alamdar designed a D latch with 28 cells, an area of 0.03 μm^2, and a delay of 0.5 Clock cycle for PFD design [10]. Fig. 1 shows Alamdar's design well. In 2014, a rising edge D flip-flop with 84 cells, an area of 0.11 μm^2 and a delay of 2.5 Clock cycles was designed by Dutta [15]. The disadvantages of this design are the many cells and the high delay. It can be said that this design is not cost-effective for construction in terms of many cells and large areas and it involves a lot of cost. In 2018, Gholami and his colleagues have been able to design the rising edge sensitive D flip-flop with 53 cells, an area of 0.04 μm^2 and a delay of 2.25 Clock cycles with the ability to set and reset [11]. This design also has the same problem of long-time delay and extra cell, which cannot be used for construction in the future.

In 2022, Amirzadeh and his colleagues designed D flip-flops with 34 and 37 cells, an area of 0.03 μm^2 and a delay of 1 Clock cycle, respectively simple D flip-flop and D flip-flop with reset [16].

Series shift registers can be very useful in making random and synchronous counters. According to the block diagram in Fig. 2, which shows a 4-bit shift register, we can present the idea of making a random counter that is almost like this block diagram. A random

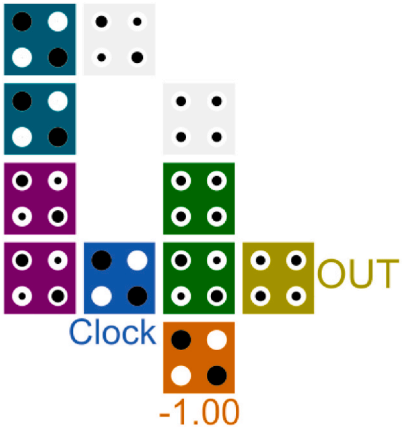

Fig. 4. Proposed rising edge converter in QCA technology

counter or LFSR is a type of digital counter that is used to generate random patterns or to be used in many other applications such as encryption, frequency generation, and channel error correction in digital communications.

Now, according to the basic explanations about the random counter, we will review some references together. To have a good view of the proposed designs. In fact, with these comparisons, researchers can provide more interesting designs more easily and better. Because part of the design work is related to past works. Articles [17–20] presented designs about 4-bit LFSR. But it is less common to design an 8-bit random counter in QCA. In 2014, reference [17] presented a four-bits LFSR, which design has 290 cells and an area of 0.46 μm^2. This design used a D latch to build a random counter, which we know is easier to build a counter with a latch, and we may not have accurate and stable output. And it may also be related to the initial conditions of the circuit. Therefore, in the construction of a random counter, it is tried to use the rising edge sensitive D flip-flop in order to have a more regular and accurate output. Also, in 2015, reference [18] was able to design a four-bits LFSR with 253 cells and an area of 0.41 μm^2. In this design, he used a latch to make a random counter. Disadvantages of this design, like the reference design [17], are many number of cells and a large area. As Fig. 3 shows, in 2019, Amirzadeh and his colleagues have been able to design a four-bits LFSR with 226 cells and an area of 0.3 μm^2. that this design used the rising edge sensitive D flip-flop [19]. The disadvantages of this design are many number of cells and a large area. It can be said that these designs are not suitable for construction and are not affordable. Also, in the same year, Gholamnia was able to design a four-bit LFSR with 157 cells and an area of 0.3 μm^2. In this design, an edge-sensitive D flip-flop is used, and its disadvantages are the large area and many number of cells [20]. From these comparisons and reviews, we can have a better view of the proposed designs, and researchers and readers of this article can use these comparisons and make much better designs for themselves. This article has presented the same comparisons in a table in the results and simulation section so that we can know about past designs more easily and with a better view.

3. Presentation of proposed plans

In this part, we want to present the rising edge sensitive D flip-flop, which has the smallest possible cell and area. This flip-flop is widely used in making a random counter. In the rest of this section, the design of four and eight bits LFSRs is discussed.

3.1. Proposed optimized D-flip-flop

Flip flops can be made using latches in two ways. In the first method, with two D latches and a not gate, these two latches are placed consecutively behind each other, and the first latch is called the master, and the second latch is the slave. With the change in input, the output is separated from it, and the first latch plays a fundamental role in changing the output. The second method is such that with one D-latch and an edge converter, a D flip-flop can be generated. The output is only activated upon seeing the active edge of the input clock and remains unchanged until the next clock edge.

As shown in Fig. 4, a rising-edge sensitive converter consisting of 11 cells with an area of 0.007 μm^2 is used for our related design. In this converter, the initial clock value is majority gated with the non-active state of the previous clock, and then the rising-edge sensitive output is generated. The output of this converter remains in the zero-time region, and depending on the clocking regions of the latch, after connecting this converter to a D-latch, a rising-edge sensitive D flip-flop can be designed. This converter exhibits superiority in terms of dimensions, cell count, and stability compared to the converters presented in Refs. [12,15]. Equation (1) represents the performance of this converter.

$$OUT = Clock(t) \times \overline{Clock(t-1)} \tag{1}$$

As Fig. 5 shows, the proposed D flip-flop has two general parts, in the first part, the proposed rising edge sensitive converter is located, and in the second part, there is a proposed D latch. If we want to explain in more detail, this proposed flip-flop has two majority

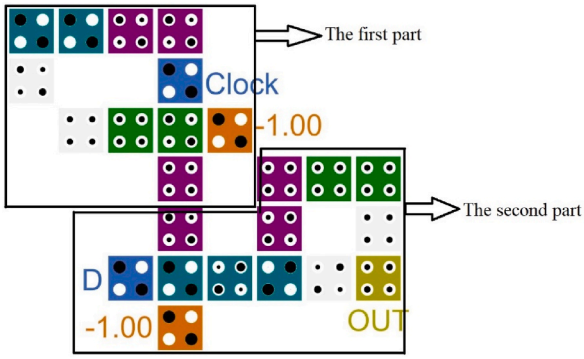

Fig. 5. Proposed optimized simple D-flip-flops with a raised edge

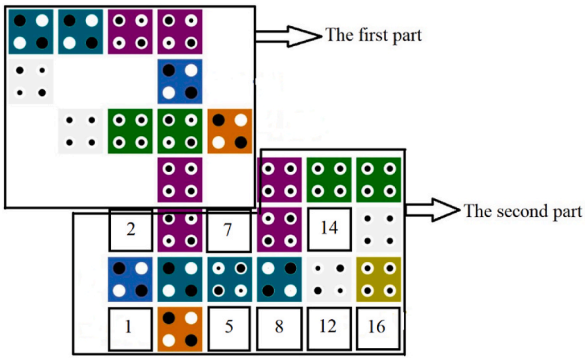

Fig. 6. Fault analysis for D-flip-flops

Table 1
Fault calculation for D-flip-flops.

Cell	Output(actual = 00111000010)	Fault
1	00111111111	5
2	00111000000	1
3	00000000000	4
4	00111000010	0
5	00000000000	4
6	00000000000	4
7	00100000011	3
8	00000000000	4
9	00011111101	6
10	00011011000	4
11	00111000010	0
12	00100000010	2
13	00111000010	0
14	00111011010	2
15	00111000010	0
16	00101010010	2
17	00111000010	0
18	00100000010	2

gates, one for transferring the clock to the output and another one for transferring the data input D. The proposed edge-sensitive D flip-flop has 24 cells and an area of 0.01 μm^2. It can be said that the booklet is considered the best design for engineers and researchers. According to Fig. 5, the function of the proposed rising edge sensitive D flip-flop is that when the clock is 1, that is, when the clock goes from 0 to 1, if the data value is 1, the output will be 1 until the next high edge of the clock, and if data is 0, the output will be 0 until the upper edge of the next clock. We designed this flip-flop in such a way that when the bases are set and reset, the area of the structure does not change and is easy to understand. This is an important advantage for design.

Now, to check the stability of the circuit, according to Fig. 5, the proposed design is separated into two parts so that the fault analysis can be done for the second part, the proposed D-latch. According to Fig. 6, fault analysis is done by adding and removing cells.

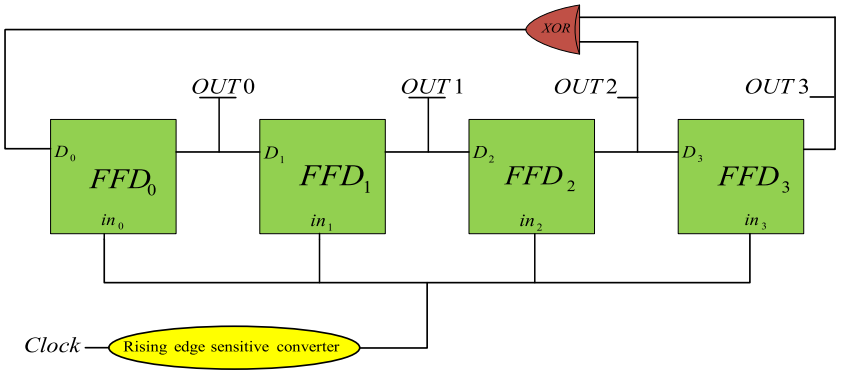

Fig. 7. Block diagram of the proposed four-bit LFSR

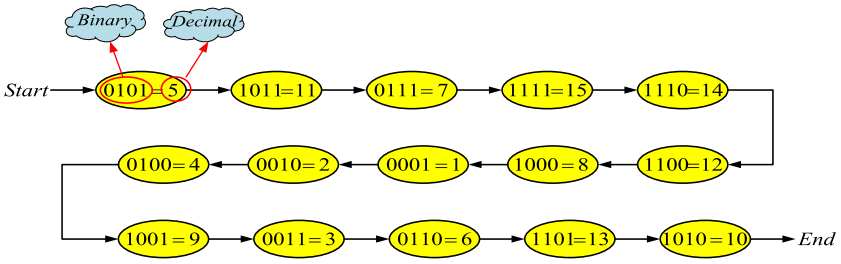

Fig. 8. State diagram of four-bits LFSR

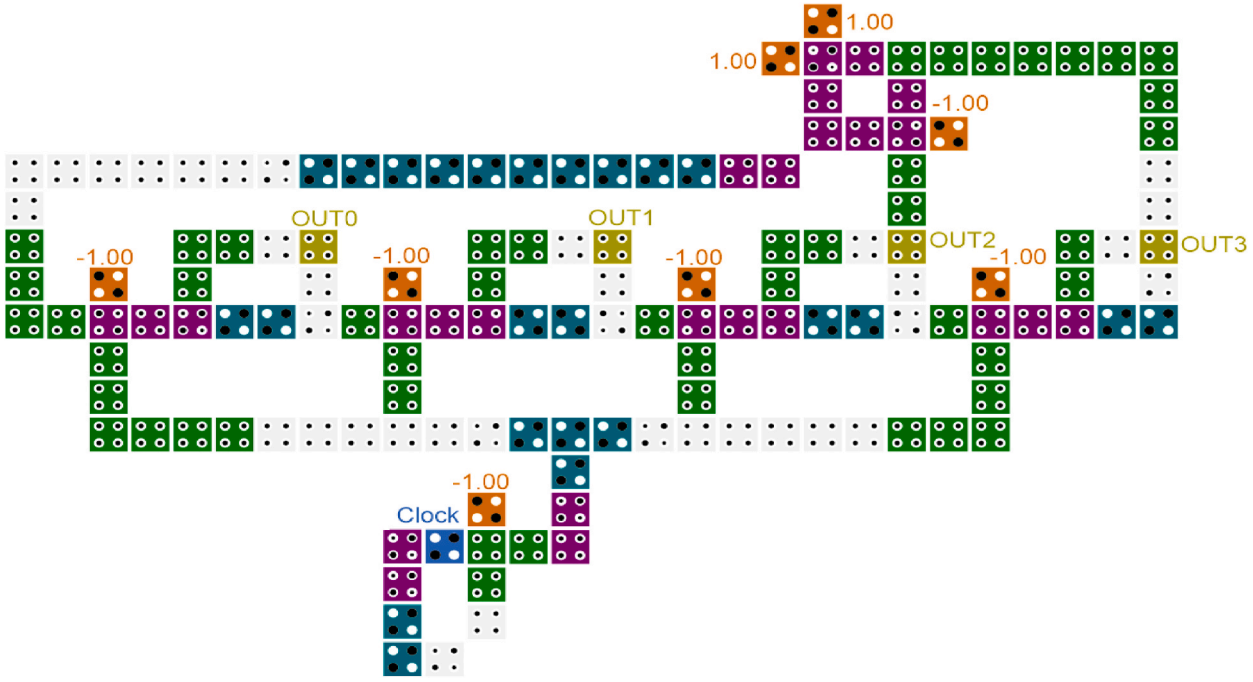

Fig. 9. The proposed four-bit LFSR

We are careful that the input and output cells do not play a role in adding or removing cells. As a result, the lost cells are: 3, 4, 6, 9, 10, 11, 13, 15, 17, 18. And the added cells are: 1, 2, 5, 7, 8, 12, 14, 16. The actual output of D-latch is 00111000010. To check the error by removing and adding each cell, their output is compared with the actual output. Table 1 presents the faults due to a single cell missing and addition defects. Table 1 shows that the total faults are 43 out of 198 bits. Therefore, this proposed basic design has 79 % stability

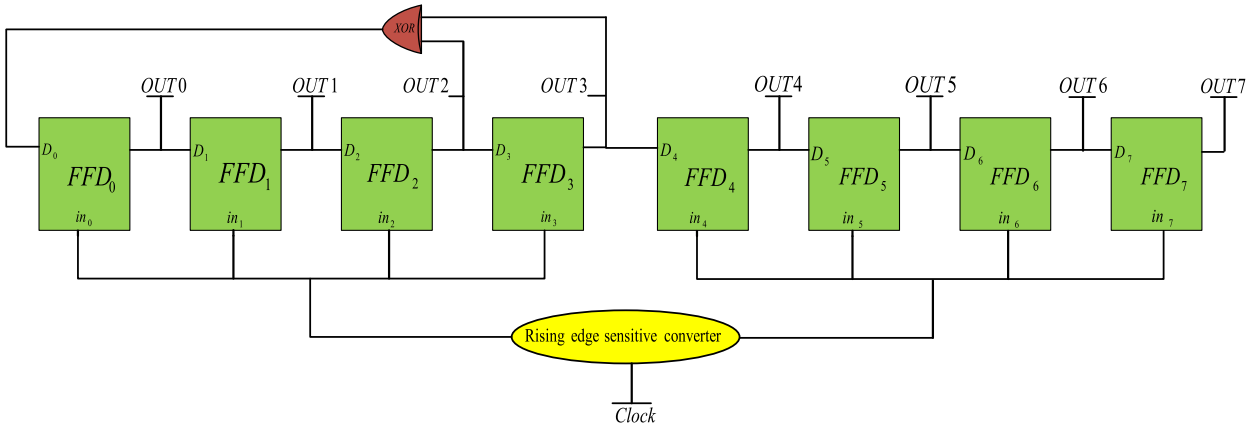

Fig. 10. Block diagram of the proposed eight-bit LFSR

and 21 % Fault.

3.2. Proposed optimized four-bits LFSR

LFSRs are tools that are used in many different applications, including military industries, generating random extensions, etc. These counters consist of serial structures of micro-addressable flip-flops that are combined with a linear feedback function. The main features and applications of LFSR are:

Simple structure: LFSR consists of simple flip-flops and XOR or AND operators, which have a simple structure and have significant advantages in terms of implementation.

Generation of random patterns: One of the main applications of LFSR is in the generation of random patterns. By using initial random values also known as seed and feedback function, LFSR can generate random patterns of arbitrary length.

Generating fundamental frequencies: LFSR can be used to generate fundamental frequencies in digital systems and signaling circuits.

Fig. 7 shows the block diagram of a four-bit LFSR. In this section, we will first present a newly designed four-bit LFSR using four D flip-flops and an XOR gate as well as a rising edge-sensitive converter according to the same block diagram.

In this block diagram, the outputs of the second and third flip-flops are applied together to the XOR inputs, and then the output of the XOR gate is transferred to the data input of the first floor. By doing this, random numbers are generated accurately and consecutively. Fig. 8 shows the state diagram of the numbers generated by the four-bits LFSR.

According to Fig. 7, we were able to provide a four-bit LFSR with an optimal and suitable design using the block diagram described. The proposed four-bits LFSR has 144 cells and an area of 0.2 μm^2. As Fig. 9 shows. The operation of the proposed four-bits LFSR is that in order to generate a number, first an initial value, which is the input clock, must be applied to the circuit, and then the output of the first flip-flop is generated and transferred to the next outputs. The outputs of the LFSR are continued and repeated as the output of a shift register. And the numbers are randomly entered into the repetitive counting cycle. Therefore, in this way, a four-bit LFSR is created and shows us four bits in the output. Although the proposed random counter is four-bits, it is more optimal and suitable compared to the other 3-bits random counters designed in terms of the number of cells and area. Note that this LFSR counts from 0 to 15, randomly. Also, in the results and simulation section, we will see that the designed design has very high accuracy and a good output.

3.3. Proposed optimized eight-bits LFSR

The eight-bits LFSR is a type of random counter with linear feedback, which consists of eight flip-flops and is used to generate random patterns and other applications. This type of LFSR is popular and common due to its simple structure and easy implementation in circuits and software, including random counters. Below are some of the applications of this type of LFSR:

Cryptography: One of the main uses of this structure is in cryptography. These counters are used to generate cryptographic keys, which are used as dynamic keys in cryptographic algorithms such as A5/1 (used in mobile networks).

Generating clock signals: Eight-bits LFSR can be used to generate clock signals in digital circuits and FPGA (Field Programmable Gate Array). These clock signals are used to synchronize and activate various operations in digital circuits.

Signal processing: In some applications, such as signal processing, random patterns may be used to generate random noise or generate patterns of random jumps. It can also be used for this purpose.

Random Tests: May be used to create random patterns for random tests in software engineering and unit tests.

Random number generation: In some applications such as computer networks and security related matters, there is a need to generate random numbers to randomly select and create key strings, and eight-bit LFSR can be used for this purpose. According to

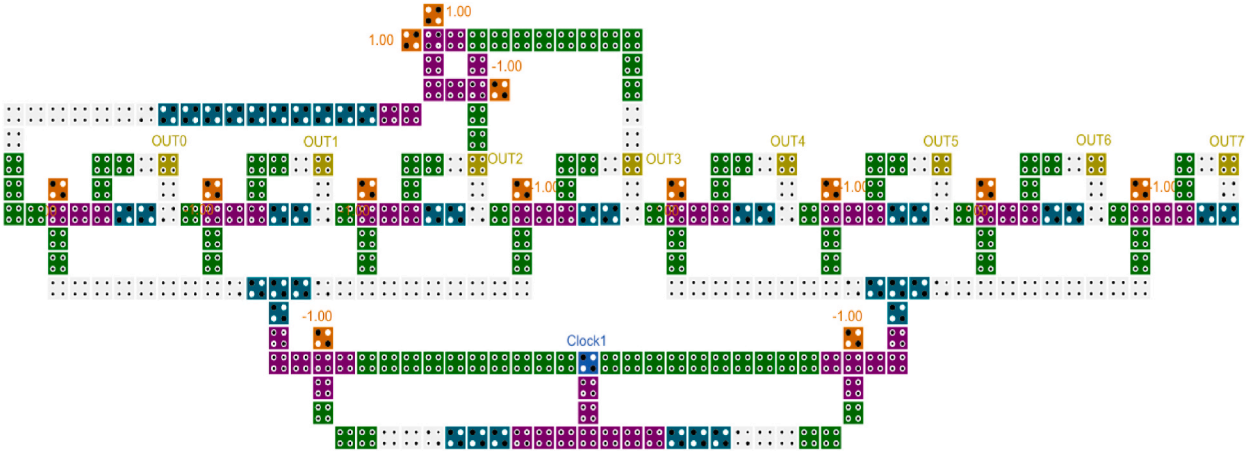

Fig. 11. The proposed eight-bit LFSR

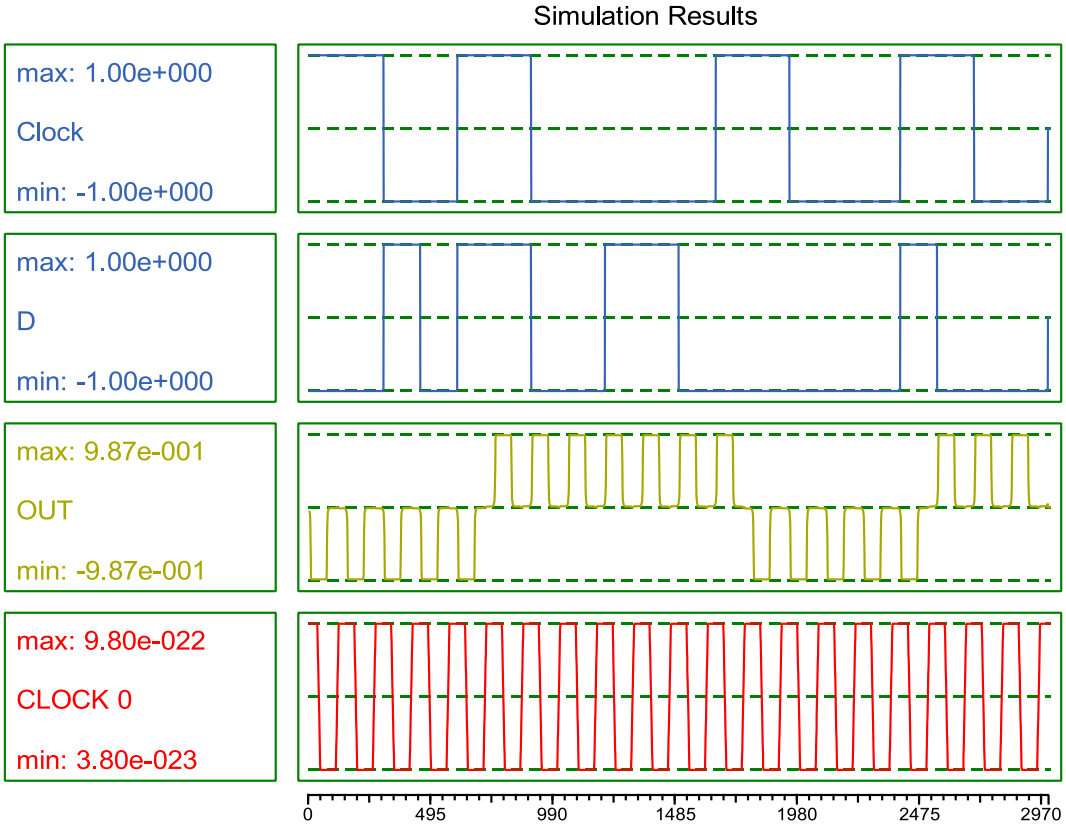

Fig. 12. Simulation results of proposed simple D flip-flop

these applications, it can be said that it is known as an efficient and effective tool in the digital world and information security.

Fig. 10 shows the block diagram of an eight-bit LFSR. According to this block in QCA technology, we first designed an eight-bit LFSR with the least possible number of cells and small area. The proposed structure consists of eight D flip-flops and an XOR gate, as well as a rising edge-sensitive converter for the flip-flops. In this design, we designed an eight-bits random counter without applying two clocks and two converters. The way this structure works is the same as the four-bit LFSR, except that this structure provides us with eight bits and randomly counts from 0 to 255.

According to the block diagram of Fig. 10, we were able to design an eight-bit LFSR in QCA technology with a new technique. Fig. 11 shows this design well. In this design we used only a rising edge sensitive converter and applied an input clock. As Fig. 11

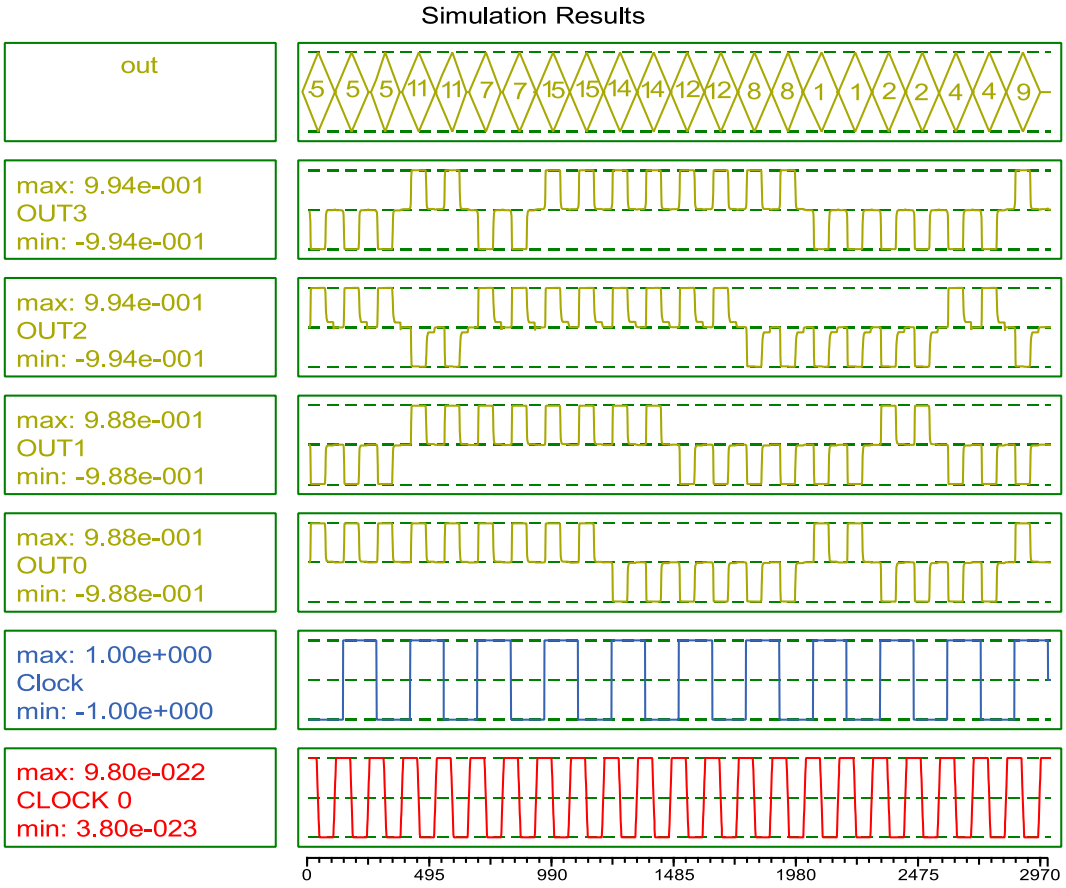

Fig. 13. Simulation results of proposed four-bits LFSR

shows, in this structure, we applied the outputs of the second and third flip-flops to an XOR gate, and finally we entered the output of the XOR gate to the input of the first floor. When the input clock becomes one, the outputs of this structure are placed sequentially. As a result, the XOR gate randomly generates a number and finally the next numbers enter the counting cycle, and this process continues repeatedly. As Fig. 11 shows, the proposed eight-bits LFSR has 281 cells and an area of 0.4 μm^2. It can be said that with this number of cells and small area, this booklet structure is considered the best and most optimal design available in the references. With this number of cells and area, different authorities have only been able to design four-bit LFSR.

4. Simulations and results

In this section, we want to simulate the designed LFSR circuits using QCADesigner version 2.0.3 software. To have accurate results in the presented simulator, we manually applied Vector and set the simulation engine to Coherence Vector and considered the rest of the simulation engine options by default. QCADesigner software is one of the common tools for designing and simulating circuits based on QCA technology. Despite its wide applications, this software comes with limitations and problems that can create challenges for researchers and designers. Some of these limitations are: limited accuracy of simulation, limited scalability, limitation in physical modeling, complexity of clocking implementation, lack of analysis and optimization capabilities, lack of support for all types of cells and structures.

Despite these limitations, QCADesigner is still one of the key tools for researchers in the field of QCA, but developers need to improve and upgrade it to achieve more accurate and practical results.

Fig. 12 shows the output of the proposed rising edge sensitive D flip-flop. As seen in this figure, the output of the proposed flip-flop when the input clock is 1 and the input data value is 1, the output will be 1 until the next edge of the clock. Now, if the input data is zero, the output will be zero until the next edge of the clock. According to the seen output, it can be well understood that the proposed structure has a very accurate and valid output.

Fig. 13 shows the four-bit LFSR output. As this figure shows, the counting numbers start counting randomly according to the state diagram in Fig. 8. Because all the numbers cannot be shown on one page, we only show a part of the count here. To have a correct understanding of the proposed design. As you can see in Fig. 13, the outputs are repeated as the outputs of a shift register to accurately display the random numbers.

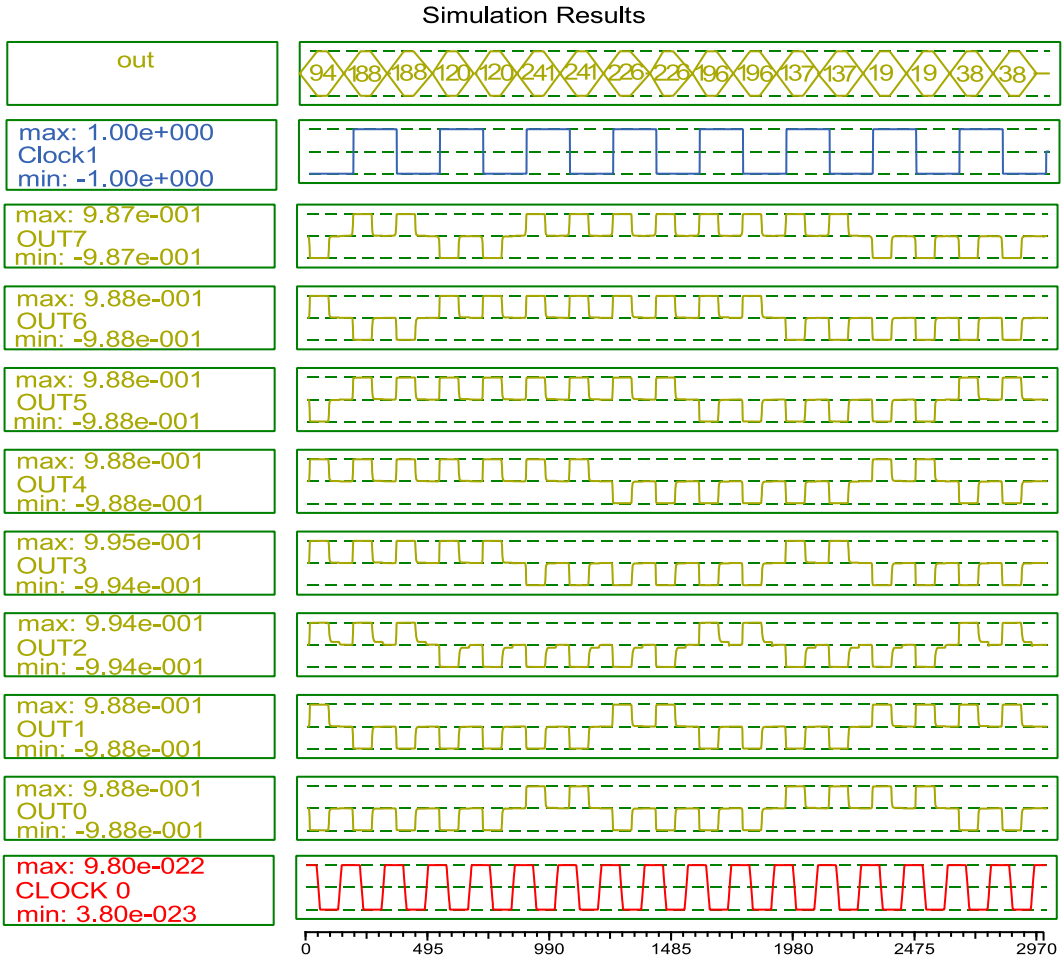

Fig. 14. Simulation results of proposed eight-bits LFSR

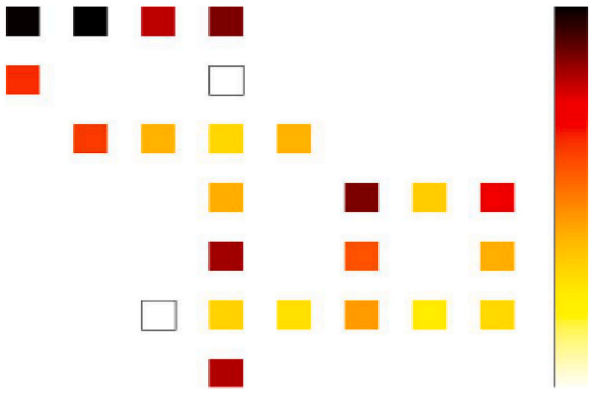

Fig. 15. The energy dissipation map of proposed rising edge D Flip-Flop

Fig. 14 shows the output of the eight-bit LFSR. In this figure, you can see that some numbers from 0 to 255 are counted randomly. Since it is not possible to display all counting numbers from 0 to 255 on one page, we have displayed some of these numbers in the output so that we can see the exact output of this design.

Fig. 15 shows the energy diagram of the proposed flip-flop. This diagram shows the energy consumption of a circuit designed in QCA technology. With this diagram, you can understand how much energy the designed circuit needs for its operation. We know that the lower the energy consumption or the power consumption of a circuit, that circuit has been prioritized for construction and delivers

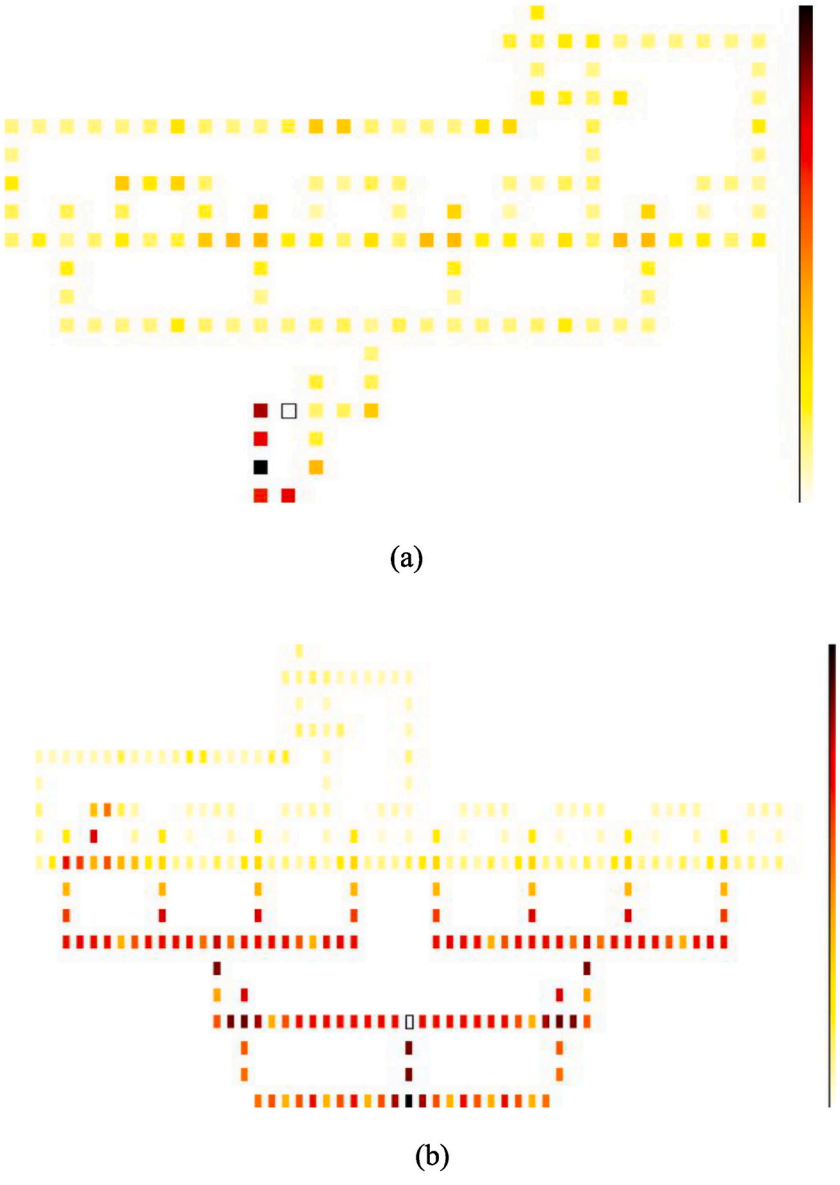

Fig. 16. The energy dissipation map for proposed a) four-bit LFSR, b) eight-bit LFSR

Table 2
Comparison of the proposed D Flip-Flops with other circuits.

Refs.	Cell count	Area($\mu\ m^2$)	Latency($10^{-12}s$)	Set input	Reset input	Triggered
[15]	84	0.11	2.5	No	No	Rising
[21]	56	0.06	2.5	No	No	Rising
[16]	34	0.03	1	No	No	Rising
proposed (Fig. 5)	24	0.01	1	No	No	Rising

more accurate and stable output to us. As Fig. 15 shows, the energy consumption of the proposed D flip-flop is very low, so it delivers accurate and stable output.

Fig. 16 shows the energy consumption diagram of the proposed four and eight bits LFSR. As you can see, designed circuits have low energy consumption and low energy consumption is one of the most important advantages of circuits for construction.

Table 2 is a comparison for the proposed D flip-flop with other references. In this table, our proposed structure has many advantages over other proposed structures, including less cell number, smaller area, and low delay. Therefore, it can be said that the proposed

Table 3
Comparison of the proposed LFSR circuits with other circuits.

Refs.	Bits	Cell count	Area (μm^2)	Cell/Bits	Area/Bits	Latency($10^{-12}s$)	Latch/Flip-flop
[17]	3	290	0.46	96.6	0.1533	3.5	Latch
[18]	3	253	0.41	84.33	0.1366	3.75	Latch
[19]	4	226	0.3	56.5	0.075	4	Flip-flop
[20]	4	157	0.22	39.25	0.055	4.5	Flip-flop
proposed (Fig. 8)	4	144	0.2	36	0.05	2	Flip-flop
proposed (Fig. 10)	8	281	0.4	35.1	0.05	2	Flip-flop

Table 4
Energy dissipation of proposed D Flip-Flops and proposed LFSRs.

	Average switching energy dissipation			Average leakage energy dissipation		
	$\mathbf{1.50E_k}$	$\mathbf{1.00E_k}$	$\mathbf{0.50E_k}$	$\mathbf{1.50E_k}$	$\mathbf{1.00E_k}$	$\mathbf{0.50E_k}$
Fig. 5	**0.0013**	0.0015	0.0019	0.0423	0.0253	**0.097**
Fig. 8	**0.0041**	0.0051	0.0063	0.2517	0.1426	**0.0481**
Fig. 10	**0.1796**	0.2130	0.2477	0.4703	0.2622	**0.0855**

designs are among the best available designs.

Table 3 shows the comparison of the proposed LFSR with other references. With this comparison, the readers of this article can better understand the proposed design.

Table 4 shows the energy consumption of the proposed designs. This table shows us how much energy each designed circuit consumes for different tunneling energy.

5. Conclusion

QCA technology is one of the fast-computing technologies and is widely used for designing digital circuits. D Flip-flops and random counters, or LFSR, are among the most important circuits in the digital system. In the past few years, these circuits have been designed in various sizes based on QCA technology. For this reason, in this paper, first, the rising edge sensitive D flip-flop and then four and eight bits LFSR circuits were designed for the first time with the least possible cell and in a small area. Compared to other references, the designed circuits have various advantages, including a lower number of cells, a smaller area, and most importantly, less energy consumption. It can be said that the designs made are the best and most optimal D flip-flops and random counters. To suggest future work, these designed circuits can be moved towards the design of larger and practical circuits such as detectors, 16-bit counters, 16-bit LFSR and etc.

CRediT authorship contribution statement

Pezhman Kiani Vosta: Writing – original draft, Validation, Software, Methodology, Investigation, Conceptualization. **Mohammad Gholami:** Writing – review & editing, Visualization, Validation, Supervision, Software, Resources, Methodology.

Ethics approval and consent to participate

Not applicable.

Consent for publication

Not applicable.

Availability of data and materials

The data that supports the findings of this study are available from the corresponding author upon reasonable request.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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