







# Foundry-compatible high-resolution patterning of vertically phase-separated semiconducting films for ultraflexible organic electronics

Binghao Wang <sup>1,2,3</sup>, Wei Huang <sup>2</sup>, Sunghoon Lee<sup>3</sup>, Lizhen Huang<sup>2,4</sup>, Zhi Wang<sup>2,5</sup>, Yao Chen<sup>2</sup>, Zhihua Chen<sup>6</sup>, Liang-Wen Feng<sup>2,7</sup>, Gang Wang<sup>2,8</sup>, Tomoyuki Yokota <sup>3</sup>, Takao Someya <sup>3✉</sup>, Tobin J. Marks <sup>2✉</sup> & Antonio Facchetti <sup>2,6✉</sup>

Solution processability of polymer semiconductors becomes an unfavorable factor during the fabrication of pixelated films since the underlying layer is vulnerable to subsequent solvent exposure. A foundry-compatible patterning process must meet requirements including high-throughput and high-resolution patternability, broad generality, ambient processability, environmentally benign solvents, and, minimal device performance degradation. However, known methodologies can only meet very few of these requirements. Here, a facile photolithographic approach is demonstrated for foundry-compatible high-resolution patterning of known p- and n-type semiconducting polymers. This process involves crosslinking a vertically phase-separated blend of the semiconducting polymer and a UV photocurable additive, and enables ambient processable photopatterning at resolutions as high as 0.5  $\mu\text{m}$  in only three steps with environmentally benign solvents. The patterned semiconducting films can be integrated into thin-film transistors having excellent transport characteristics, low off-currents, and high thermal (up to 175  $^{\circ}\text{C}$ ) and chemical (24 h immersion in chloroform) stability. Moreover, these patterned organic structures can also be integrated on 1.5  $\mu\text{m}$ -thick parylene substrates to yield highly flexible (1 mm radius) and mechanically robust (5,000 bending cycles) thin-film transistors.

<sup>1</sup>Joint International Research Laboratory of Information Display and Visualization, Key Laboratory of MEMS of Ministry of Education, School of Electronic Science and Engineering, Southeast University, Nanjing, Jiangsu, PR China. <sup>2</sup>Department of Chemistry and the Materials Research Center, Northwestern University, Evanston, IL, USA. <sup>3</sup>Department of Electrical Engineering and Information Systems, School of Engineering, The University of Tokyo, Bunkyo-ku, Tokyo, Japan. <sup>4</sup>Institute of Functional Nano & Soft Materials (FUNSOM), Jiangsu Key Laboratory for Carbon Based Functional Materials and Devices, Soochow University, Suzhou, Jiangsu, PR China. <sup>5</sup>Research Center for Engineering Technology of Polymeric Composites of Shanxi Province, School of Materials Science and Engineering, North University of China, Taiyuan, Shanxi, PR China. <sup>6</sup>Flexterra Inc., Skokie, IL, USA. <sup>7</sup>College of Chemistry, Sichuan University, Chengdu, Sichuan, PR China. <sup>8</sup>State Key Laboratory for Modification of Chemical Fibers and Polymer Materials, International Joint Laboratory for Advanced Fiber and Low-Dimension Materials, College of Materials Science and Engineering, Donghua University, Shanghai, PR China. ✉email: [someya@ee.t.u-tokyo.ac.jp](mailto:someya@ee.t.u-tokyo.ac.jp); [t-marks@northwestern.edu](mailto:t-marks@northwestern.edu); [a-facchetti@northwestern.edu](mailto:a-facchetti@northwestern.edu)

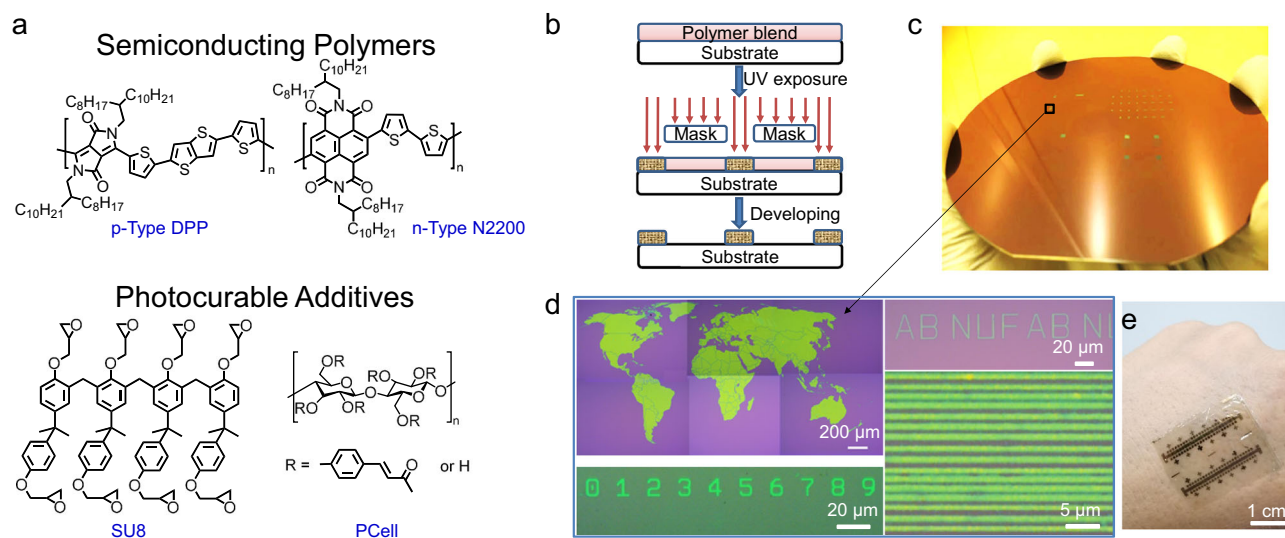
To minimize electronic device feature sizes, eliminate crosstalk in circuitry, and scale-up soft matter optoelectronic device fabrication, foundry-compatible patterning of all functional layers is essential for creating multiple circuitry layers, and systems integration<sup>1–6</sup>. Specifically, high-resolution patterning of robust semiconductor films in thin-film transistor (TFT) arrays must optimize the charge transport and on-current/off-current ratio ( $I_{\text{on}}/I_{\text{off}}$ ) ratio, while achieving reliable deposition by solution-processing of all additional non-TFT components, including the gate dielectric/gate contact in top-gated TFTs, and the source-drain electrodes in top-contact TFTs, as well as planarization/passivation layers in both architectures<sup>7–12</sup>. Several pioneering studies realized patternable photocrosslinked polymer semiconductors by appending crosslinkable moieties to the polymer backbone. Following these approaches, crosslinked patterned films of various polythiophenes with 50–100  $\mu\text{m}$  features and TFT mobilities of  $10^{-3}$ – $10^{-1} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  were demonstrated<sup>13–16</sup>. To further enhance pattern resolution, alternative approaches have focused on developing chemically orthogonal photoresist/protective layers to preserve the underlying semiconductor layer integrity during photolithography<sup>1,8,17,18</sup>. In this way high-resolution features (1–5  $\mu\text{m}$ ) were realized with mobilities of ca.  $10^{-1} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . Nevertheless, foundry-compatible patterning methodologies that are low-cost, ambient processable, environmentally benign, highly efficient and reliable, and enable high-resolution patterned features without compromising device performance have remained elusive. Thus, the existing patternable semiconductors for orthogonal photolithography are chemically and/or morphologically unstable in most solvents as well as metal etchants, and to date cannot be realistically implemented in circuitry fabrication. Moreover, the crosslinking of functionalized polymeric semiconductors typically relies on high deep-UV radiation doses in inert atmosphere, which is incompatible with efficient FAB processing.

Here we report a foundry-compatible wafer-scale patterning approach for creating polymeric semiconducting layers with fidelity at the 0.5  $\mu\text{m}$  resolution scale. The robust patterned semiconducting layers are produced from a phase-separated blend of readily available p- or n-type polymeric semiconductors and a compatible photo-crosslinkable additive (Fig. 1a). The patterned layers are chemically inert to aggressive

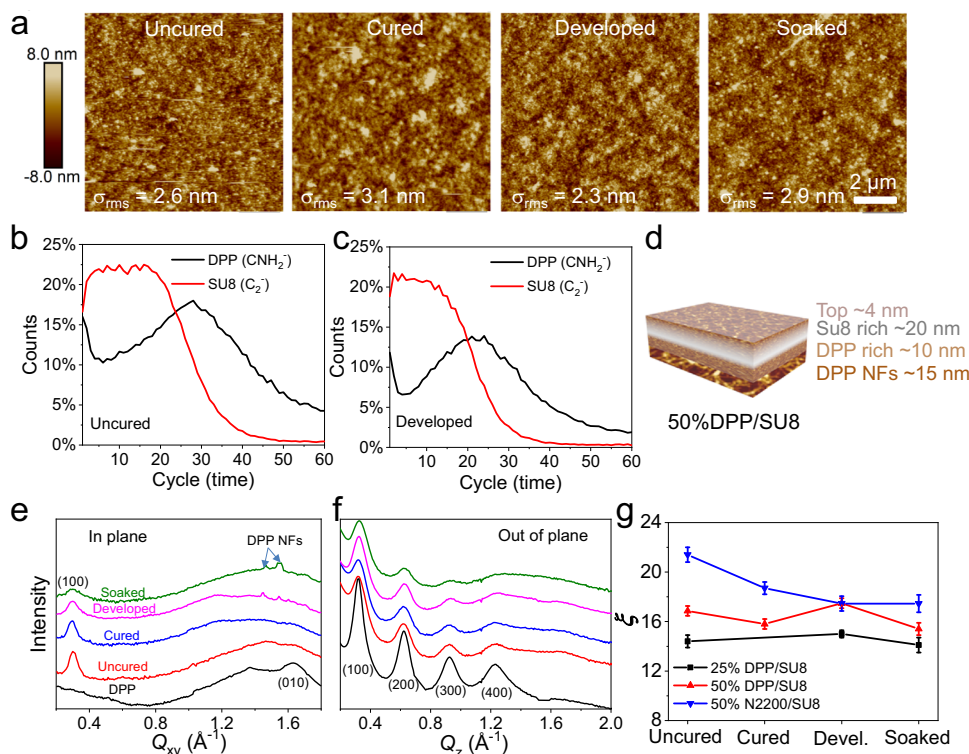
aqueous and organic solvents, and thereby withstand subsequent deposition and patterning of the additional organic layers and/or metal contacts used in the circuitry fabrication. To illustrate the generality of this methodology and availability of all components, we employ both p-type, poly[2,5-bis(2-octyldodecyl)-3,6-diketopyrrolopyrrole-alt-5,5'-(2,5-di(thien-2-yl)thieno[3,2-*b*]thiophene)] (DPP) and n-type, poly[[*N,N*-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)] (N2200) semiconducting polymers paired with photocurable additives (PAs) such as commercially available SU-8 2000.5 (abbreviated SU8) and a Northwestern cinnamate-functionalized cellulose polymer abbreviated PCell<sup>19</sup>. The vertical phase separation (VPS) and semiconductor nanofiber morphology in the resulting blend films are confirmed by comprehensive characterization techniques including atomic force microscopy (AFM), time-of-flight secondary ion mass spectrometry (ToF-SIMS), and 2D grazing incidence wide angle X-ray scattering (GIWAXS). The patterning process is highly efficient and minimizes waste since it requires only 3 steps, versus 7+ steps for conventional photolithography (Fig. 1b and Supplementary Fig. 1). Furthermore, both the film deposition and patterning processes can be effectively carried out using environmentally benign green solvents such as tetrahydrofuran (THF) as a proof-of-concept. The fabricated OTFTs have carrier mobilities of 0.1–0.24  $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , comparable to those of the pristine polymers, but with far more efficient switching (subthreshold swing = 1.4 V dec<sup>-1</sup>), greater thermal stability (175 °C), and superior mechanical durability (5000 bending cycles at a radius of 1 mm).

## Results

**Semiconductor blend film and device fabrication.** The semiconducting polymers DPP and N2200 were selected because they are among the most efficient p- and n-type semiconductors for OTFTs while SU8 and PCell are inexpensive and readily available. Regarding the OTFT architectures, and to demonstrate architecture generality, we preferentially investigated bottom-gate top-contact (BGTC) OTFTs for DPP and top-gate bottom-contact (TGBC) OTFTs for N2200 since they are those where the pristine



**Fig. 1** Materials and methodology used to produce high-resolution patterned ultraflexible soft matter electronic circuitry. **a** Chemical structures of the semiconductors and photocurable additives used in this study. **b** Schematic of the photolithographic process. **c** Photograph of a patterned 50% DPP/SU8 (DPP:SU8 = 1:1 w/w) film on a 4-inch  $\text{SiO}_2/\text{Si}$  wafer. **d** Optical images of 50% DPP/SU8 films with various patterned topologies. **e** Photographic image of ultraflexible 50% DPP/SU8-based organic TFTs (OTFTs) on a human hand.



**Fig. 2** Characterization of materials phase separation processes enabling transistor fabrication for high-resolution patterned ultraflexible soft matter electronic circuitry. **a** AFM images of a 50% DPP/SU8 films at different stages of the photolithographic process, demonstrating excellent chemical resistance. The ToF-SIMS depth profiles for **b** uncured and **c** developed 50% DPP/SU8 films in uncured 50% DPP/SU8 films into SU-8 rich, DPP-rich, and DPP nanofibers, based on the AFM and ToF-SIMS characterization. **d** Schematic of VPS in uncured 50% DPP/SU8 films. **e** In-plane and **f** out-of-plane GIWAXS line cuts of the indicated 50% DPP/SU8 films. **g** Coherence lengths ( $\xi$ ) derived from out-of-plane (200) reflections for DPP/SU8 and in-plane (100) reflections for 50% N2200/SU-8 after the indicated processing conditions. The error bars provide the standard deviation.

polymers perform the best. Details of the semiconductor blend film deposition, curing/patterning, and OTFT fabrication processes are reported in the Supporting Information. Briefly, in a typical experiment for bottom-gate top-contact (BGTC) OTFT fabrication, used for the p-type DPP-based devices, the semiconductor/PA solution ( $x\%$  in weight semiconductor vs. PA,  $x = 25, 50, \text{ and } 75$ ; total concentration =  $4 \text{ mg mL}^{-1}$ ) was spin-coated on trichloro(octyl)silane-treated  $\text{SiO}_2/\text{Si}$  substrates at 1500 rpm for 30 s in ambient with  $\sim 30\%$  relative humidity. After baking the films at  $95^\circ\text{C}$  for 1 min, they were exposed through a shadow mask to a 365 nm ultraviolet (UV) light (Electrodeless UV lamp, dose =  $60\text{--}80 \text{ mJ cm}^{-2}$ ) or by a maskless aligner for high-resolution patterning, followed by annealing at  $95^\circ\text{C}$  for 2 min (Fig. 2b). Next, the resulting cured  $x\%$  DPP/SU8 blend films were developed with  $\text{CHCl}_3$  for 5 s, to achieve the desired patterned films with thickness of 40–70 nm, depending on the semiconductor and semiconductor/PA weight ratio. The BGTC OTFT structures were completed by thermally depositing gold source/drain contacts with channel width/length ( $W/L, \mu\text{m}$ ) of 1000/100 or 40/10, defined by metal mask or lift-off process, respectively (*vide infra*). Top-gate bottom-contact (TGBC) OTFTs were employed for n-type N2200-based devices, which were fabricated/patterned on glass substrates with thermally evaporated Au source-drain contact ( $W/L = 1000/100$ ) and completed by spin-coating a  $740 \pm 10 \text{ nm}$ -thick poly(methyl methacrylate) (PMMA) gate dielectric layer ( $C_i = 3.6 \text{ nF cm}^{-2}$ ), and thermally evaporating a gold gate contact. Fig. 1c, d, and Supplementary Fig. 2 show representative optical images of photo-patterned DPP:SU8 films, demonstrating excellent reproducibility and reliability over a large scale for patterns of different shapes and feature sizes. The minimum features achievable are  $\sim 0.5 \mu\text{m}$ , limited by the

maskless aligner (Heidelberg MLA150), and the calculated line width roughness (LWR) and line edge roughness (LER) are  $97.8 \pm 1.5 \text{ nm}$  and  $70.1 \pm 1.2 \text{ nm}$ , respectively. These values are superior to those for conventional several micrometer-thick photoresists (Supplementary Figs. 3 and 4). The generality of this three-step patterning process was verified with other blends such as DPP/PCell, N2200/SU8, and N2200/PCell (Supplementary Figs. 4–8) on glass or ultraflexible polymer substrates (Fig. 1e).

**Blend film morphological characterization.** The film morphologies and microstructures of the semiconductor/PA films during the patterning process were investigated by AFM, ToF-SIMS, and GIWAXS. Fig. 2a and Supplementary Fig. 9 show representative AFM images of pristine DPP and 50% DPP/SU8 (DPP:SU8 = 1:1 w/w) films before photocuring (uncured), after UV irradiation (cured), after development (developed/patterned), and after 24 h immersion in  $\text{CHCl}_3$  (soaked). The pristine DPP films (120 nm thick) exhibit uniform crystalline domain structures with an rms roughness ( $\sigma_{\text{rms}} = 1.7 \text{ nm}$ ), while the 50% DPP/SU8 film ( $\sim 50 \text{ nm}$  thick) has smaller crystalline domains and a slightly rougher surface ( $\sigma_{\text{rms}} = 2.6 \text{ nm}$ ). Negligible morphological and thickness changes are evident for 50% DPP/SU8 films after UV irradiation. After developing, the film thickness is found to contract slightly to  $\sim 45 \text{ nm}$  due to partial removal of the top DPP/SU8 portion. Impressively, negligible morphological and thickness changes are observed on 24 h immersion in  $\text{CHCl}_3$ , retaining a  $\sigma_{\text{rms}} = 2.9 \text{ nm}$ . This blend film thickness and morphology evolution with curing/developing indicate multilayer VPS in the semiconductor/polymer blends as supported by the ToF-SIMS data (Fig. 2b–d and Supplementary Fig. 10). The  $\text{C}_2^-$  and  $\text{CNH}^-$  ion signals are



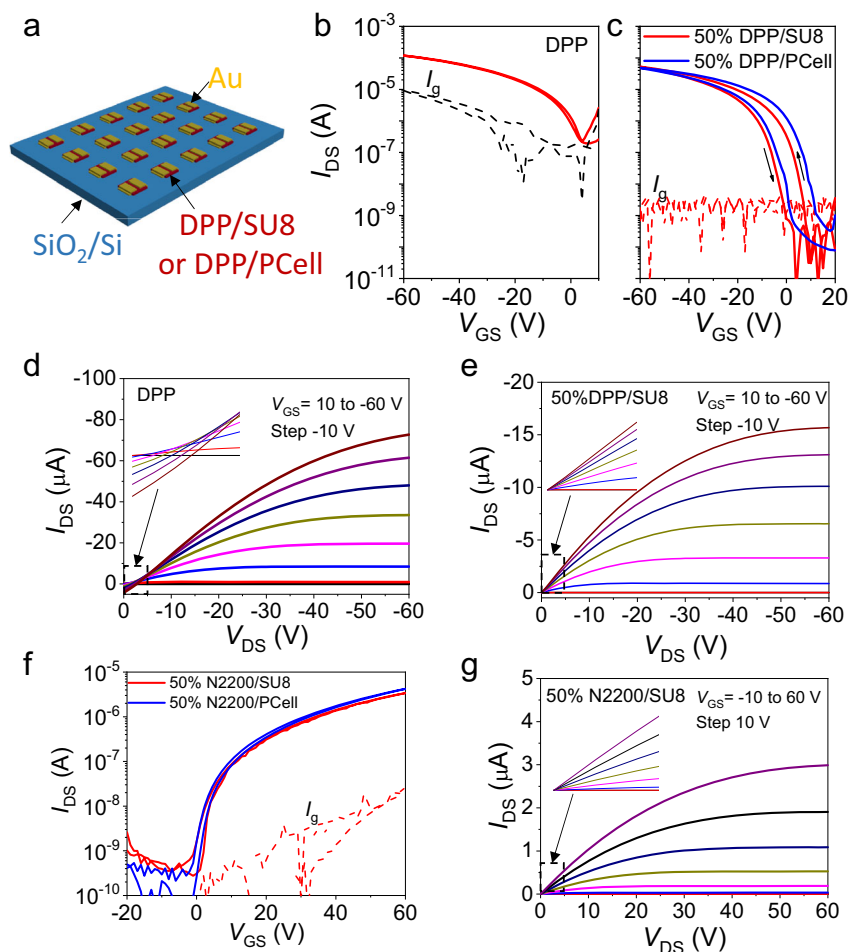
signatures of SU8 and the DPP, respectively, and their ratio can be used to assay the distribution of the two components with film depth.<sup>25</sup> Thus, the ToF-SIMS depth profile for uncured 50% DPP/SU8 samples (1 etching cycle represents  $\sim 1$  nm, Fig. 2b) indicates formation of a multilayer structure (Fig. 2d) with a top layer having comparable SU8-DPP contents and of thickness  $\sim 4$  nm, a central layer greatly enriched in SU8 with thickness of  $\sim 20$  nm, and a lower layer primarily consisting of DPP ( $\sim 10$  nm), and then exclusively (another  $\sim 15$  nm), composed of DPP nanofibers (NFs).<sup>20–26</sup> Regarding the developed 50% DPP/SU8 sample, which is only  $\sim 5$  nm thinner than the undeveloped sample, its ToF-SIMS result indicates a similar composition profile with only the film upper portion affected. However, the film bulk, and particularly the bottom pure DPP layer, remains intact. GIWAXS measurements on the DPP-based films (Fig. 2e, f and Supplementary Figs. 11 and 12) reveal that both pure DPP and 50% DPP/SU8 blends have a predominant edge-on orientation of the polymer chains in accord with DPP literature reports.<sup>27</sup> Specifically, along the in-plane direction (Fig. 2e and Supplementary Table 1), the typical broad (010) DPP reflection at  $1.65 \pm 0.0011 \text{ \AA}^{-1}$ , corresponding to a  $\pi$ - $\pi$  stacking distance ( $d_{\pi}$ ) of  $0.38 \pm 0.0004$  nm, is weakened in the 50%DPP/SU8 films. However, other small peaks ( $1.48/1.55/1.62/1.72 \text{ \AA}^{-1}$ ) present in the  $\text{CHCl}_3$ -developed and soaked 50%DPP/SU8 films are assigned to DPP nanofibers.<sup>28</sup> Thus, SU8 promotes DPP aggregation in solution or during the film deposition, yielding fibers with polymer chains  $\pi$ - $\pi$  stacked at  $\sim 0.4$  nm distances. This morphology is known to enhance conjugation length and carrier mobility in  $\pi$ -polymers.<sup>29,30</sup> Furthermore, a (100) reflection appears in all blends at  $\sim 0.30$  nm (absent in pristine DPP films), corresponding to lamellar spacings of  $d_{\text{lam}} = 2.07\text{--}2.13$  nm. This may reflect formation of a mixed orientation morphology in blending (Supplementary Table 2). Along the out-of-plane direction (Fig. 2f), all films exhibit a family of ( $n00$ ) reflections corresponding to a lamellar stacking located at  $\sim 0.32 \text{ \AA}^{-1}$  and corresponding to a  $d_{\text{lam}}$  of  $1.93\text{--}1.99$  nm. The lamellar stacking coherence lengths ( $\xi$ ) for all films are summarized in Fig. 2g and Supplementary Tables 1–4.<sup>31</sup> The  $\xi$  of the as-deposited DPP is 24.6 nm and falls to 16.8 nm for the uncured 50% DPP/SU8 film. The  $\xi$  has minimal change on UV irradiation,  $\text{CHCl}_3$  development, or 24 h immersion in  $\text{CHCl}_3$ , further demonstrating the excellent UV and chemical resistance. Similar trends are observed for other x% DPP/SU8 and x% DPP/PCell blends (Supplementary Note 1, Supplementary Figs. 13–15).

AFM images of 25% DPP/SU8 films from different processing conditions in Supplementary Fig. 16, clearly reveal the presence of DPP nanofibers on the top surface, which are removed after developing in  $\text{CHCl}_3$ . Regarding PA effects, the uncured 50% DPP/PCell films (Supplementary Fig. 17) exhibit a distinctive fibrillar surface morphology ( $\sigma_{\text{rms}} = 4.7$  nm)<sup>32,33</sup>. The film morphology is unchanged after UV irradiation, but the film smoothens after  $\text{CHCl}_3$  development for 5 s ( $\sigma_{\text{rms}} = 3.1$  nm) and eventually the fibrous morphology disappears after 24 h  $\text{CHCl}_3$  immersion, yielding a fish scale morphology. By decreasing (25% DPP/PCell) or increasing (75% DPP/PCell) the semiconductor contents in the blend, similar morphological evolutions are noted (Supplementary Fig. 18). In the case of N2200-based films (Supplementary Figs. 9 and 19), pure N2200 films exhibit a typical smooth surface with  $\sigma_{\text{rms}}$  of only 0.3 nm.<sup>34</sup> The 50% N2200/SU8 films also exhibit a fibrillar morphology and  $\sigma_{\text{rms}} = 2.1$  nm; however, the fibrous structure decreases on UV irradiation and the film exhibits a  $\sigma_{\text{rms}} = 0.8$  nm. After development, these films also exhibit a fish scale morphology with a greatly increased  $\sigma_{\text{rms}} = 3.5$  nm again due to partial removal of the N2200/SU8 discontinuous phase<sup>33</sup>. Note that selective

removal of SU8 or PCell from the uncured blends with the developing solvent (See Experimental Section for details) leaves  $\sim 15$  nm thick fibrillar DPP or N2200 films consistent with a semiconductor-rich bottom interface (Supplementary Fig. 20), demonstrating the VPS between semiconductors and PAs<sup>20,25,33,35,36</sup>. Impressively, these fibrillar films, exhibiting good phase purity and connectivity, are OTFT-active (Supplementary Fig. 21).

Regarding the GIWAXS results for N2200-based films, pure N2200 films (Supplementary Fig. 22) exhibit typical preferential  $\pi$ -face-on polymer crystallite orientation with a broad  $\pi$ -stacking peak (010) at  $1.61 \pm 0.0012 \text{ \AA}^{-1}$  ( $d_{\pi} = 3.9 \pm 0.003 \text{ \AA}$ ) known for this polymer.<sup>37</sup> The in-plane plot shows four orders of lamellar reflection with the lowest order (100) located at  $0.25 \pm 0.0002 \text{ \AA}^{-1}$  ( $d_{\text{lam}} = 2.48 \pm 0.004$  nm) and three orders of (001) backbone periodicity the first located at  $0.46 \pm 0.0011 \text{ \AA}^{-1}$  ( $d_{\text{back}} = 1.38 \pm 0.007$  nm).<sup>38</sup> When N2200 is blended with SU8 at 50%, the out-of-plane (010) and in-plane (00n) reflections are strongly suppressed vs. that of neat N2200 while the other reflections, such as the ( $n00$ ) reflections, persist or even increase in intensity (Supplementary Figs. 23 and 24). However, comparing the plots proceeding from uncured to soaked blend films, the patterning process has minimal effect on the N2200 macromolecular packing and texturing. Thus, the  $\xi$  of the (100) peak for the 50% N2200/SU8 films (Fig. 2g, Supplementary Table 5) slightly decreases from  $21.4 \pm 0.6$  nm (as-deposited) to  $18.7 \pm 0.5$  nm (UV cured), then to  $\sim 17.4$  nm for both the developed and 24 h immersion in SU8 developer films. Similar trends are observed for other x% N2200/SU8 and 50% N2200/PCell blends (Supplementary Figs. 22 and 25). These comprehensive characterizations for various semiconductor/PA films demonstrate that blending with the PA, as well as curing and development, does not compromise semiconductor film texturing. Furthermore, all blends remain macroscopically uniform and continuous. Finally, VPS and nanofiber formation during the film deposition process is confirmed. Thus, the combined characterizations demonstrate positive morphological and structural characteristics which are critically important for high-resolution patterning of the semiconductor film and efficient charge transport in the corresponding devices as verified in the next section.

**Device electrical properties and stability.** Next, the performance of the DPP BGTC and N2200 TGBC OTFTs was evaluated, starting with large channel ( $W/L = 1000/100 \mu\text{m}$ ) devices based on pristine/unpatterned DPP as well as developed/patterned x% DPP/SU8 and x% DPP/PCell films (Fig. 3a). Note that the DPP-based devices exhibit typical  $p$ -type behavior as seen in the transfer and output plots of Fig. 3b–e. The DPP OTFTs exhibit very high off-currents (in the level of  $10^{-7}$  A), large subthreshold swings ( $SS = 5.9 \pm 0.3 \text{ V dec}^{-1}$ ), and small current on/off ratios ( $10^2\text{--}10^3$ ), reflecting gate/parasitic leakage currents typical of high-mobility/unpatterned semiconductors<sup>39,40</sup>. In contrast, the patterned 50% DPP/SU8 and 50% DPP/PCell devices (semiconductor area =  $1.1 \times 1.3 \text{ mm}^2$ ) exhibit low off/gate currents ( $10^{-10}$  A, instrumentation-limited), lower SS ( $2.2 \pm 0.2 \text{ V dec}^{-1}$ ), high current on/off ratios ( $>10^6$ ) and textbook output curves. Electrical parameters were extracted using standard MOSFET equations and are summarized in Table 1. The average carrier mobility ( $\mu$ ) and threshold voltage ( $V_T$ ) for the DPP devices are  $0.4 \pm 0.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $20.2 \pm 2.5 \text{ V}$ , respectively. These values are comparable to previously reported pristine DPP data in cases where the mobility was realistically estimated<sup>20,28,41,42</sup>. The mobilities of the patterned 50% DPP/SU8 and 50% DPP/PCell OTFTs are  $0.24 \pm 0.04 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  ( $V_T = 18.6 \pm 2.3 \text{ V}$ ) and  $0.20$



**Fig. 3** Response characteristics of patterned organic p- and n-type transistors. **a** Schematic OTFT structure using patterned DPP-based films and evaporated Au source/drain electrodes. Transfer curves of OTFTs based on **b** pristine DPP, **c** patterned 50% DPP/SU8 and 50% DPP/PCell films. Output curves of OTFTs using, **d** pristine DPP, **e** patterned 50% DPP/SU8 films. **f** Transfer curves of OTFTs based on 50% N2200/SU8 and 50% N2200/PCell films. **g** Output curves of OTFTs based on patterned 50% DPP/SU8 films. All devices here have W/L of 1000/100  $\mu\text{m}$ .

$\pm 0.03 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  ( $V_{\text{T}} = 29.7 \pm 2.8 \text{ V}$ ), respectively, indicating minimal degradation during patterning. Varying the DPP content in the blend to lower (25%) and higher (75%) values does not significantly change the transport characteristics or field-effect mobility, which remains in the range of  $0.1\text{--}0.22 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  (Supplementary Figs. 26 and 27). Interestingly, the  $V_{\text{T}}$ s for the 25% DPP/SU8 and 25% DPP/Cell OTFTs are much lower than those of the pristine DPP and other DPP-based blends. Seen from Supplementary Table 2, we believe that when the DPP concentration is lower than a critical point (perhaps percolation related), the edge-on packing contribution (62.6% for 25%DPP/SU8) is much lower than those of 50%DPP/SU8 (94.9%) and pristine DPP (99.6%). Thus, different switching behavior is observed at high  $V_{\text{g}}$  (shown in the transfer curves, Supplementary Fig. 27), resulting in much lower  $V_{\text{T}}$ s. Finally, DPP and 25% DPP/SU8 OTFTs with TGBC and BGBC (bottom-gate bottom-contact) architectures were also evaluated. However, they all exhibit poor performance likely due to unfavorable charge injection from pristine Au electrodes into DPP in bottom-contact devices (Supplementary Fig. 28).

Regarding the pristine N2200, x% N2200/SU8, and x% N2200/PCell TGBC devices, Figs. 3f, g and Supplementary Fig. 29 show representative transfer and output curves. The patterned devices exhibit optimal  $I\text{--}V$  characteristics with lower off-currents ( $10^{-10} \text{ A}$ ), lower gate currents ( $10^{-8} \text{ A}$ ), lower SS ( $\sim 2.0 \text{ V dec}^{-1}$ ), and near-zero turn on voltages vs. the unpatterned N2200 TFTs, while the electron mobilities of  $0.09 \pm 0.02 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  are comparable to

those of literature N2200 devices.<sup>43</sup> To avoid the toxic chloroform solvent used above and to make this fabrication and patterning process potentially acceptable in semiconductor FABs, the green solvent THF was used as proof-of-concept for 50% N2200/SU8 films. It is found that these films exhibit satisfactory patterning and electrical performance (Supplementary Fig. 30). Note, we also attempted to fabricate DPP TFTs with THF, however, this semiconductor is not sufficiently soluble in this solvent for processing.

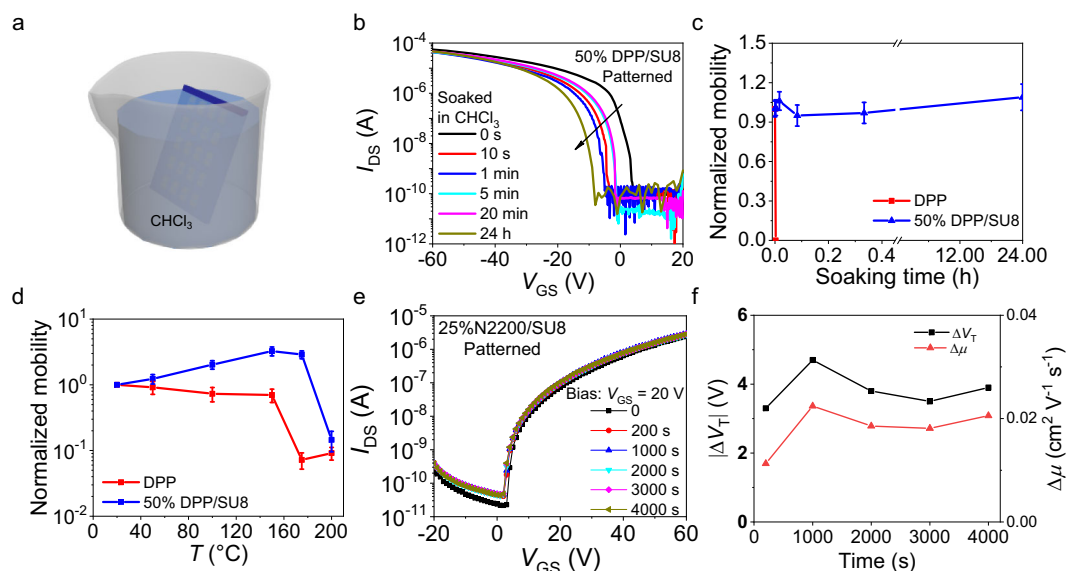
Next, we evaluated the chemical, thermal and bias stabilities of our patterned OTFTs vis-à-vis those based on the pristine semiconductors. As noted in the morphology and GIWAXS sections above, the DPP/SU8 films are stable upon long-term exposure to  $\text{CHCl}_3$ . Thus, we investigated how the corresponding TFTs, fabricated on robust  $\text{Si/SiO}_2$  gate contact/dielectric platforms respond to a similar treatment. The data in Figs. 4a-3c indicate that while the DPP TFTs are immediately damaged upon immersion in  $\text{CHCl}_3$ , the patterned 50% DPP/SU8 devices function even after  $\text{CHCl}_3$  immersion for 24 h, but with the transfer curve shifting negative with increasing immersion time and pinned maximum on-current and carrier mobility. The negative shift probably originates from additional charge traps due to solvent intercalation and nanoscopic morphological changes in the semiconductor during extended solvent immersion. Regarding the thermal stability, blending organic semiconductors with high glass-transition temperature ( $T_{\text{g}}$ ) insulating

**Table 1 Performance metrics of selected TFTs based on pristine semiconductor and patterned polymer blend films<sup>a</sup>.**

Semiconductor	Device structure	W/L ( $\mu\text{m}/\mu\text{m}$ )	$\mu$ ( $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ )	$I_{\text{on}}/I_{\text{off}}$	$V_T$ (V)	SS ( $\text{V dec}^{-1}$ )	
DPP	BGTC	1000/100	$0.4 \pm 0.05$	$<10^3$	$20.2 \pm 2.5$	$5.9 \pm 0.3$	
25% DPP/SU8			$0.1 \pm 0.02$	$10^5\text{--}10^6$	$0.63 \pm 0.1$	$2.4 \pm 0.2$	
50% DPP/SU8			$0.24 \pm 0.04$	$10^5\text{--}10^6$	$18.6 \pm 2.3$	$2.2 \pm 0.2$	
75% DPP/SU8			$0.22 \pm 0.03$	$10^5\text{--}10^6$	$20.0 \pm 2.6$	$2.3 \pm 0.1$	
25% DPP/Cell			$0.1 \pm 0.02$	$10^5\text{--}10^6$	$7.1 \pm 0.5$	$2.7 \pm 0.2$	
50% DPP/Cell			$0.2 \pm 0.03$	$10^5\text{--}10^6$	$29.7 \pm 2.8$	$2.4 \pm 0.1$	
75% DPP/Cell			$0.2 \pm 0.02$	$10^4\text{--}10^5$	$25.4 \pm 2.0$	$3.2 \pm 0.2$	
50% DPP/SU8			40/10 <sup>b</sup>	$0.1 \pm 0.02$	$10^5\text{--}10^6$	$11.3 \pm 1.4$	$1.4 \pm 0.08$
Ultraflexible			1000/100	$0.03 \pm 0.01$	$10^3\text{--}10^4$	$20.5 \pm 3.2$	$3.7 \pm 0.4$
50% DPP/SU8			TGBC	1000/100	$0.1 \pm 0.02$	$10^4\text{--}10^5$	$9.9 \pm 1.0$
25% N2200/SU8	$0.06 \pm 0.01$	$-10^5$			$18.3 \pm 2.3$	$3.0 \pm 0.2$	
50% N2200/SU8	$0.09 \pm 0.02$	$10^4\text{--}10^5$			$5.6 \pm 0.5$	$2.1 \pm 0.2$	
50% N2200/SU8 (THF)	$0.08 \pm 0.02$	$-10^4$			$6.8 \pm 0.5$	$3.0 \pm 0.3$	
50% N2200/Cell	$0.1 \pm 0.02$	$10^4\text{--}10^5$			$8.3 \pm 0.7$	$2.0 \pm 0.1$	
Ultraflexible	1000/50	$0.01 \pm 0.005$			$10^4\text{--}10^5$	$17.9 \pm 2.9$	$3.6 \pm 0.4$
50% N2200/SU8							

<sup>a</sup>Data collected from >15 devices. Chloroform used solvent unless otherwise indicated.

<sup>b</sup>W/L defined by lift-off process.



**Fig. 4 Chemical and thermal stability of DPP and 50% DPP/SU8 devices.** **a** Schematic of device soaking in  $\text{CHCl}_3$ . **b** Transfer curves and **c** normalized mobility of DPP and patterned 50% DPP/SU8 devices after  $\text{CHCl}_3$  immersion for various times. The  $V_{\text{DS}}$  is  $-60$  V. The error bars are the standard deviation. **d** Normalized mobilities of DPP and 50% DPP/SU8 devices evaluated at various temperatures. The error bars are the standard deviation. **e** Transfer curves evolution of patterned 25%N2200/SU8 OTFTs under positive gate bias stress at a  $V_{\text{GS}}$  of  $20$  V for up to  $4000$  s. The  $V_{\text{DS}}$  is  $60$  V. **f** Threshold voltage shift ( $\Delta V_T$ ) and mobility shift ( $\Delta\mu$ ) of the patterned 25%N2200/SU8 devices OTFTs under positive gate bias stress.

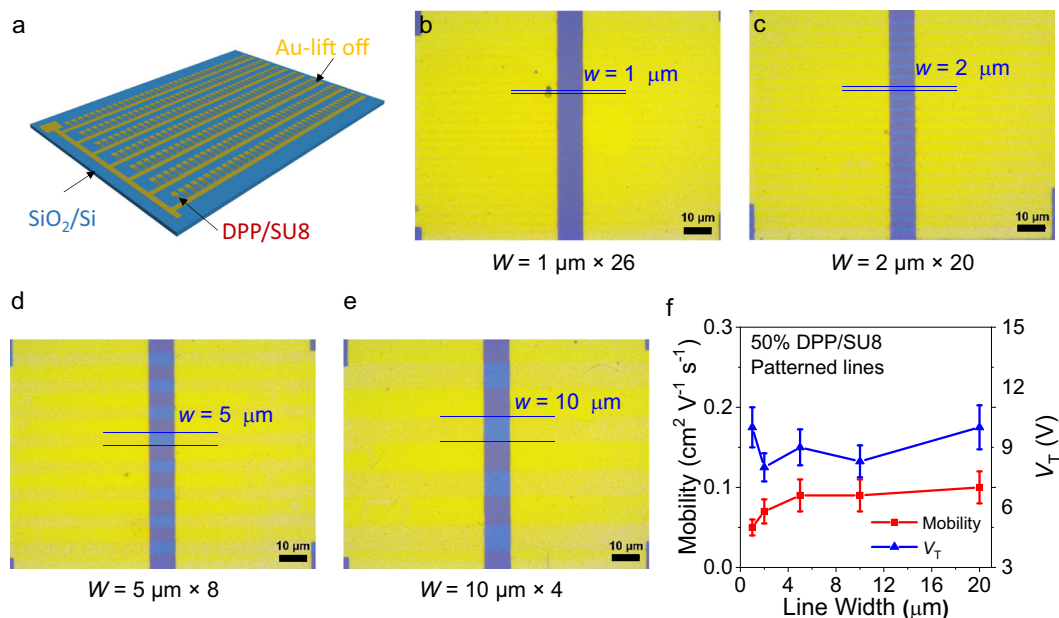
polymers has proved to be an efficient way to improve film morphological and device thermal stability.<sup>44</sup> Considering the high SU8  $T_g$  ( $\sim 200^\circ\text{C}$ ), we next compared the performance changes of OTFTs in ambient based on DPP and 50%DPP/SU8 films. As shown in Fig. 4d and Supplementary Fig. 31, the 50% DPP/SU8 devices retain a high  $\mu$  of  $0.7 \pm 0.1 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  upon thermal annealing up to  $175^\circ\text{C}$ , while the DPP ones do not function at temperatures higher than  $150^\circ\text{C}$ .

The operational stability of representative N2200/SU8 and DPP/SU8 OTFTs was also probed by applying a gate voltage ( $V_{\text{GS}} = \pm 20$  V) for up to  $4000$  s (Figs. 4e, f, Supplementary Fig. 32). The results show that TGBC 25%N2200/SU8 devices exhibit excellent bias stability with threshold voltage shift ( $\Delta V_T$ ) and mobility shift ( $\Delta\mu$ )

below  $4$  V and  $0.02 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ , respectively. BGTC patterned 50% DPP/SU8 devices are also tested and exhibit larger  $\Delta V_T$  ( $\sim 16$  V) and  $\Delta\mu$  ( $\sim 0.06 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ ) variation than the DPP devices during the bias test ( $V_{\text{GS}} = -20$  V for up to  $4000$  s). However, note that pristine BGTC DPP TFTs exhibit a similar stress behavior [ $\Delta V_T$  ( $\sim 12$  V) and  $\Delta\mu$  ( $\sim 0.05 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ )]. These data indicate that, as expected, a top-gate architecture better stabilizes devices during bias stress in ambient and, more importantly, the addition of PA does not impact the device stability of either device.

**High-resolution patterning and ultraflexible devices.** Owing to the excellent chemical stability of the above semiconducting





**Fig. 5 High-resolution patterned DPP/SU8 lines and corresponding device performance.** **a** Schematic of TFT arrays based on patterned DPP/SU8 films and photolithographically defined (lift off) Au source/drain electrodes. **b–e** Optical images of patterned 50% DPP/SU8 lines (horizontal) and Au contacts (vertical) on SiO<sub>2</sub>/Si substrates. The scale bars are 10  $\mu\text{m}$ . **f** Mobility and threshold voltage evolution of 50% DPP/SU8 devices on OTS-treated SiO<sub>2</sub>/Si substrates with varied line widths.

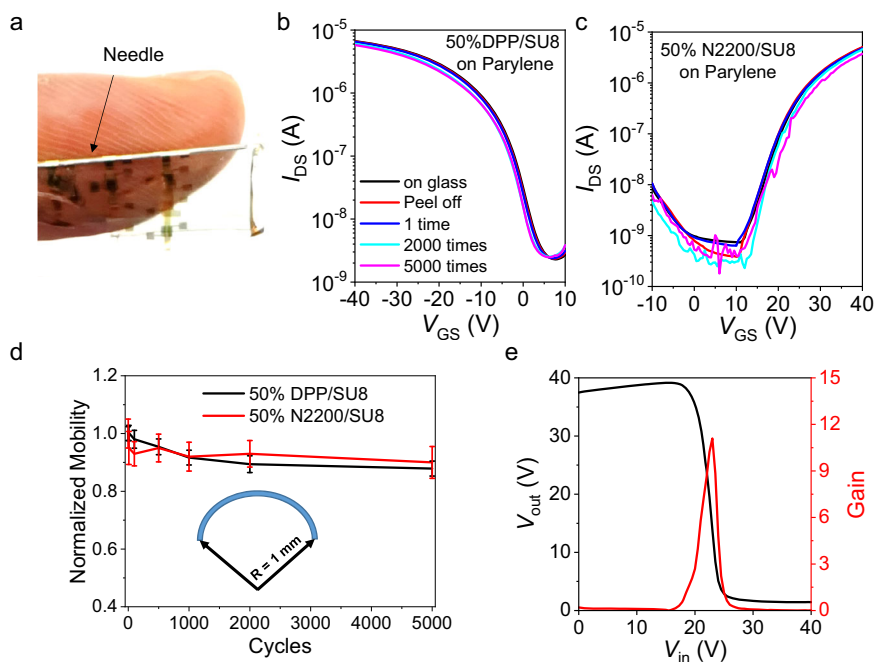
polymer blends, additional BGTC device architectures were fabricated by combining patterned 50% DPP/SU8 semiconducting lines of different widths ( $w = 1\text{--}20 \mu\text{m}$ ) with photolithographically patterned Au Source/Drain electrodes (layout in Fig. 5a). Note, 50% DPP/SU8 lines were fabricated as discussed above by photo exposure/CHCl<sub>3</sub> development, while Au patterning used a lift-off process involving the S1813 photoresist, the aggressive AZ<sup>®</sup> 400 K developer (alkaline solution), and acetone. Fig. 5b–e demonstrate that metal electrodes with channel length/width of 10/100  $\mu\text{m}$  can be precisely patterned on the semiconducting lines. Representative TFT transfer plots and transport parameters of TFTs based on these channel topologies are shown in Fig. 5f and Supplementary Fig. 33. Note here that the effective channel width,  $W$ , of these devices is  $n \times w$ , where  $n$  are the number of semiconducting lines in the channel area. The hole mobility of these TFTs remains  $0.09 \pm 0.02 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  when the line width is greater than 5  $\mu\text{m}$ , then gradually falls to  $0.05 \pm 0.01 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  when the line width is 1  $\mu\text{m}$ , likely due to the large effect of the line sidewalls. The  $V_T$  and  $SS$  are relatively stable at  $9 \pm 0.8 \text{ V}$  and  $1.4 \pm 0.1 \text{ V dec}^{-1}$ , respectively. TFT arrays (100 dpi) were also fabricated with different channel lengths which show uniform device performance (Supplementary Fig. 34). These data demonstrate the realization of very robust semiconductor structures with large surface/volume ratios which should also be suitable for fabricating sensors/TFTs and electrochemical transistors.

Finally, to further validate materials and processing generality, ultraflexible BGTC and TGBC TFT arrays based on patterned 50% DPP/SU8 and 50% N2200/SU8 films, respectively, were fabricated on 1.5  $\mu\text{m}$ -thick parylene substrates. For simplicity of integration, a 300 nm-thick parylene film was also used as the gate dielectric (see parylene dielectric properties in Supplementary Fig. 35). Optical images, device structures, and representative transfer plots of these devices are shown in Fig. 6a–c and Supplementary Fig. 36. The ultraflexible 50% DPP/SU8 and 50% N2200/SU8 devices exhibit an average mobility of  $0.03 \pm 0.01$  and  $0.01 \pm 0.005 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ , respectively. Importantly, negligible mobility/ $V_T$  changes are observed after peeling the devices from

the rigid support and bending them 5000 times at a radius of 1 mm despite microcracks forming in areas surrounding the device (Fig. 6d and Supplementary Fig. 37). Finally, Fig. 6e shows the static switching characteristics and the gain of an ultraflexible inverter based on the p- + n-TFTs. The wide-range switching voltage with a 40 V supply voltage is  $22.2 \pm 0.3 \text{ V}$ , where the high noise margin and low noise margin are  $13.2 \pm 0.2 \text{ V}$  and  $15.6 \pm 0.2 \text{ V}$ , respectively. This inverter exhibits a gain of 11, rivalling or exceeding the performance of other solution-processed flexible devices.<sup>45–48</sup>

## Discussion

We demonstrate a versatile strategy for foundry-compatible high-resolution patterning of organic semiconducting films by cross-linking a vertically phase-separated blend of the semiconducting polymer and a UV photocurable additive (PA). This process is effective for both p- and n-type semiconducting polymers, can use environmentally benign solvents (e.g., THF) under ambient atmosphere, and yields ultraflexible transistor circuitry. GIWAXS, AFM, and TOF-SIMS analyses reveal formation of textured semiconductor film morphologies with a vertically multiphase-separated channel layer preserved during the patterning process. Both PAs promote the formation of close-packed DPP or N2200 nanofiber structures at the bottom of the blend film, which is crucial to achieving functional devices even when only 25 wt% of the semiconductor is added. Equally important, PA addition influences semiconductor polymer backbone orientation, especially for blends with a >50wt % PA content. Excessive PA significantly reduces the edge-on content, thus degrading device performance. Compared with TFTs based on the pristine (unpatterned) polymer semiconductors, the present polymer blend-based patterned devices exhibit optimal transfer/output curves, higher thermal/chemical stability, respectable p-type and n-type TFT performance, and enable the fabrication of ultraflexible TFTs and complementary inverters. Note that the TFT mobilities reported here are not limited by the fabrication



**Fig. 6** Patterned ultraflexible organic p- and n-type transistors. **a** Photo of an ultraflexible DPP/SU8 device array on a 1.5  $\mu\text{m}$  thick parylene substrate. The semiconductor layers are patterned by photolithography while the S/D electrodes are patterned with metal mask. Transfer curves of ultraflexible. **b** BGTC 50% DPP/SU8 devices and **c** BCTG 50% N2200/SU8 devices before and after bending at a radius of 1 mm for the indicated repetitions. The  $V_{\text{DS}}$  is 40 V. **d** Mobility variations of ultraflexible 50% DPP/SU8 and 50% N2200/SU8 devices after bending at a 1 mm radius for the indicated repetitions. **e** Static switching characteristics and gain of an inverter based on ultraflexible 50% DPP/SU8 and 50% N2200/SU8 devices. The supply voltage is set at 40 V.

methodology, which should be readily applicable to current generation semiconducting polymers.<sup>49–52</sup> A possible limitation of the present patterning method relying on VPS is the limited charge transport along the vertical direction since the PA-rich layer is required to protect the underlying semiconducting polymer layer during photolithography. Thus the addressable patterning of high-performance vertical devices, such as organic photovoltaic devices, photodetectors and light-emitting diodes, may be more challenging. Solution-processed organic electronics, especially those enabled by printing technologies, are on the verge of large-scale industrialization. Thus, we can envision that the continuous development of high-performance semiconductors compatible with environmentally benign solvents, together with the present patterning methodology, will facilitate the industrialization of solution-processed organic electronics.<sup>53,54</sup>

## Methods

**Materials.** Poly[2,5-bis(2-octyldodecyl)-3,6-diketopyrrolopyrrole-alt-5,5'-(2,5-di(thien-2-yl)thieno[3,2-*b*]thiophene)] (abbreviated as DPP) was purchased from 1-Material Inc.. Poly[[*N,N*-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene)](P(NDI2OD-T2)), N2200) was provided by Flexterra Inc.. Trichloro(octyl)silane (OTS), polymethyl methacrylate (PMMA, average  $M_w \sim 120$  kg/mol), 2-butanol, acetone, Tetrahydrofuran and anhydrous chloroform were purchased from Sigma-Aldrich. Microposit<sup>TM</sup> S1813<sup>TM</sup> photoresist, SU-8 2000.5 photoresist, SU-8 2002 photoresist, and SU8 developer were purchased from Kayaku Advanced Materials, Inc. (formerly MicroChem Corp.). AZ<sup>®</sup> 400 K developer and hexamethyldisilazane (HDMS) adhesion promoter were purchased from Microchemicals GmbH. The 300 nm-thick SiO<sub>2</sub>/Si substrates and Corning<sup>®</sup> glass substrates were purchased from University Wafer Inc. and Ted Pella Inc., respectively.

**Synthesis of PCell.** PCell was synthesized according to our previously published procedure.<sup>19</sup> Specifically, a suspension of 1.0 g of cellulose in 40 mL of *N,N*-dimethylacetamide was kept at 130 °C for 2 h under stirring. After the slurry was allowed to cool to 100 °C, 3.0 g of anhydrous lithium chloride was added. The cellulose was completely dissolved as the solution was cooled to room temperature under stirring. Next, the cellulose solution was put into an ice bath for 15 min, followed by adding 3.2 g of cinnamoyl chloride. The reaction mixture was heated at

80 °C for 24 h before pouring into an excess volume of ethanol (100 mL). The precipitate was collected by filtration and then it was extracted with ethanol in a Soxhlet extractor for 12 h. Finally, we obtained the dried PCell with a yield of 84.3% after drying under vacuum at 50 °C.

**Preparation of solutions and substrates.** Exactly 8 mg of DPP, 8 mg of N2200, and 8 mg of cinnamate-functionalized PCell were separately dissolved in 2 mL of chloroform. Next, 50  $\mu\text{L}$  SU-8 2000.5 photoresist was diluted with 1.89 mL of chloroform to form a 4 mg/mL solution. All the solutions were stirred overnight at 50 °C in a glovebox. PMMA/2-butanol solutions were prepared by dissolving 70 mg of PMMA in 1.0 mL of 2-butanol and stirring it at 60 °C for 3 h. With regard to the preparation of OTS-treated SiO<sub>2</sub>/Si substrates, 200 mL of OTS was dissolved in a 100 mL mixed solvent of chloroform and hexane with a volume ratio of 3:7. The clean SiO<sub>2</sub>/Si substrates were first treated with an O<sub>2</sub> plasma for 5 min and then immersed in the above OTS solution for 3 h. Clean Corning<sup>®</sup> glass substrates were used for top-gated N2200-based devices without additional cleaning.

**Fabrication of DPP and DPP/SU8 films.** Approximately 1 h before device fabrication, the DPP/chloroform and SU8/chloroform solutions were mixed in a volume ratio of 1:3, 1:1, and 3:1, for fabricating the 25%, 50%, and 75% DPP/SU8 blends, respectively. The mixed solution was spin-coated on OTS-treated SiO<sub>2</sub>/Si substrates at 1500 rpm for 30 s in ambient (RH $\sim$ 30%). After prebaking at 95 °C for 1 min, the films were exposed to 365 nm UV light (F300S, Inpro Technologies, dosage = 60–80 mJ cm<sup>-2</sup>) through a photomask, followed by annealing at 95 °C for 2 min. For high-resolution patterning, maskless aligner (Heidelberg MLA150) equipped with 375 nm laser light was used. Next, the resulting cured films were developed in chloroform for 5 s to achieve the desired patterns. After that, the films were annealed at 150 °C for 30 min in a glovebox. The final film thickness is 40–70 nm depending on the DPP/SU8 ratio. DPP films were prepared by spin-coating of DPP/CHCl<sub>3</sub> solutions at 1500 rpm for 30 s in ambient (RH $\sim$ 30%), followed by thermal annealing at 150 °C for 30 min in a glovebox. The film thickness of DPP film is  $\sim$ 120 nm. Note here the use of low boiling point (<120 °C) solvent is critical for complete VPS, and protecting the underlying polymer semiconductors during photolithography. Other high boiling point solvents such as chlorobenzene, dichlorobenzene, which were generally used in previous reports on semiconductor/insulating polymer blends, are unsuccessful for efficient patterning.<sup>20–26</sup>

**Fabrication of DPP/PCell films.** About 1 h before device fabrication, DPP/chloroform solution and PCell/chloroform solution were mixed with a volume ratio of 1:3, 1:1, and 3:1 for fabricating the 25%, 50%, and 75% DPP/PCell blends, respectively. The mixed solution was spin-coated on OTS-treated SiO<sub>2</sub>/Si substrates



at 1500 rpm for 30 s in ambient (RH~30%). After prebaking at 120 °C for 1 min, the films were exposed to 365 nm UV light (dose = 60–80 mJ cm<sup>-2</sup>) through a photomask, followed by annealing at 120 °C for 5 min. For high-resolution patterning, maskless aligner (Heidelberg MLA150) equipped with 375 nm laser light was used. Next, the resulting cured films were developed in chloroform for 5 s to achieve desired patterns. After that, the films were annealed at 150 °C for 30 min in a glovebox. The final film thickness is 40–70 nm depending on the DPP/PCell ratio.

**Deposition and patterning of gold electrodes.** For OTFTs with large channel size ( $W/L = 1000/100 \mu\text{m}$ ), gold electrode patterns (30 nm thick) were achieved by thermal evaporation underneath semiconductor blend films through a metal mask. For OTFTs with small channel sizes ( $W = 20\text{--}200 \mu\text{m}$   $L = 1\text{--}20 \mu\text{m}$ ), a MCC Primer 80/20 layer (from MicroChem) was first spin-coated on semiconductor layer, followed by 100 °C/annealing for 60 s. S1813 photoresist was then spin-coated at 4000 rpm for 60 s and thermal annealed at 115 °C for 60 s. After that, the resulting films were exposed to 365 nm UV light (dose = 150 mJ cm<sup>-2</sup>) through a photomask and developed in AZ<sup>®</sup> 400 K/H<sub>2</sub>O ( $v/v = 1/4$ ) developer. For high-resolution patterning, maskless aligner (Heidelberg MLA150) equipped with 375 nm laser light was used. Finally, 30 nm-thick gold films were thermally evaporated on the films and the source/drain patterns were achieved by stripping in acetone. For DPP-based devices with TGBC structures, PMMA is used as dielectric layer (see below for details).

**Fabrication of TGBC N2200 and N2200/SU8 devices.** About 1 h before device fabrication, N2200/chloroform solutions and SU8/chloroform solutions were mixed in volume ratios of 1:3, 1:1, and 3:1 for fabricating the 25%, 50%, and 75% N2200/SU8 blends, respectively. Cr/Au source/drain electrodes (2/23 nm thick) on glass substrates were first thermally evaporated through a metal mask. The mixed solution was spin-coated on the above substrates at 1500 rpm for 30 s in ambient (RH ~ 30%). After prebaking at 95 °C for 1 min, the films were exposed to 365 nm UV light (dose = 60–80 mJ cm<sup>-2</sup>) through a photomask, followed by annealing at 95 °C for 2 min. For high-resolution patterning, maskless aligner (Heidelberg MLA150) equipped with 375 nm laser light was used. Next, the resulting cured films were developed with SU8 developer for 5 s to achieve the desired patterns. After that, the films were annealed at 150 °C for 30 min in a glovebox. The final film thickness is 40–50 nm depending on the N2200/SU8 ratio. Pure N2200 films were also spin-coated at 1500 rpm for 30 s in ambient (RH~30%), followed by thermal annealing at 150 °C for 30 min in a glovebox. The film thickness of N2200 film is ~25 nm. Regarding the gate dielectric layer, a PMMA/2-butanol solution was spin-coated on the N2200 or N2200/SU8 films at 1500 rpm for 60 s in a glovebox, followed by 80 °C/3 h annealing. Finally, the gate electrodes were thermally evaporated through a metal mask to obtain bottom-contact top-gate OTFTs. Regarding the use of the green solvent tetrahydrofuran (THF), the fabrication method is identical to above procedure except that the solvent is replaced with THF and SU8 developer is diluted with IPA (SU8 developer: IPA = 7:3 in vol).

**Fabrication of TGBC N2200/PCell devices.** About 1 h before device fabrication, N2200/chloroform solution and PCell/chloroform solution were mixed in volume ratios of 1:3, 1:1, and 3:1 for fabricating the 25%, 50%, and 75% N2200/PCell blends, respectively. Cr/Au source/drain electrodes (2/23 nm thick) on glass substrates were first thermally evaporated through a metal mask. The mixed solution was spin-coated on above substrates at 1500 rpm for 30 s in ambient (RH~30%). After prebaking at 120 °C for 1 min, the films were exposed to 365 nm UV light (dose = 60–80 mJ cm<sup>-2</sup>) through a photomask, followed by annealing at 120 °C for 5 min. For high-resolution patterning, maskless aligner (Heidelberg MLA150) equipped with 375 nm laser light was used. Next, the resulting cured films were developed in SU8 developer for 5 s to achieve the desired patterns. After that, the films were annealed at 150 °C for 30 min in a glovebox. The final film thickness is 40–50 nm depending on the N2200/SU8 ratio. PMMA dielectric and top gate electrodes were deposited by following the above procedure.

**Fabrication of ultraflexible BGTC DPP/SU8 BGTC devices.** A fluorinated polymer solution [Novec 1700 and 7100 ( $v/v = 1:7$ ), 3 M] was spin-coated on solvent-cleaned glass substrates, serving as a delamination layer, and next a 2  $\mu\text{m}$ -thick parylene film was deposited with an SCS Labcoter<sup>®</sup> 2 (PDS2010) deposition system. Next, 50 nm-thick bottom-gate electrodes were thermally evaporated through a metal mask, followed by deposition of a 300 nm-thick parylene film as the gate dielectric layer. After that, patterned 50% DPP/SU8 films and S/D electrodes ( $W/L = 1000/100 \mu\text{m}$ ) were deposited following the procedure used for the rigid devices. Finally, the entire device arrays were delaminated from the glass/fluorinated polymer carrier prior to electrical measurements and bendability tests.

**Fabrication of ultraflexible TGBC N2200/SU8 TGBC devices.** A fluorinated polymer solution [Novec 1700 and 7100 ( $v/v = 1:7$ ), 3 M Company] was spin-coated on solvent-cleaned glass substrates, serving as a delamination layer, next a 1.5  $\mu\text{m}$ -thick parylene film was deposited with an SCS Labcoter<sup>®</sup> 2 (PDS2010)

deposition system. Cr/Au source/drain electrodes (2/23 nm-thick) on glass substrates were thermally evaporated and defined by photolithography as described above. The W/L is 1000/50  $\mu\text{m}$ . After that, patterned 50% N2200/SU8 films were deposited following the procedure used for the rigid devices, followed by evaporation of a 300-nm-thick parylene film as a dielectric layer. The devices were finished by depositing 50-nm-thick top-gate Au electrodes. Finally, the entire device arrays were delaminated from the glass/fluorinated polymer carrier prior to electrical measurements and bendability tests.

**Film and device characterization.** Film morphologies were measured with a Bruker Dimensional Icon AFM system in the tapping mode. To acquire the bottom semiconductor morphologies, the spin-coated films (DPP/SU8, DPP/PCell, N2200/SU8 and N2200/PCell) were immersed in SU8 developer for 5 s and then rinsed with IPA; thus SU8 or PCell can be selectively removed. Optical images were taken using a Nikon Eclipse E200 microscope and film thickness is measured by a Dektak 150 surface profilometer (Veeco Instruments, Inc.). GIWAXS measurements were performed at Beamline 8ID-E at the Advanced Photon Source (APS) at Argonne National Laboratory. Samples were irradiated with a 10.9 keV X-ray at an incidence angle 0.13°–0.15° in vacuum for two summed exposures of 2.5 s (totaling 5 s of exposure), and scattering X-rays were recorded by a Pilatus 1 M detector located 228.16 mm from the sample. The collected images were then processed by using the GIXSGUI software. The background was subtracted by fitting the curves to an exponential decay, and peaks were fitted to an intermediate Lorentzian. The peak width and positions were used to calculate the correlation length and layer spacing. The coherence length was calculated using a modified Scherrer analysis which accounts for instrument resolution using the standard shape factor ( $K = 0.866$  for lamellar polymer aggregates. For DPP-based films, the second order reflection ( $\sim 0.62 \text{ \AA}^{-1}$ ) in the out-of-plane plot is chosen for calculation of coherence length as the first-reflection is obviously affected by beam signal and the 3rd/4th order reflections are relatively weak. The electrical measurements on the dielectrics, OTFTs, and inverters were performed under ambient condition using an Agilent B1500A semiconductor parameter analyzer. The carrier mobility ( $\mu$ ) was evaluated in the saturation region. The areal capacitance for 300 nm SiO<sub>2</sub>/Si is 10.5 nF cm<sup>-2</sup> here, while the areal capacitances of the parylene dielectric is calculated to be 8.6 nF cm<sup>-2</sup>. To test the chemical stability of 50% DPP/SU8 films, OTFTs based on DPP and patterned 50% DPP/SU8 films on 300 nm SiO<sub>2</sub>/Si substrates were immersed in CHCl<sub>3</sub> for 10 s, then the devices were annealed at 100 °C for 1 min in ambient before testing to remove the remaining solvent inside the films. After that, the procedure of immersing, annealing and testing was repeated for several times until the total immersing time reached 24 h. To test the thermal stability, the DPP and 50% DPP/SU8 devices were put on a hotplate. The devices were tested when the temperature increased to the desired set point.

## Data availability

The authors declare that all the data supporting the finding of this study are available from the corresponding authors on reasonable request.

Received: 16 January 2021; Accepted: 16 July 2021;

Published online: 16 August 2021

## References

1. Park, H. W. et al. Universal route to impart orthogonality to polymer semiconductors for sub-micrometer tandem electronics. *Adv. Mater.* **31**, e1901400 (2019).
2. Noh, Y. Y., Zhao, N., Caironi, M. & Sirringhaus, H. Downscaling of self-aligned, all-printed polymer thin-film transistors. *Nat. Nanotechnol.* **2**, 784–789 (2007).
3. Park, S. et al. Large-area formation of self-aligned crystalline domains of organic semiconductors on transistor channels using CONNECT. *Proc. Natl Acad. Sci. USA* **112**, 5561–5566 (2015).
4. Jacobs, I. E. et al. Direct-write optical patterning of P3HT films beyond the diffraction limit. *Adv. Mater.* **29**, 1603221 (2017).
5. Kim, M. J. et al. Universal three-dimensional crosslinker for all-photopatterned electronics. *Nat. Commun.* **11**, 1520 (2020).
6. Zhao, X. et al. High-performance full-photolithographic top-contact conformable organic transistors for soft electronics. *Adv. Sci.* **8**, 2004050 (2021).
7. Li, Q.-F., Liu, S., Chen, H.-Z. & Li, H.-Y. Alignment and patterning of organic single crystals for field-effect transistors. *Chin. Chem. Lett.* **27**, 1421–1428 (2016).
8. Zakhidov, A. A. et al. Orthogonal processing: A new strategy for organic electronics. *Chemical Science* **2**, 1178–1182 (2011).

9. Zhu, H. et al. Printable semiconductors for backplane TFTs of flexible OLED displays. *Adv. Funct. Mater.* **30**, 1904588 (2020).
10. Sirringhaus, H. 25th anniversary article: organic field-effect transistors: the path beyond amorphous silicon. *Adv. Mater.* **26**, 1319–1335 (2014).
11. Fahlman, M. et al. Interfaces in organic electronics. *Nat. Rev. Mater.* **4**, 627–650 (2019).
12. Su, Z. et al. High-speed photothermal patterning of doped polymer films. *ACS Appl. Mater. Interfaces* **11**, 41717–41725 (2019).
13. Png, R. Q. et al. High-performance polymer semiconducting heterostructure devices by nitrene-mediated photocrosslinking of alkyl side chains. *Nat. Mater.* **9**, 152–158 (2010).
14. Kim, H. J. et al. Solvent-resistant organic transistors and thermally stable organic photovoltaics based on cross-linkable conjugated polymers. *Chem. Mater.* **24**, 215–221 (2011).
15. Lu, K. et al. Novel functionalized conjugated polythiophene with oxetane substituents: synthesis, optical, electrochemical, and field-effect properties. *Macromolecules* **42**, 3222–3226 (2009).
16. Qiu, L. et al. Organic thin-film transistors with a photo-patternable semiconducting polymer blend. *J. Mater. Chem.* **21**, 15637–15642 (2011).
17. Liu, S., Al-Shadeedi, A., Kaphle, V., Keum, C.-M. & Lüssem, B. Patterning organic transistors by dry-etching: the double layer lithography. *Org. Electron.* **45**, 124–130 (2017).
18. Shin, J. et al. Electrical transport characteristics of chemically robust PDPP-DTT embedded in a bridged silsesquioxane network. *J. Mater. Chem. C*, 14889–14896 (2019).
19. Wang, Z. et al. Cinnamate-functionalized natural carbohydrates as photopatternable gate dielectrics for organic transistors. *Chem. Mater.* **31**, 7608–7617 (2019).
20. Zhang, G. et al. Robust and stretchable polymer semiconducting networks: from film microstructure to macroscopic device performance. *Chem. Mater.* **31**, 6530–6539 (2019).
21. Nikzad, S. et al. Inducing molecular aggregation of polymer semiconductors in a secondary insulating polymer matrix to enhance charge transport. *Chem. Mater.* **32**, 897–905 (2020).
22. Goffri, S. et al. Multicomponent semiconducting polymer systems with low crystallization-induced percolation threshold. *Nat. Mater.* **5**, 950–956 (2006).
23. Hamilton, R. et al. High-performance polymer-small molecule blend organic transistors. *Adv. Mater.* **21**, 1166–1171 (2009).
24. Xu, J. et al. Highly stretchable polymer semiconductor films through the nanoconfinement effect. *Science* **355**, 59–64 (2017).
25. Riera-Galindo, S., Leonardi, F., Pfaltner, R. & Mas-Torrent, M. Organic semiconductor/polymer blend films for organic field-effect transistors. *Adv. Mater. Technol.* **4**, 1900104 (2019).
26. Smith, J. et al. Solution-processed small molecule-polymer blend organic thin-film transistors with hole mobility greater than 5 cm<sup>2</sup>/Vs. *Adv. Mater.* **24**, 2441–2446 (2012).
27. Li, J. et al. A stable solution-processed polymer semiconductor with record high-mobility for printed transistors. *Sci. Rep.* **2**, 754 (2012).
28. Lei, Y. L. et al. Hydrocarbons-driven crystallization of polymer semiconductors for low-temperature fabrication of high-performance organic field-effect transistors. *Adv. Funct. Mater.* **28**, 1706372 (2018).
29. Xi, Y., Wolf, C. M. & Pozzo, L. D. Self-assembly of donor-acceptor conjugated polymers induced by miscible ‘poor’ solvents. *Soft. Matter*, **15**, 1799–1812 (2019).
30. Li, M. et al. Controlling the microstructure of conjugated polymers in high-mobility monolayer transistors via the dissolution temperature. *Angew. Chem. Int. Ed. Engl.* **59**, 846–852 (2020).
31. Smilgies, D. M. Scherrer grain-size analysis adapted to grazing-incidence scattering with area detectors. *J. Appl. Crystallogr.* **42**, 1030–1034 (2009).
32. Lei, Y., Li, N., Chan, W.-K. E., Ong, B. S. & Zhu, F. Highly sensitive near infrared organic phototransistors based on conjugated polymer nanowire networks. *Org. Electron.* **48**, 12–18 (2017).
33. Zhang, G. et al. Versatile interpenetrating polymer network approach to robust stretchable electronic devices. *Chem. Mater.* **29**, 7645–7652 (2017).
34. Shin, N., Zessin, J., Lee, M. H., Hamsch, M. & Mannsfeld, S. C. B. Enhancement of n-type organic field-effect transistor performances through surface doping with aminosilanes. *Adv. Funct. Mater.* **28**, 1802265 (2018).
35. Lei, Y. et al. Solution-processed donor-acceptor polymer nanowire network semiconductors for high-performance field-effect transistors. *Sci. Rep.* **6**, 24476 (2016).
36. Wang, G. et al. Mixed-flow design for microfluidic printing of two-component polymer semiconductor systems. *Proc. Natl. Acad. Sci. USA* **117**, 17551–17557 (2020).
37. Zhang, X. et al. Breath figure-derived porous semiconducting films for organic electronics. *Sci. Adv.* **6**, eaaz1042 (2020).
38. Gann, E., Caironi, M., Noh, Y.-Y., Kim, Y.-H. & McNeill, C. R. Diffractive X-ray waveguiding reveals orthogonal crystalline stratification in conjugated polymer thin films. *Macromolecules* **51**, 2979–2987 (2018).
39. Liu, S. et al. Direct patterning of organic-thin-film-transistor arrays via a “dry-taping” approach. *Adv. Mater.* **21**, 1266–1270 (2009).
40. Dickey, K. C. et al. Large-area patterning of a solution-processable organic semiconductor to reduce parasitic leakage and off currents in thin-film transistors. *Appl. Phys. Lett.* **90**, 244103 (2007).
41. Choi, H. H., Cho, K., Frisbie, C. D., Sirringhaus, H. & Podzorov, V. Critical assessment of charge mobility extraction in FETs. *Nat. Mater.* **17**, 2–7 (2018).
42. Bittle, E. G., Basham, J. I., Jackson, T. N., Jurchescu, O. D. & Gundlach, D. J. Mobility overestimation due to gated contacts in organic field-effect transistors. *Nat. Commun.* **7**, 10908 (2016).
43. Luzio, A., Criante, L., D’Innocenzo, V. & Caironi, M. Control of charge transport in a semiconducting copolymer by solvent-induced long-range order. *Sci. Rep.* **3**, 3425 (2013).
44. Gumyusenge, A. et al. Semiconducting polymer blends that exhibit stable charge transport at high temperatures. *Science* **362**, 1131–1134 (2018).
45. Huang, K.-M. et al. 2-V operated flexible vertical organic transistor with good air stability and bias stress reliability. *Org. Electron.* **50**, 325–330 (2017).
46. Takeda, Y. et al. Organic complementary inverter circuits fabricated with reverse offset printing. *Adv. Electron. Mater.* **4**, 1700313 (2018).
47. Shiwaku, R. et al. Printed organic inverter circuits with ultralow operating voltages. *Adv. Electron. Mater.* **3**, 1600557 (2017).
48. Ji, D. et al. Copolymer dielectrics with balanced chain-packing density and surface polarity for high-performance flexible organic electronics. *Nat. Commun.* **9**, 2339 (2018).
49. Wang, Z. et al. Charge mobility enhancement for conjugated DPP-selenophene polymer by simply replacing one bulky branching alkyl chain with linear one at each DPP unit. *Chem. Mater.* **30**, 3090–3100 (2018).
50. Yang, J., Zhao, Z., Wang, S., Guo, Y. & Liu, Y. Insight into high-performance conjugated polymers for organic field-effect transistors. *Chem* **4**, 2748–2785 (2018).
51. Kang, I., Yun, H. J., Chung, D. S., Kwon, S. K. & Kim, Y. H. Record high hole mobility in polymer semiconductors via side-chain engineering. *J. Am. Chem. Soc.* **135**, 14896–14899 (2013).
52. Back, J. Y. et al. Investigation of structure–property relationships in diketopyrrolopyrrole-based polymer semiconductors via side-chain engineering. *Chem. Mater.* **27**, 1732–1739 (2015).
53. Ho, D. et al. Green solvents for organic thin-film transistor processing. *J. Mater. Chem. C*, **8**, 5786–5794 (2020).
54. Campana, F., Kim, C., Marrocchi, A. & Vaccaro, L. Green solvent-processed organic electronic devices. *J. Mater. Chem. C*, **8**, 15027–15047 (2020).

## Acknowledgements

We thank AFOSR (FA9550-18-1-0331), the Northwestern U. MRSEC (NSF DMR-1720139), the US Department of Commerce, National Institute of Standards and Technology as part of the Center for Hierarchical Materials Design Award 70NANB10H005, and the Department of Energy under contract no. DE-AC02-05CH11231, at beamline 8-ID-E of the Advanced Photon Source, a U.S. Department of Energy (DOE) Office of Science User Facility operated for the DOE Office of Science by Argonne National Laboratory under Contract No. DE-AC02-06CH11357, the Japan Science and Technology Agency Exploratory Research for Advanced Technology Someya Bio-Harmonized Electronics Project, Japan Society for the Promotion of Science KAKENHI (Grant 17H06149), and Flexterra Corp. for support of this research. B. W. is grateful to the Southeast University Research Startup Fund (4306002172). This work made use of the Northwestern U. J. B. Cohen X-Ray Diffraction Facility, the EPIC facility, Keck-II facility, and SPID facility of the NUANCE Center at Northwestern U., which received support from the Soft and Hybrid Nanotechnology Experimental (SHyNE) Resource (NSF ECCS-2025633), the Northwestern U. MRSEC (NSF DMR-1720139), and the International Institute for Nanotechnology (IIN).

## Author contributions

B.W. conceived the project and A.F. helped design the experiments. B.W. conducted most of the experiments and drafted the manuscript. W.H. conducted the Tof-SIMS experiment, and L.H. assisted with AFM image collection. Z.W. synthesized the PCell and Z.C. synthesized the N2200. Y.C., L.-W.F., and G.W. helped perform the GIWAXS experiment. S.L. and T.Y. helped fabricate and evaluate the ultraflexible devices. B.W., A. F., T.J.M., S.L., and T.S. co-wrote and revised the manuscript. All authors discussed the results and commented on the manuscript.

**Competing interests**

The authors declare no competing interests.

**Additional information**

**Supplementary information** The online version contains supplementary material available at <https://doi.org/10.1038/s41467-021-25059-8>.

**Correspondence** and requests for materials should be addressed to T.S., T.J.M. or A.F.

**Peer review information** *Nature Communications* thanks Peter Müller-Buschbaum and the other, anonymous, reviewer(s) for their contribution to the peer review of this work.

**Reprints and permission information** is available at <http://www.nature.com/reprints>

**Publisher's note** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.



**Open Access** This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this license, visit <http://creativecommons.org/licenses/by/4.0/>.

© The Author(s) 2021