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Semi-analytical modelling and evaluation of uniformly doped silicene nanotransistors for digital logic gates

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Abstract

Silicene has attracted remarkable attention in the semiconductor research community due to its silicon (Si) nature. It is predicted as one of the most promising candidates for the next generation nanoelectronic devices. In this paper, an efficient non-iterative technique is employed to create the SPICE models for p-type and n-type uniformly doped silicene field-effect transistors (FETs). The current-voltage characteristics show that the proposed silicene FET models exhibit high on-to-off current ratio under ballistic transport. In order to obtain practical digital logic timing diagrams, a parasitic load capacitance, which is dependent on the interconnect length, is attached at the output terminal of the logic circuits. Furthermore, the key circuit performance metrics, including the propagation delay, average power, power-delay product and energy-delay product of the proposed silicene-based logic gates are extracted and benchmarked with published results. The effects of the interconnect length to the propagation delay and average power are also investigated. The results of this work further envisage the uniformly doped silicene as a promising candidate for future nanoelectronic applications.

1. Introduction

Digital logic gates are the foundation of modern computation and information processing in various systems such as nanostructure computers [1,2], photonic technology [3,4] and biomedical engineering [5,6]. The development of these systems is governed by Moore's Law [7,8] for more than four decades. However, the present digital logic gates, primarily based on bulk silicon (Si) field-effect transistors (FETs), are reaching the fundamental device limitations [9,10]. Therefore, the quest for next-generation FETs to leverage nanotechnologies, for more than Moore's applications, has become one of the mainstream research topics.

The development of two-dimensional (2D) materials has been motivated by the success of monolayer honeycomb carbon (C)—graphene [11]. While the discovery of graphene has more than 15 years of history, the honeycomb Si-based monolayer—silicene has only attracted research interest in the recent years as shown by the trend of publication numbers [12,13] despite its potential compatibility with the present Si-dominant fabrication processes. In 2015,

study design, data collection and analysis, decision to publish, or preparation of the manuscript.

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Tao *et al*. [14] demonstrated the first silicene-based transistor using synthesis-transfer fabrication technique. Interestingly, silicene is envisaged as an alternative material for transistor scaling in the International Roadmap for Devices and Systems (IRDS) [15]. Although silicene sheets have successfully been formed on various substrates in their buckled [16–18] and planar [19] forms, the fabrication of stable free-standing silicene still remains a major challenge. At this early stage of development, computational modelling and simulation are very useful in providing fundamental insights of silicene-based devices and circuits.

Silicene, as a counterpart of graphene [20,21], exhibits the Dirac cone properties and in addition, an extremely small energy bandgap of 1.55 *meV* [22]. Similar to graphene, bandgap engineering techniques are required in order to build silicene-based transistors, where the transistors for digital switching applications typically require an energy bandgap of at least 0.4 *eV* [23] to suppress the unwanted subthreshold conduction. Silicene sheets can be sliced into semiconducting silicene nanoribbons (SiNRs) which have shown promising transistor performances [24], but their energy bandgap values and electronic properties are heavily dependent on the nanoribbons widths [25]. Although altering nanoribbon width is proven to be an viable bandgap engineering option, the fabrication technique to produce nanoribbon with perfect edge control is yet to be discovered, even for the well-known and matured graphene [26].

Due to this shortcoming, we propose to employ the n-type and p-type uniformly doped silicene as the semiconducting channel of the silicene-based FETs, by using phosphorus (P) and aluminium (Al) as the dopant atoms, respectively. This uniform doping technique has been proven previously to be an effective way to obtain semiconducting silicene nanosheets, that are suitable for digital switching applications [27]. The silicene sheets that are uniformly doped using P and Al will be denoted as PSi_3 and $AlSi_3$, respectively in the rest of this paper. Unlike the selective doping technique [28,29], where the electronic properties of doped silicene vary with dopant sites, the uniform doping technique is independent on the dopant sites [30]. After obtaining semiconducting silicene nanosheets, these n-type and p-type silicene-based FETs can be employed to build various complementary metal–oxide–semiconductor (CMOS) circuits such as inverter, NAND, and NOR gates.

Despite rigorous efforts to model and simulate silicene-based devices [12,31], there is still minimal work focusing on the circuit-level performance analysis featuring silicene-based transistor. In this paper, the circuit-level performance of n-type and p-type uniformly doped silicene FETs, as shown in **Fig 1**, are assessed by developing a SPICE-compatible model [32]. This circuit-level model is developed by extending our previous works on uniformly doped silicene model at the material-level [33] and device-level [34]. **Section 2** describes the detailed modelling procedures employed in this work. In **Section 3**, the simulation results of the silicene-based logic gates are shown by plotting the timing diagrams. Subsequently, the circuit performance of the logics gates are analysed based on their propagation delay, average power, power-delay product (PDP) and energy-delay product (EDP). Finally, the conclusion of this work is drawn and potential future work is recommended in **Section 4**.

2. Modelling procedures

This section describes the step-by-step modelling procedures for the proposed silicene-based nanotransistors from material-level up to circuit-level, where the overall flow chart is depicted in **Fig 2**.

2.1 Uniformly doped silicene transistors

At the material-level, the electronic properties of p-type ($AlSi_3$) and n-type (PSi_3) nanosheets as shown in **Fig 1**, are modelled using nearest neighbour tight-binding (NNTB) model by

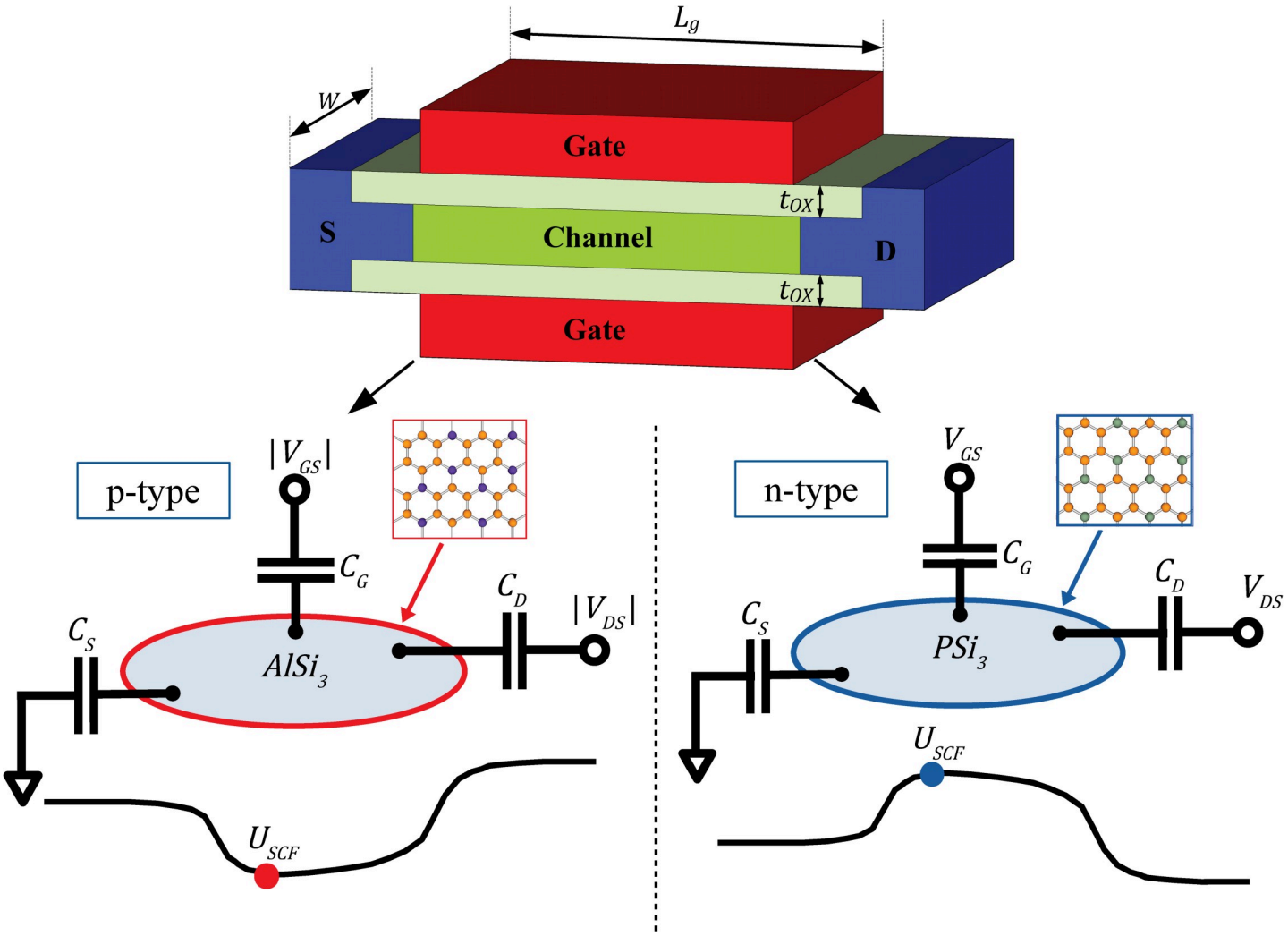

Fig 1. Schematic structure and circuit diagrams of n-type and p-type uniformly doped silicene FETs. Brown atoms represent silicon (Si) atoms; purple atoms represent aluminium (Al) atoms; and grey atoms represent phosphorus (P) atoms.

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fitting the published DFT band structures in **Ref** [27]. The nanosheets are assumed to be in their perfect planar honeycomb lattice. This assumption is applicable because the successful fabrication of planar silicene has recently been reported [19]. Subsequently, the transverse effective masses (in the zigzag direction) of these materials are obtained by using parabolic band approximation. The detailed procedures to obtain the effective masses can be found in **Ref** [33]. Although previous work [33] shows only the modelling procedures for the p-type $AlSi_3$ nanosheet, the same technique is repeated to compute the electronic properties of n-type PSi_3 nanosheet, in order to obtain both type of transistors for CMOS applications. **Table 1** summarises the important electronic properties of the $AlSi_3$ and PSi_3 nanosheets, where m_0 is the constant for electron rest mass. The results show that both uniformly doped silicene nanosheets have achieve energy bandgap values of $0.4\ eV \leq E_g \leq 3.0\ eV$, making them suitable for nanoelectronic digital switching applications [35].

With the obtained electronic properties, the work then proceeds with device-level modelling by employing the top-of-the-barrier (TOB) ballistic nanotransistor model [36], which has been widely used to predict the performance limits of various low-dimensional materials [37].

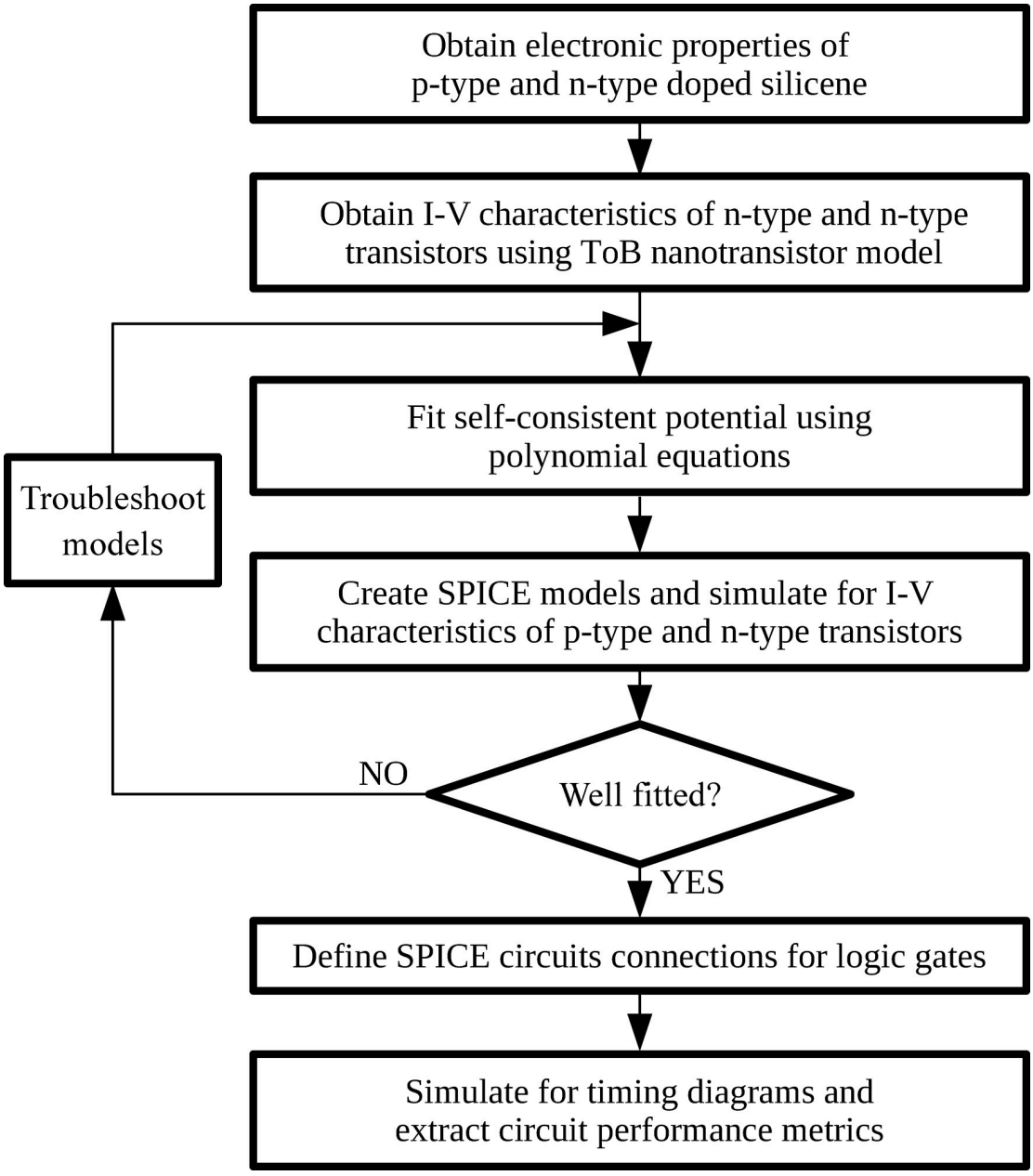

Fig 2. Modelling and simulation flow chart of this work.

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Table 1. Electronic properties of uniformly doped silicene nanosheets.

Parameters	$AlSi_3$	PSi_3
Semiconductor type	p-type	n-type
Energy bandgap, E_g (eV)	0.780	0.660
Electron effective mass, m_e^*	$0.235m_0$	$0.230m_0$
Hole effective mass, m_h^*	$0.255m_0$	$0.240m_0$

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In this work, a double-gated FET structure with $L_g = 10\ nm$ is employed, where the gate oxide layers are SiO_2 ($\varepsilon_r = 3.9$) with thickness of $t_{OX} = 1.5\ nm$. All simulations are done at the room temperature of $T = 300\ K$. For simplification, the W/L_g aspect ratio is set as unity for both type of silicene FETs. The schematic diagrams of the FETs are illustrated in **Fig 1**. In n-type 2D FETs, the current transport primarily depends on the electron mobility via the conduction band, and vice versa for p-type 2D FETs (where the structures of 2D FETs are similar to those of junctionless FETs [38]). Therefore, electron effective mass is used for n-type (PSi_3) FET while hole effective mass is used for p-type ($AlSi_3$) FET.

The self-consistent potentials U_{SCF} in the TOB model are calculated iteratively in MATLAB until the solutions for the charge carriers at the TOB converge. Therefore, further modifications are required to obtain a non-iterative model, in terms of the drain-source voltage V_{DS} and gate-source voltage V_{GS}, to allow cross-platform simulation and reduce computational cost [39]. In order to create a model compatible with the Simulation Program with Integrated Circuit Emphasis (SPICE), the self-consistent potential U_{SCF} in the TOB model is computed through fifth order polynomial equation within the non-linear regression model [40], expressed as

$$U_{SCF}(|V_{GS}|, |V_{DS}|) = P_{ij} \sum_{k=0}^{5} (|V_{GS}| + |V_{DS}|)^k, \tag{1}$$

where P_{ij} is the coefficient for each respective $|VG_S|^i |V_{DS}|^j$ term. The fifth order binomial equation as shown in **Eq (1)** can be expanded via Pascal's triangle rule. The coefficients are extracted and optimised using MATLAB curve fitting tool, where **Fig 3** shows the results of the non-linear regression model. The full equation and coefficients for p-type and n-type uniformly doped silicene is attached in the supplementary data file (**S1 File**). We employed the fifth order binomial equation because the lower order binomial equations are unable to produce decent fit for the U_{SCF} and the fifth order is the highest available within the curve fitting tool.

2.2 Device and circuit simulation

Following that, the current-voltage (I-V) characteristics of n-type and p-type uniformly doped silicene FETs can be obtained in terms of V_{DS} and V_{GS}, by using Landauer-Büttiker ballistic transport equation [36] with Fermi-Dirac integral solution [41], given as

$$|I_{DS}(|V_{GS}|, |V_{DS}|)| = \frac{gW}{\hbar^2} \sqrt{\frac{m_x^* q^2 (k_B T)^3}{2\pi^3}} \{\log[1 + e^{\eta_S(|V_{GS}|,|V_{DS}|)}] - \log[1 + e^{\eta_D(|V_{GS}|,|V_{DS}|)}]\}, \tag{2}$$

with the normalised source and drain energies of

$$\eta_S(|V_{GS}|, |V_{DS}|) = \frac{E_F - U_{SCF}(|V_{GS}|, |V_{DS}|)}{k_B T}, \tag{3}$$

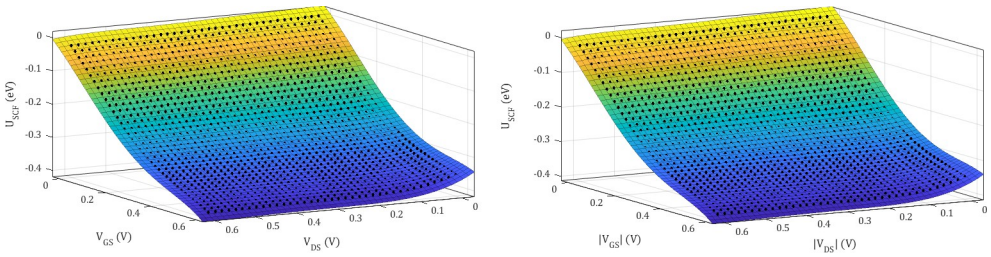

Fig 3. The non-linear regression fit for self-consistent potential: (a) p-type $AlSi_3$ and (b) n-type PSi_3. The dots are U_{SCF} data from ToB model; and the coloured plane is the plot of fifth order polynomial equation.

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and

$$\eta_D(|V_{GS}|,|V_{DS}|) = \frac{E_F - U_{SCF}(|V_{GS}|,|V_{DS}|) - q|V_{DS}|}{k_B T}, \quad (4)$$

where g is the degeneracy factor (set as 2 to include up and down spins); $\hbar$ is the Planck's constant; q is the constant for electric charge; and k_B is the Boltzmann constant.

The magnitude of the supply voltage $|V_{DD}|$ proposed in this work is 0.60 V and the Fermi energy level E_F is adjusted such that the off-current $I_{off} = 100\ nA/\mu m$, for low-standby power (LSTP) CMOS applications [42]. In this work, the original gate control ($\alpha_D = 0.880$) and drain control ($\alpha_D = 0.035$) parameters from **Ref** [36] are employed and the source terminal is always tied to the ground ($V_S = 0\ V$). Eqs (**1**) to (**4**) are used to create the SPICE library files for n-type and p-type uniformly doped silicene FET. With these operating conditions, the n-type and p-type silicene FETs have achieved on-to-off current (I_{on}/I_{off}) ratio of $I_{on}/I_{off} = 2.8\times10^5$ and $I_{on}/I_{off} = 2.6\times10^5$, respectively at room temperature $T = 300\ K$. The n-type silicene FET has higher I_{on}/I_{off} ratio because the electron effective mass of PSi_3 nanosheet is lighter than the hole effective mass of $AlSi_3$. The I_{on}/I_{off} ratio of the proposed device is higher than Si FinFET [43] by two orders. In addition, the I_{on}/I_{off} ratios of the n-type and p-type uniformly doped silicene FETs are improved by 35.7% and 19.2%, respectively, when compared to n-type and p-type Si nanowire FETs (where the I_{on}/I_{off} ratios of n-type and p-type Si nanowire FETs were found to be 1.8×10^5 and 2.1×10^5, respectively in **Ref** [44]). In addition, **Table 2** compares the I_{on}/I_{off} ratios of the proposed model with published 2D material-based FET models. It is shown that the proposed FET models outperform Phosphorene and graphene nanoribbon (GNR) FET models. Although 27-ASiNR FET outperforms the proposed FETs, it still remains a huge challenge to precisely control the size of 2D nanoribbons with specific widths, even for graphene which was discovered in the laboratory more than 15 years ago [26,45].

The simulated I-V characteristics for the original iterative TOB model and non-iterative SPICE model are plotted on the same graph in **Fig 4**. The results show that the fifth order binomial equation for U_{SCF} is capable of reproducing the iterative TOB model in the HSPICE circuit simulator with minimal error. With the p-type and n-type FET SPICE models ready, the work proceeds to build and simulate digital logic circuits using HSPICE simulator. In order to make the circuit simulation more practical, copper (Cu) interconnect capacitance is incorporated as the load capacitance for all circuits. The Cu interconnect capacitance is identified as $C_{int} = 121.3\ aF/\mu m$ by using the ITRS projected interconnect capacitance value for transistor with 10 nm gate length [40]. The length L_{int} of the Cu interconnect is varied from 10 nm to 50 μm to investigate its effects on the logic circuit performance.

3. Results and discussions

In this section, the simulation results of digital logic gates, including inverter, 2-input NAND and 2-input NOR gates are shown. Their circuit performances are also evaluated by extracting

Table 2. Comparison of I_{on}/I_{off} ratio of the proposed model with published 2D material-based FET models.

[Ref]	Channel	L (nm)	Gate oxide	t_{OX} (nm)	I_{on}/I_{off} ratio
This work	PSi_3	10	SiO_2	1.5	2.8×10^5
This work	$AlSi_3$	10	SiO_2	1.5	2.6×10^5
[24]	27-ASiNR	15	-	1.0	2.8×10^6
[42]	Phosphorene	20	ZrO_2	3.0	1.0×10^4
[46]	GNR	10	Mixed	1.5	4.5×10^4

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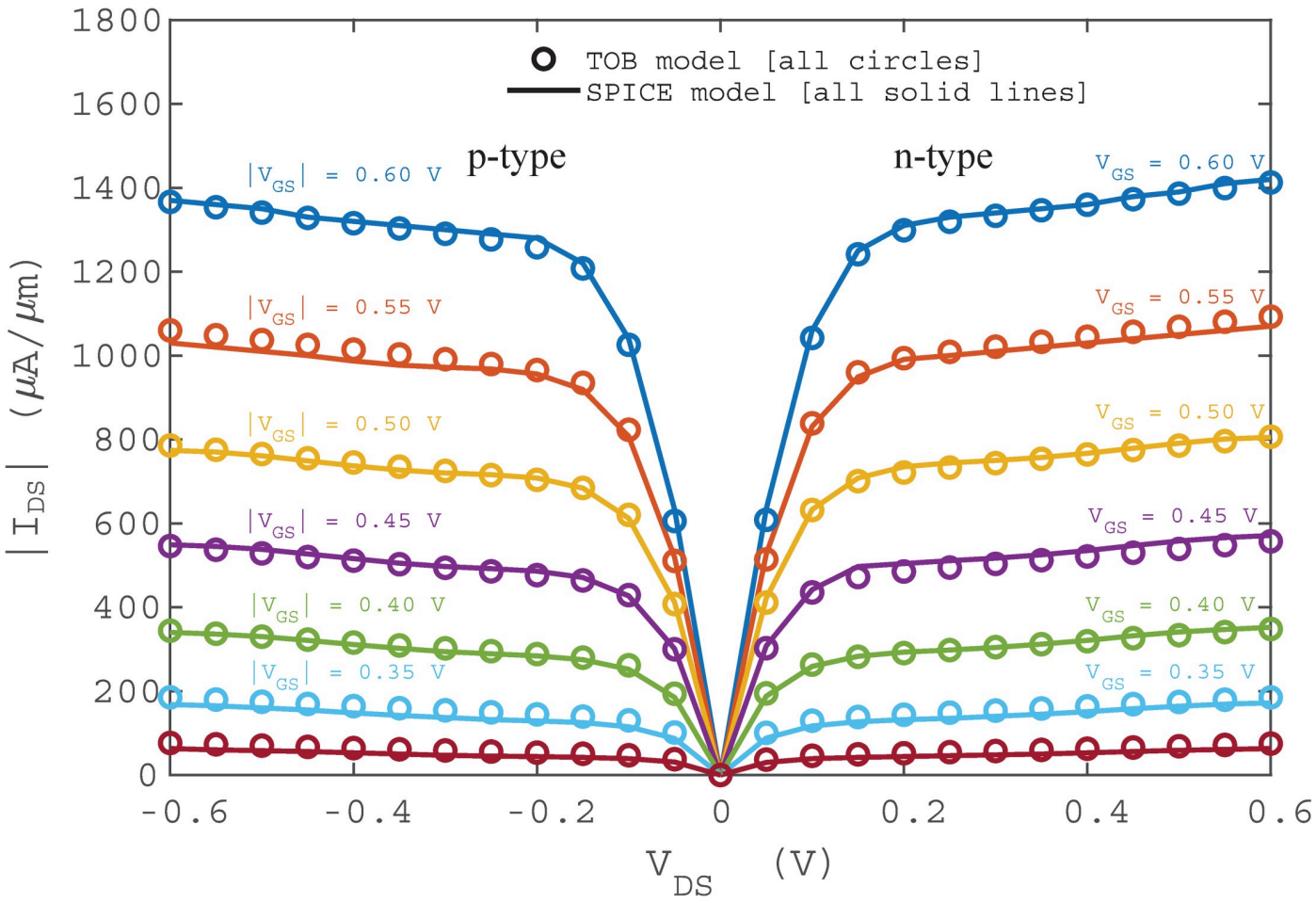

Fig 4. Comparison of I-V characteristics between iterative and non-iterative TOB nanotransistor models.

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the propagation delay (t_p), average power (P_{avg}), PDP and EDP. The propagation delay of the proposed model is also benchmarked with selected published results.

3.1 Timing diagrams

The silicene-based logic circuits simulated in HSPICE are then plotted using Avanwaves. The high voltage (representing '1' digital signal) of the input pulses are set to the supply voltage of 0.60 *V*; and low voltage (representing '0' digital signal) of the input pulses are set to the ground voltage of 0 *V*. A rise and fall time of $t_r = t_f = 0.1$ *ps* are used for the input waveforms in order to obtain sharp rising and falling edges. **Figs** 5–7 clearly show that the silicene-based logic circuits are able to function correctly according to the intended Boolean logics for inverter, 2-input NAND and 2-input NOR gates [47], respectively.

3.2 Performance analysis of digital logic circuits

The propagation delay (t_p) and average power (P_{avg}) for the simulated logic gates are extracted and plotted against the length L_{int} of Cu interconnect, as depicted in **Fig 8**. It is clearly shown that the t_p for all three logic gates increases as the L_{int} increases. Nevertheless, the 2-input NAND gate has the highest t_p for all interconnect lengths. On the other hand, the P_{avg} for all

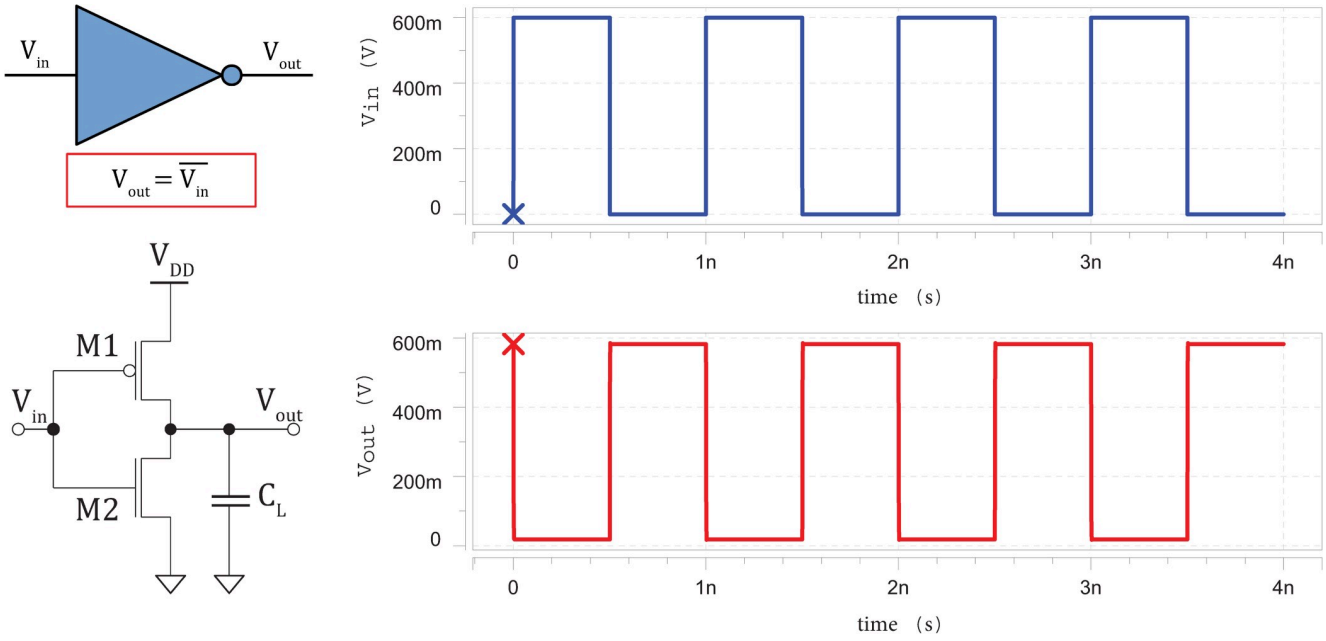

Fig 5. Schematic circuit diagram of silicene-based inverter (L_{int} = 1 μm) with its input (blue) and corresponding output waveforms (red).

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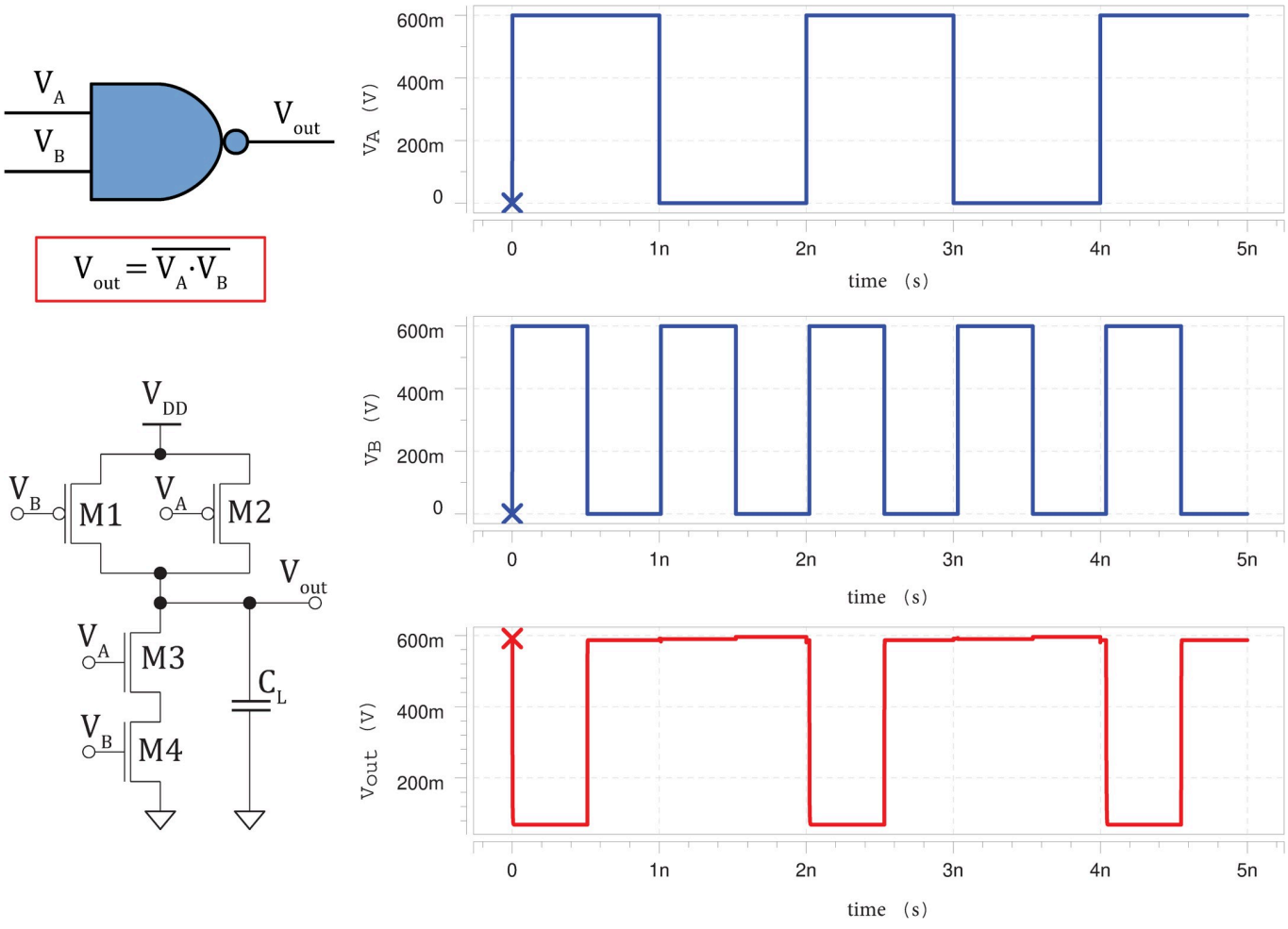

Fig 6. Schematic circuit diagram of silicene-based 2-input NAND gate (L_{int} = 1 μm) with its input (blue) and corresponding output waveforms (red).

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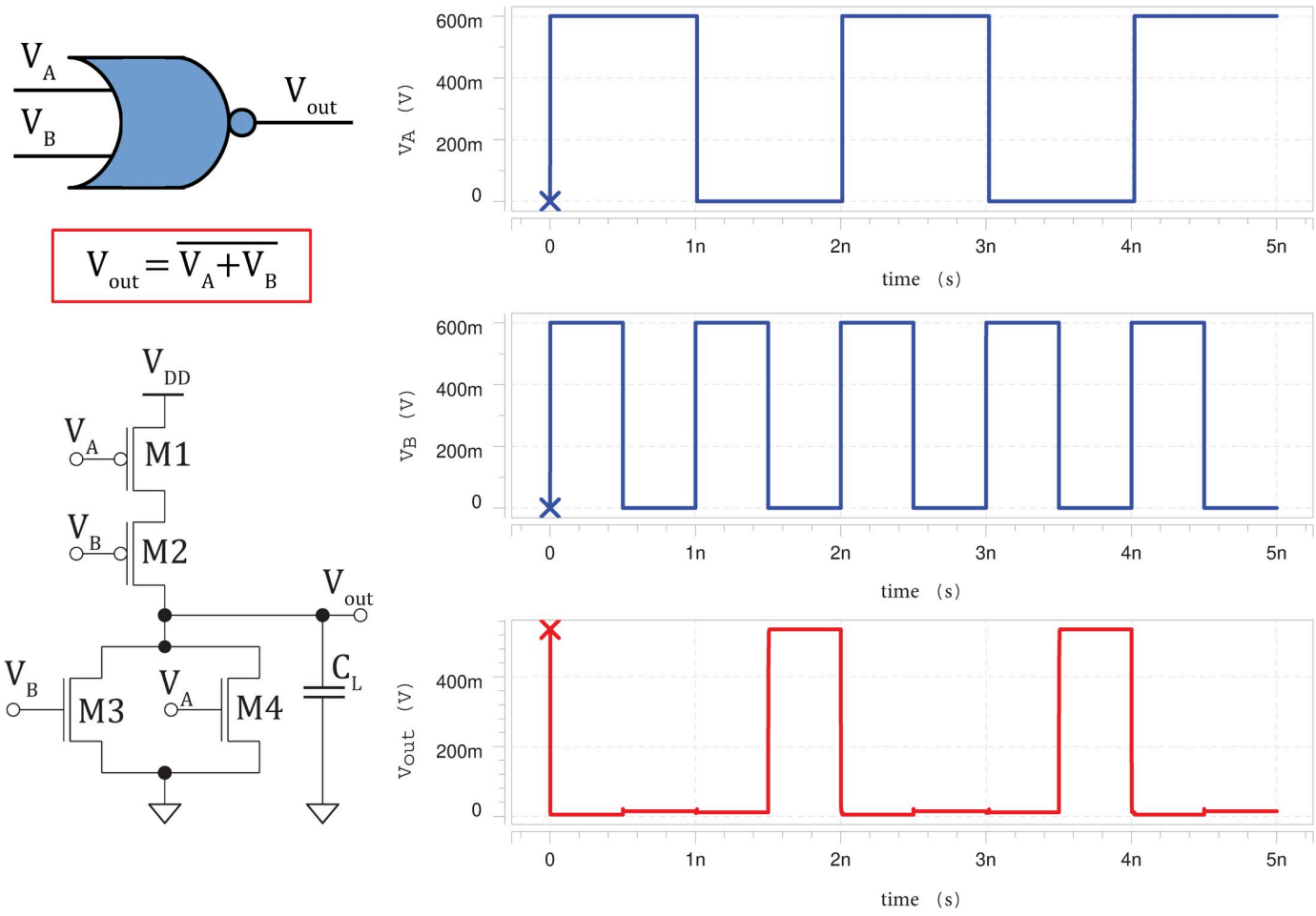

Fig 7. Schematic circuit diagram of silicene-based 2-input NOR gate (L_{int} = 1 μm) with its input (blue) and corresponding output waveforms (red).

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three logic gates remain almost constant until L_{int} = 1 μm, regardless of the type of logic gates. Thus, it is crucial to optimise the L_{int} in digital system design in order to achieve minimal propagation delay and suppress the power consumption. Similar circuit degradation due to long L_{int} was also previously reported for GNR FETs with interconnect analysis [40].

Subsequently, the figure of merits for digital logic circuits are calculated using the extracted values in Fig 8 and the equations of the PDP and EDP [47], given as

$$PDP = P_{avg} \times t_p, \tag{5}$$

and

$$EDP = PDP \times t_p, \tag{6}$$

where the average power P_{avg} and propagation delay t_p. Fig 9 shows the PDP and EDP of proposed silicene-based digital logic circuits when L_{int} is varied from 10 nm to 50 μm. The 3D plot in Fig 9(b) show that, at all values of L_{int}, 2-input NAND gate has the highest EDP due to its high propagation delay t_p compared to inverter and 2-input NOR gates.

As this study aims to assess the circuit-level performance of the proposed uniformly doped silicene FETs for digital logic gates, the results are benchmarked with published works that are based on low-dimensional materials, including GNR FET and 7 nm FinFET from **Ref** [48]; as

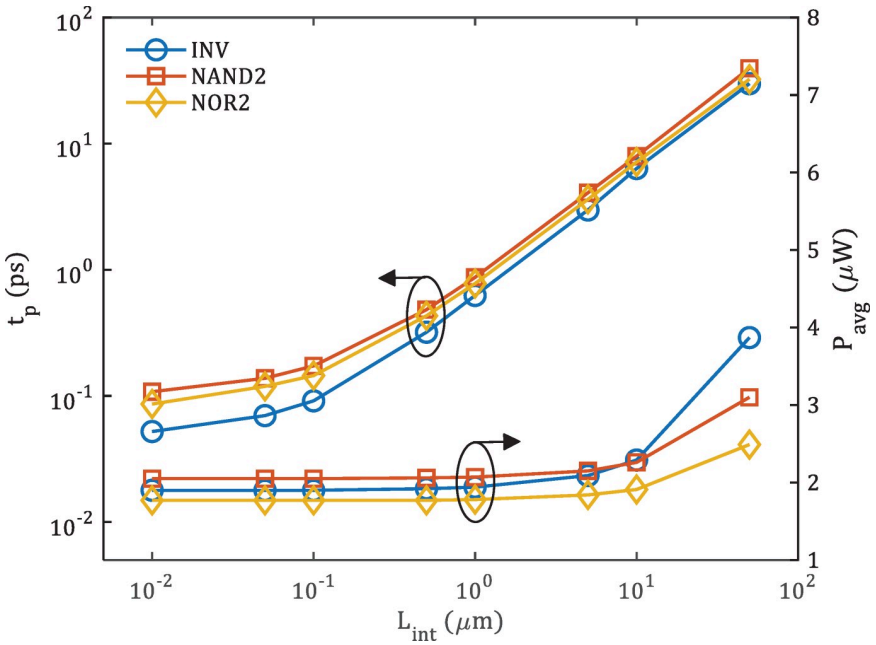

Fig 8. Propagation delay (t_p) and average power (P_{avg}) of silicene-based digital logic circuits with varying interconnect length (L_{int}). INV, NAND2 and NOR2 represent inverter, 2-input NAND and 2-input NOR gates, respectively.

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well as 10 *nm* carbon nanotube (CNT) FET and 10 *nm* FinFET from **Ref** [49]. Due to the unavailability of complete data, we have only compared the propagation delay t_p among the models for inverter and 2-input NAND gates as shown in **Fig 10**. The bar graph clearly shows that the proposed silicene-based inverter gate outperforms all the published models in terms of the propagation delay. However, the propagation delay of proposed silicene-based 2-input NAND gate is higher than that of the graphene-based logic circuit [48]. Despite this slight disadvantage, silicene-based circuits are still a prospective choice for the future nanoelectronic applications due to its potential compatibility with Si CMOS technology [14].

4. Conclusions

In this paper, we have investigated the circuit-level performance of digital logic gates built using the p-type and n-type uniformly doped silicene FETs. By fitting the self-consistent potential at the TOB using fifth order binomial equations, a non-iterative SPICE model for the proposed FETs are created, where the model is then utilised to perform circuit-level

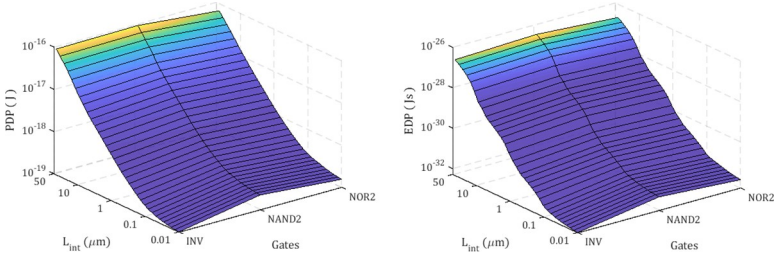

Fig 9. (a) PDP and (b) EDP of silicene-based digital logic circuits. INV, NAND2 and NOR2 represent inverter, 2-input NAND and 2-input NOR gates, respectively.

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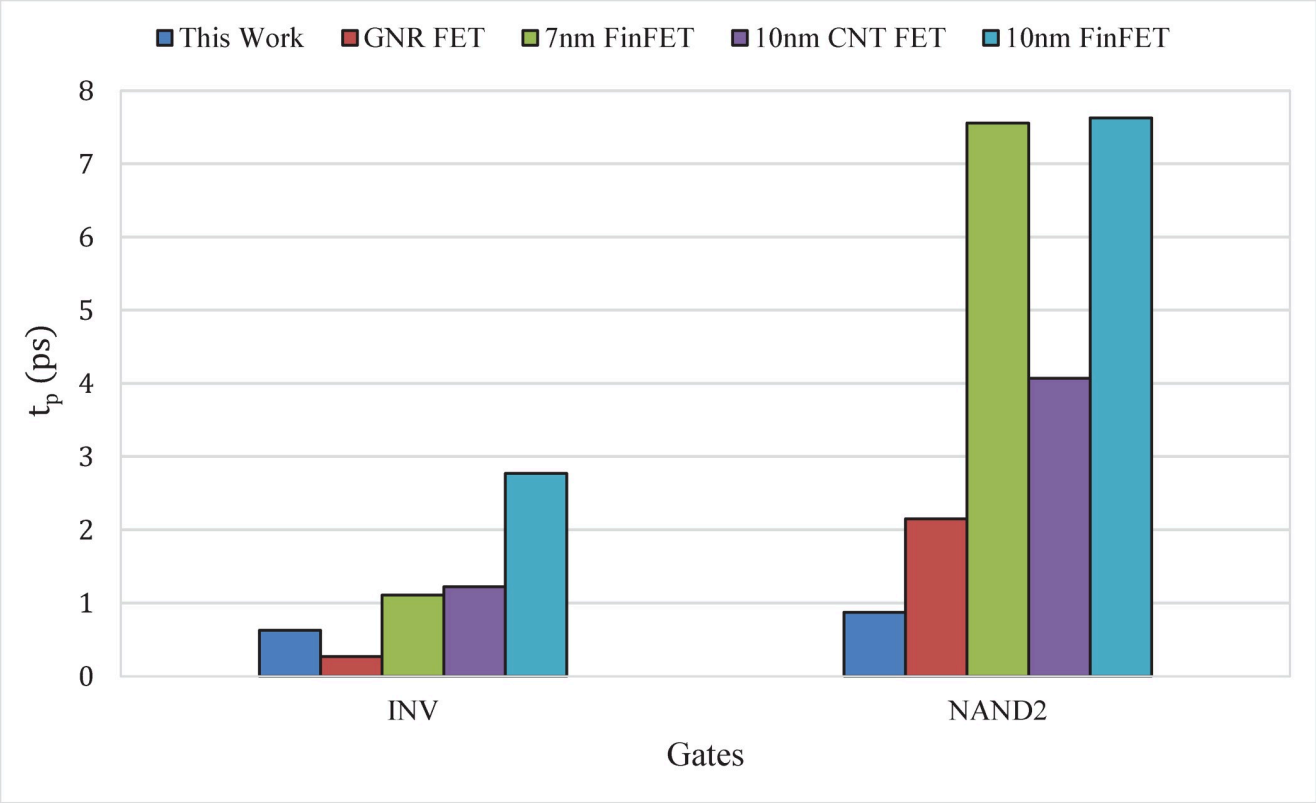

Fig 10. Comparison of propagation delay (t_p) between the proposed silicene-based logic circuit with recent published results. INV and NAND2 represent inverter and 2-input NAND gates, respectively.

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simulations. Following that, the timing diagrams for the proposed silicene-based logic gates are computed and verified. In order to gain more insights from the digital logic output waveforms, the figure of merits for inverter, 2-input NAND, and 2-input NOR gates are extracted and compared to recent published results. Based on the benchmark of the results, the proposed silicene-based inverter has achieved the lowest propagation delay. Although the propagation delay of the proposed silicene-based 2-input NAND gate is outperformed by GNR-based gate, it is still optimistic that silicene-based CMOS logic circuits are promising substitutes for future nanoelectronic devices because graphene-based systems might require an entirely redesigned fabrication technique and equipment for mass production in the semiconductor industry. In future work, it may be useful to extend the present study on the basic logic gates to explore more complex silicene-based digital circuits and systems.

Supporting information

S1 File. Equations and coefficients of self-consistent potential.
(DOCX)

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Supervision: Michael Loong Peng Tan.

Validation: Mu Wen Chuan, Kien Liong Wong, Afiq Hamzah, Shahrizal Rusli, Nurul Ezaila Alias.

Visualization: Mu Wen Chuan.

Writing – original draft: Mu Wen Chuan.

Writing – review & editing: Mu Wen Chuan, Munawar Agus Riyadi, Afiq Hamzah.

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