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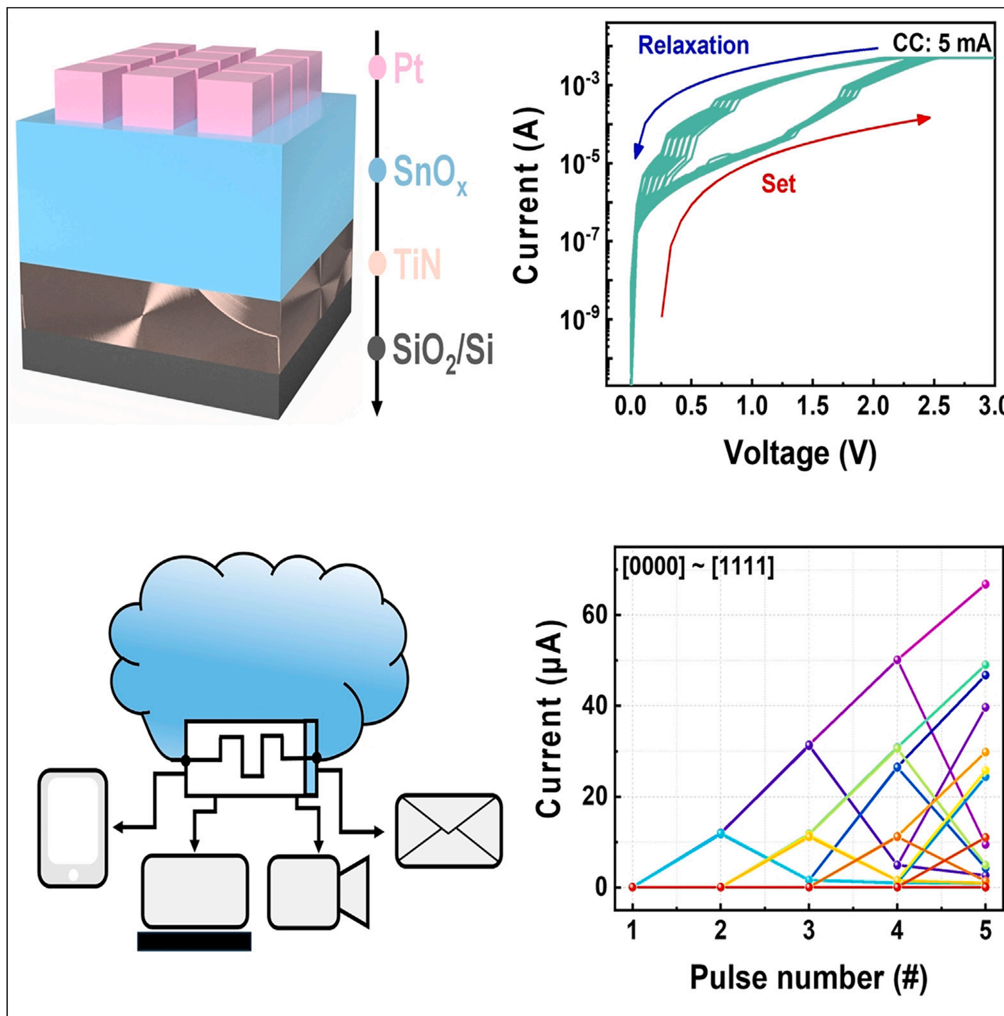

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Highlights

The Pt/SnO_x/TiN memristor showcases unipolar resistive switching properties

Multi-level cell showcased through controlling set bias and compliance current

Short-term memory emulated through volatile memory function

Edge computing demonstrated through application of controlled 4-bit pulse stream

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Article

Volatile tin oxide memristor for neuromorphic computing

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SUMMARY

The rise of neuromorphic systems has addressed the shortcomings of current computing architectures, especially regarding energy efficiency and scalability. These systems use cutting-edge technologies such as Pt/SnO_x/TiN memristors, which efficiently mimic synaptic behavior and provide potential solutions to modern computing challenges. Moreover, their unipolar resistive switching ability enables precise modulation of the synaptic weights, facilitating energy-efficient parallel processing that is similar to biological synapses. Additionally, memristors' spike-rate-dependent plasticity enhances the adaptability of neural circuits, offering promising applications in intelligent computing. Integrating memristors into edge computing architectures further highlights their importance in tackling the security and efficiency issues associated with conventional cloud computing models.

INTRODUCTION

In the landscape of modern computing, traditional architectures (epitomized by the von Neumann model) are encountering escalating challenges in terms of energy efficiency, scalability, and versatility. This has instigated a search for alternative paradigms capable of emulating the parallel processing prowess of the human brain, resulting in the emergence of neuromorphic computing as a promising contender.[1–4] Within this quest for neuromorphic computing solutions, various types of next-generation memory have emerged to adapt such computing functions. Among these, resistive random-access memory (RRAM) is prominent due to its unique advantages over other emerging next-generation memory technologies, such as phase-change RAM (PcRAM), magneto-resistive RAM (MRAM), ferroelectric tunnel junctions (FTJs), and ferroelectric RAM (FRAM). RRAM offers several distinct advantages, including its capacity for fast switching speeds, energy-efficient operation, and simplicity.[5–11] Unlike PcRAM, which relies on phase transitions between the amorphous and crystalline states, RRAM employs resistive switching mechanisms, enabling faster switching speeds and lower energy consumption.[12] In contrast, MRAM relies on magnetic effects for data storage, which can result in higher power consumption and scalability challenges compared to RRAM.[13] Furthermore, RRAM's compatibility with complementary metal-oxide-semiconductor (CMOS) processes facilitates seamless integration into existing semiconductor fabrication technologies, offering advantages of scalability and cost-effectiveness compared to FTJs.[14–16] RRAM's ability to achieve multi-bit storage per cell (surpassing the binary storage of FTJs and FRAM) further enhances its suitability for neuromorphic computing applications, where the ability to store and process analog information is crucial.[17] Unipolar switching is another characteristic feature of RRAM devices that provides additional benefits for neuromorphic computing applications. Unlike bipolar switching, which involves both set and reset operations, unipolar switching only requires one type of voltage bias application to toggle between the high and low resistance states.[18,19] This simplifies device operation and control, while also reducing the complexity and energy consumption associated with synaptic emulation in neuromorphic computing systems. In general, typical RRAM devices comprise three consecutive layers: a bottom electrode, an insulating layer, and a top electrode. The insulating layer is situated between the electrodes and functions as the switching layer, where resistive changes occur due to the migration of ions or defects.[8] Among the various materials used for the insulating film, metal oxides are the most commonly employed and can be deposited using various techniques, such as atomic layer deposition, sputtering, or spin coating.[20–22] Metal oxide materials offer high-speed operation, reliability, and compatibility with current CMOS technology, enhancing cost-effectiveness during fabrication.[23–25] Typically, metal-oxide-based RRAM operates by the migration of oxygen ions when an external bias is applied, resulting in the creation of a conductive filament or defective region, altering the memristor's resistance states.[26–28]

Recently, there have been attempts to integrate various functionalities into a single memristor to improve cost-effectiveness in neuromorphic computing applications. For example, some studies have explored the application of computing architectures such as reservoir computing and Pavlov's training using memristors.[29,30] Similarly, Du et al. demonstrated the use of dynamic memristors for reservoir computing, enabling the analysis of time-series data.[31] Jena et al. implemented Pavlov's experiment using Ag/TiO_2/Pt memristors, facilitating the establishment of strong synaptic interactions through training.[32] While various functionalities have been demonstrated in recent studies, edge computing is an aspect of memristor-based functionality that has received less attention. Edge computing revolves around processing

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Table 1. Comparison of the $Pt/SnO_x/TiN$ memristor in comparison to the previous devices

No.	Structure	Switching characteristic	Switching type	Window	Operating voltage	Multi-level state	Synapse emulation	Versatile behaviors	Reference
1	$Ag/HfO_2/Pt$	Unipolar	Digital	>10,000	0.5 V	X	O	X	Abbas et al.[38]
2	$Au/CSPbBr_3/ITO$	Bipolar	Digital	N/A	−0.5 to 0.5 V	X	O	X	Luo et al.[39]
3	Ag/ZnO/Ag	Unipolar	Digital	N/A	1 V	6	O	X	Chen et al.[40]
4	Cr/ZnO/FTO	Bipolar	Analog	>400	−3 to 3 V	X	O	X	Pham et al.[41]
5	ITO/ZnO NPs/ITO	Bipolar	Digital	N/A	−3 to 3 V	X	O	X	Fan et al.[42]
6	$W/WO_x/GaO_x/ITO$	Bipolar	Analog	N/A	−1 to 1 V	X	O	X	Liu et al.[43]
7	ITO/MXene/EGaIn	Bipolar	Digital	>100	1.5 to −2.5 V	X	X	Edge computing, Pavlov conditioning	Thomas et al.[44]
8	Pt/LCO/NiO/Pt	Bipolar	Analog	N/A	−3.5 to 3.5 V	X	O	X	Jeong et al.[45]
9	$Ag/FAPbI_3/SnO_2/ITO$	Bipolar	Analog	>100	−1.5 to 1 V	X	O	X	Lee et al.[46]
10	$Pt/SnO_x/TiN$	Unipolar	Analog	>22	3 V	23	O	Edge computing	This study

X, no emulation of synase showccased; O, emulation of synapse shown.

data closer to its origin and offers notable advantages, including latency reduction, bandwidth optimization, and enhanced privacy and security.[33] This is achieved by distributing computation and storage resources nearer to the data-generating devices, such as IoT devices, sensors, and autonomous systems. Moreover, this approach minimizes the need to transmit data to centralized data centers, resulting in real-time decision-making and responses, which are crucial for time-sensitive applications such as autonomous vehicles and industrial automation.[34,35] Edge computing also reduces network congestion and data transmission costs by processing and filtering data locally, transmitting only essential information to the cloud or data center. This overcomes one of the main limitations of current cloud computing,[33,36] enhances overall system efficiency, and addresses privacy concerns by processing sensitive data locally. Hence, risks associated with transmitting data over insecure networks are mitigated. When memristor-based neuromorphic computing systems are employed in edge computing, additional benefits are realized. For example, the fast-switching and energy-efficient nature of RRAM enables efficient processing and storage of data directly at the edge, reducing reliance on centralized computing resources.[37] Additionally, the parallel processing capabilities of memristor arrays facilitate the seamless execution of distributed computing tasks, enhancing the scalability and performance of edge computing systems. By leveraging the complementary strengths of memristor-based neuromorphic computing and edge computing paradigms, future computing architectures will be able to achieve unprecedented levels of efficiency, adaptability, and intelligence.

In this study, we investigated the diverse functionalities of an individual $Pt/SnO_x/TiN$ memristor, focusing on emulating synaptic functions alongside edge computing implementations. Prior to assessing its computing capabilities, the electrical properties of the fabricated memristor were examined through DC bias applications. The results revealed unipolar switching behavior and demonstrated uniformity across cell-to-cell and cycle-to-cycle endurance functions. During the bias sweep, gradual increases and decreases in the current state were observed, indicating a non-filamentary switching operation. This facilitated easy acquisition of multiple resistance states compared to filamentary switching memristors, in which the resistance states depend on the random formation of filaments.[26] Controlled pulse applications demonstrated the achievement of diverse conductance states, enabling potentiation and depression with a linear update of conductance values. Moreover, the volatile properties of the memristor were leveraged to emulate the short-term memory (STM) characteristics of biological brains, facilitating synapse functions such as learning, forgetting, paired-pulse facilitation (PPF), and spike-rate-dependent plasticity (SRDP). Finally, by applying different pulse schemes to the memristor, 4-bit edge computing functionality was implemented, allowing for the generation and consumption of data at a single memristor. Table 1 highlights the versatile functionalities of our memristor compared to previously reported two-terminal resistive switching devices. These findings underscore the versatile and cost-effective functionalities of the $Pt/SnO_x/TiN$ memristor, which is promising for future computing paradigms.

RESULTS AND DISCUSSION

Figure 1A presents a schematic illustration of the fabricated memristor and a summary of the fabrication process of depositing each layer via sputtering. The electrical properties were examined by applying the bias to the top Pt electrode. A cross-sectional transmission electron microscopy (TEM) image that showcases the Pt and TiN electrode with 40-nm-thick SnO_x sandwiched between each layer is depicted in Figures 1B and S1. Furthermore, to examine the chemical properties of the SnO_x insulating film, X-ray photoelectron spectroscopy (XPS) analysis in depth mode examining the chemical composition of the thin films using Ar ion sputtering, etching layer by layer was utilized. Figure 1C showcases the Sn 3d peak spectra of the SnO_x thin film, where doublet peaks of Sn $3d_{5/2}$ and Sn $3d_{7/2}$ were evident at binding energies of approximately 486.2 and 494.6 eV, respectively.[47] Additionally, the O 1s spectra in Figure 1D revealed double peaks at binding energies of approximately 531 and 529.9 eV, representing the oxygen vacancy (V_o^+) and Sn-O bonding, respectively.[48] Thus, through the TEM image and XPS spectra, the presence of the SnO_x switching film was confirmed.

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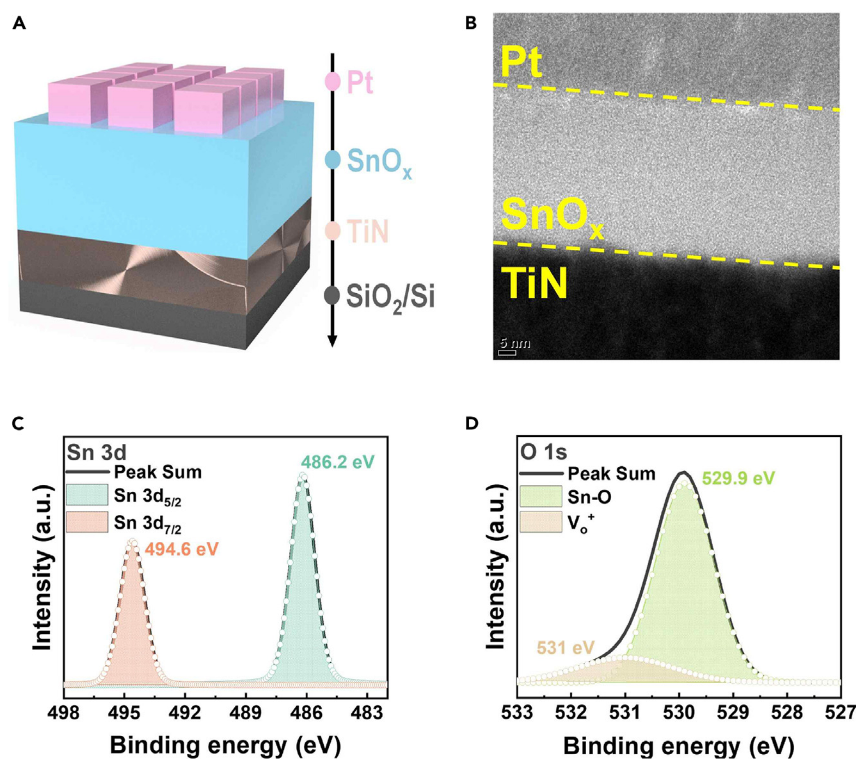

Figure 1. Structural and chemical analysis

(A) Schematic illustration of the Pt/SnO_x/TiN memristor.

(B) Cross-sectional TEM image of the Pt/SnO_x/TiN memristor.

(C and D) XPS peak spectra representing (C) Sn 3d and (D) O 1s of the SnO_x layer.

The electrical characteristics of the fabricated memristor were investigated by applying a DC bias, with a step voltage of 0.05 V Figure 2A displays the I-V curve of the Pt/SnO_x/TiN memristor. Unlike bipolar resistive switching devices, the developed memristor exhibited unipolar switching behavior, where the resistive switching only occurred in a single voltage polarity direction, comprising the set and relaxation processes.[49] When a forward bias of 2.5 V was applied, a gradual increase in current was observed. This reached the compliance current (CC) applied to prevent the hard breakdown of the memristor, reducing its overall resistance. This set process transitioned the device from the off to the on state. Conversely, during a reverse bias sweep from 2.5 to 0 V, the current gradually decreased, indicating the relaxation process. This increased the overall resistance of the memristor and transitioned the device from the on to the off state. Memory storage in resistive switching devices occurs through changes in the resistance state under an applied bias, switching between the high resistance state (HRS) and low resistance state (LRS), corresponding to the off and on states, respectively. In the presented device, the set process switched the device from HRS to LRS, while the relaxation process switched it from LRS to HRS. These resistive switching properties occurred at the same voltage polarity with resultant sequential switching, demonstrating the unipolar resistive switching functionality of the developed memristor, which may be due to the difference in work function between the metal electrode and insulator.[18] Furthermore, the uniformity of the device during continuous switching (known as endurance) was evaluated by sequentially applying 2.5 V to the top electrode. This resulted in a continuous set and relaxation process. Then, by measuring the resistance state from a read bias of 0.7 V, distinct states of LRS and HRS during consistent resistive switching were evident. Figure 2B presents the endurance performance of the Pt/SnO_x/TiN memristor, which demonstrated an average memory window of 22.53 without any significant variation in resistance states. To analyze the variation in resistance states in more detail, the coefficient of variation (CV) was calculated, as displayed in Figure 2C. The LRS and HRS exhibited CV values of 0.027 and 0.154, respectively, indicating minimal variation in resistance states during sequential bias application. The uniformity of the developed memristor across different cells is illustrated in Figure S2, where each I-V curve represents 100 DC cycles from six randomly selected cells, highlighting the consistent performance of the memristor's cell-to-cell and cycle-to-cycle variations. The conduction mechanism of the Pt/SnO_x/TiN device was expected to be non-filamentary due to the gradual increase and decrease of current values in the I-V curve.[50,51] Unlike filamentary RRAM, which exhibits abrupt switching behaviors, non-filamentary switching suggests that resistive switching occurs through the migration of oxygen ions within the insulating layer (Figure 2D), creating defective regions under an applied bias.[51] As demonstrated in Figure 2E, oxygen ions within the SnO_x film migrated toward the top electrode when a positive bias was applied to the Pt electrode. This increased the defective region and enabled conduction, resulting in resistive switching from HRS to LRS. Conversely, during the

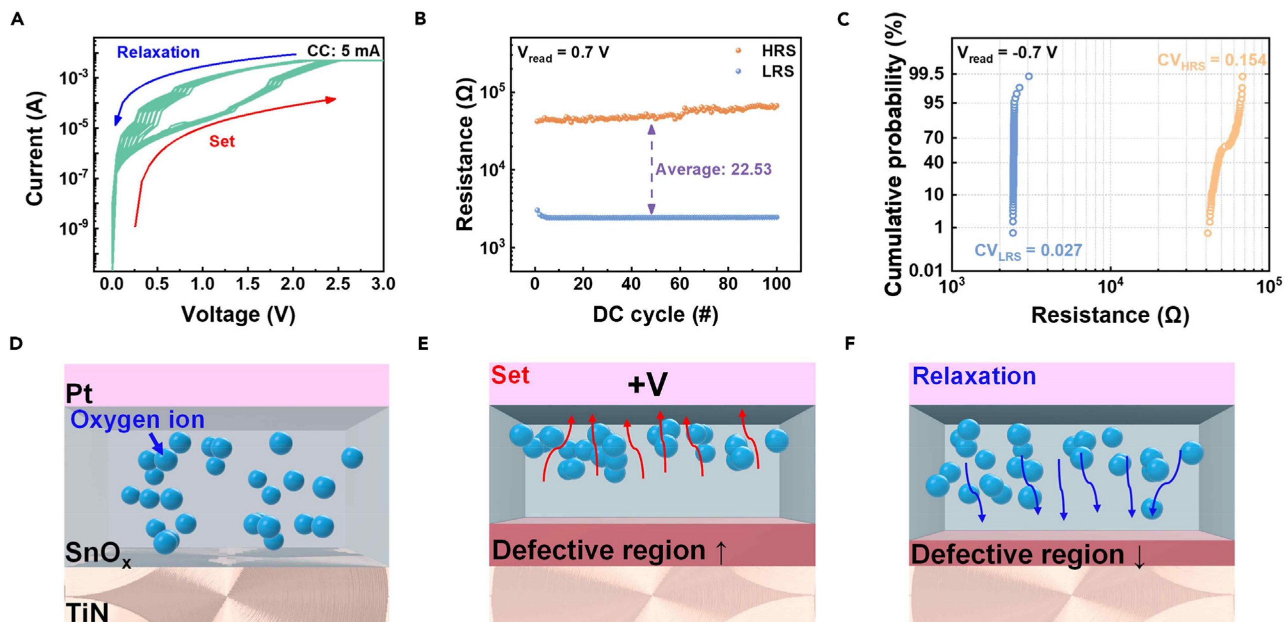

Figure 2. Electrical properties under DC bias application and conduction mechanism

(A) Unipolar resistive switching I-V curve of the Pt/SnO_x/TiN memristor.

(B) Endurance property over 100 DC cycles, gained from a read bias of 0.7 V, representing HRS and LRS.

(C) Variation of the resistance states acquired from 100 DC cycles.

(D–F) Schematic illustrations of the conduction mechanism of the Pt/SnO_x/TiN memristor: (D) initial, (E) LRS, and (F) HRS.

gradual reduction of the applied bias, the self-diffusion of oxygen ions occurred, decreasing the defective region and insulating behavior, resulting in resistive switching from LRS to HRS (Figure 2F).[52]

By using the gradual switching capabilities of the developed memristor, we investigated its multi-level cell (MLC) functionality by varying the set bias and CC during resistive switching. MLC is essential for high-density memory implementation because it increases the storage density of a single memristor by storing data in the HRS, the LRS, and the resistance states between them, enabling large datasets to be stored within a single memristor.[53] Figure 3A demonstrates that MLC was achieved by varying the set voltage, where the set biases ranged from 1.5 to 2.6 V, in an increasing step voltage of 0.1 V, resulting in 12 different LRS states. Increasing the set bias caused increased migration of the oxygen ions, which widened the defective region and altered the LRS. Figure 3B illustrates the endurance properties of each LRS state, where each state was tested for 20 cycles. This result highlighted the easy resistance state modulation and great uniformity of the device. Figure 3C illustrates how MLC was achieved by varying the CC, resulting in 23 different resistance states (0.03, 0.04, 0.05, 0.06, 0.07, 0.08, 0.09, 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1, 2, 3, 4, 5, 6, and 10 mA). The CC in memristors limits the maximum device current when a bias is applied, controlling the migration of oxygen ions and the size of the defective region. Thus, by controlling the CC similar to that of the set bias, enhancement of the defective region could be regulated. The endurance function of the CC-controlled MLC is depicted in Figure 3D, where each of the 23 distinct LRS states underwent 20 uniform DC cycles while maintaining a consistent HRS. The resistance values acquired through varying set amplitudes and CC are analyzed in Figure S3, showcasing the acquired 11 and 23 multi-level LRS states. Overall, the MLC functionality of the Pt/SnO_x/TiN memristor could be easily regulated through various methods, facilitating the attainment of high-density memory with excellent uniformity.

Through the pulse measurements, we demonstrated the neuromorphic computing capabilities and synapse emulation of the Pt/SnO_x/TiN memristor. In biological brains, data processing occurs through the linear update of synaptic weights within interconnected synapses and neurons, facilitating energy-efficient parallel processing.[54] Therefore, achieving gradual data updates and acquiring multiple conductance states within a memristor is crucial for implementing energy-efficient neuromorphic computing. To observe such behavior in the developed Pt/SnO_x/TiN memristor, we examined potentiation and depression by observing the increase and decrease of conductance under the application of sequential set and reset pulses. As the Pt/SnO_x/TiN memristor operates with a single bias polarity, the reset pulses were replaced by read pulses with intervals (0 V), enabling an energy-efficient process without the application of additional reset pulses. Owing to the inert and volatile functions of the presented memristor, a gradual decrease in current under the condition of no bias application was exhibited, resulting in decay similar to depression. Potentiation and depression in the developed memristor consisted of 50 pulses each, with potentiation pulses at 2.5 V for 0.5 ms and depression pulses at 0 V for 2 ms. This was followed by a read pulse at 0.7 V to record the change in conductance. The results of applying this pulse scheme are displayed in Figure 4A, demonstrating a gradual increase and decrease in the conductance states. During continuous potentiation pulses, there was a gradual migration of oxygen ions toward the top electrode, resulting in a gradual increase

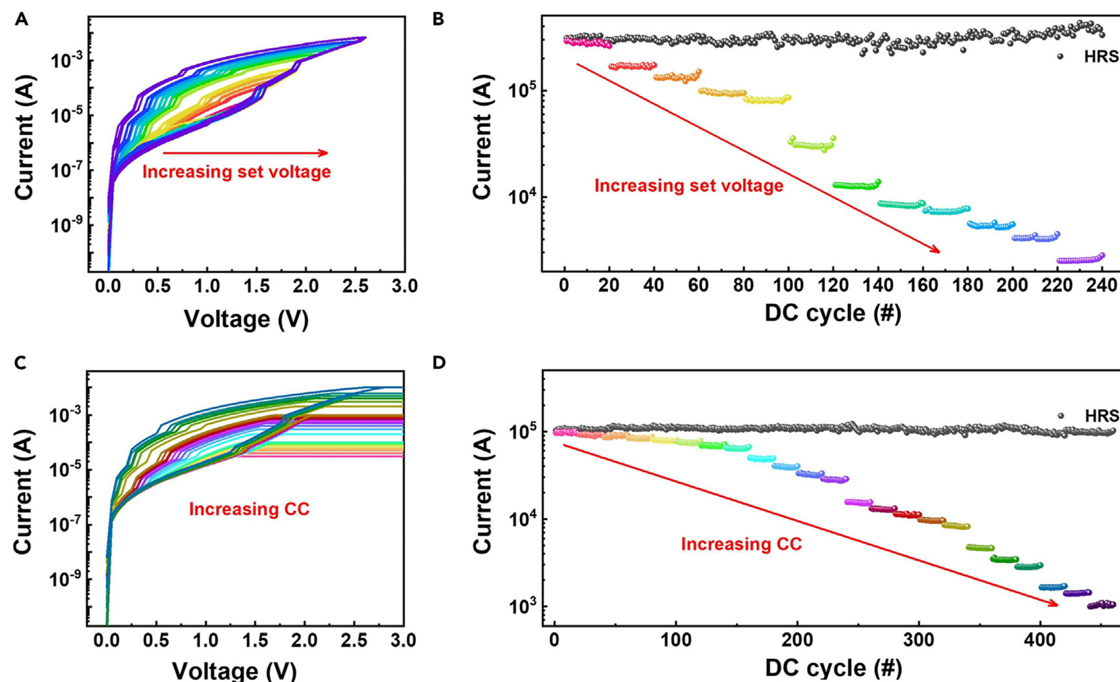

Figure 3. MLC properties of the memristor

(A) MLC properties of the Pt/SnO_x/TiN memristor acquired through differing set voltages.

(B) Endurance properties of the set voltage-induced MLC, representing 20 cycles each.

(C) MLC properties of the Pt/SnO_x/TiN memristor acquired through differing CC values.

(D) Endurance properties of the CC-induced MLC, representing 20 cycles each.

of defective regions. Conversely, the application of 0 V depression pulses resulted in gradual self-diffusion of the migrated oxygen ions, causing a gradual decrease in the conductance states. To assess the uniformity of the potentiation and depression behaviors, the pulse train applications were repeated 10 times, resulting in 10 cycles of repeated potentiation and depression curves, as displayed in Figure 4B. This result confirmed that the behavior was not temporary. Employing the easily controlled conductance functions of the Pt/SnO_x/TiN memristor, further trials were conducted to investigate conductance updates by varying the pulse applications during potentiation and depression. Initially, as depicted in Figure 4C, we varied the width of the pulse during the potentiation process into six different conditions (500 μs–3 ms), while keeping the other parameters constant. The pulse width-varied potentiation and depression behaviors of the Pt/SnO_x/TiN device are illustrated in Figure 4C, demonstrating a linear relationship between the width of the pulse and the maximum conductance value. Additionally, under different conditions, all the potentiation and depression curves exhibited a linear update of the conductance value. The repeatability of this behavior is demonstrated in Figure 4D, where each curve exhibited 10 sequential behaviors. Next, as displayed in Figure 4E, the potentiation and depression behaviors under different pulse numbers were investigated, ranging from 50 to 200. Four different conductance states were obtained, with their repeated behaviors observable in Figure 4F. The interval of potentiation pulses was also varied under five different conditions, as displayed in Figure 4G. Owing to the volatile properties of the developed memristor, a longer pulse interval caused a decrease in the increased conductance after each pulse application, resulting in the smallest enhancement of the conductance value. The repeated potentiation and depression function under different pulse interval conditions is presented in Figure 4H. By observing the potentiation and depression, the easily controlled conductance and its varied values under different pulse circumstances of the Pt/SnO_x/TiN device were demonstrated. This result highlighted the diverse methods of conductance update in the memristor, rendering it suitable for adapting neuromorphic computing.

In biological synapses, synaptic plasticity categorizes memory properties based on the synaptic weight.[55] For instance, a small application of synaptic weight results in short-term potentiation, creating STM, which typically lasts from milliseconds to a few minutes. Accordingly, STM is mainly used for tasks that demand immediate recall and filtering.[56,57] This serves as an interim stage, where information is briefly retained before being either transferred to long-term memory (LTM) or discarded. In the absence of recall, there is a gradual decline in the synaptic weight, eventually causing forgetting. In contrast, by repeatedly engaging in this process, the transition to LTM occurs as the synaptic connections undergo dynamic changes, solidifying key memories over the course of our lives through experiences.[58] Leveraging the volatile properties of the Pt/SnO_x/TiN memristor, we believe that efficient emulation of brain memory (especially STM) can be achieved. For such behavior, firstly, the volatile function of our memristor, depending on the arriving strength of the spike, was observed. Figure 5A depicts excitatory postsynaptic current (EPSC) facilitation occurring through sequential read pulse applications after the arrival of spike sets, resulting in the device's resistance state changing from HRS to LRS. The arrived spikes were modified to 3 V for 1 ms, and the number of spikes was varied

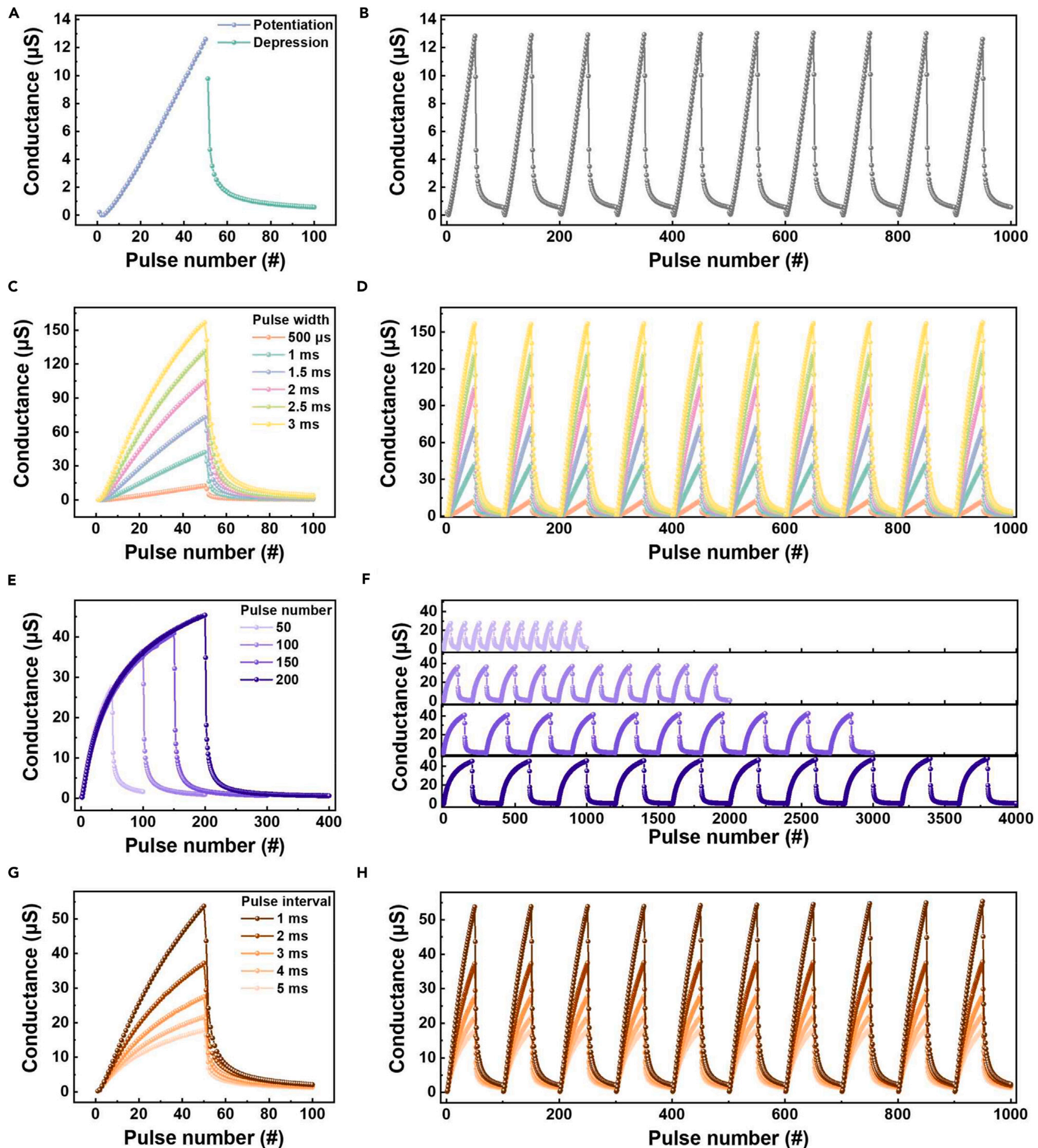

Figure 4. Controllable potentiation and depression function of the memristor

(A) Potentiation and depression behavior of the Pt/SnO_x/TiN memristor.

(B) 10 cycles of repeated potentiation and depression curves.

(C) Potentiation and depression behavior obtained through different widths of the potentiation pulse.

(D) 10 cycles of repeated potentiation and depression curves, tested under different pulse widths.

(E) Potentiation and depression behavior obtained through changing the number of pulses.

(F) 10 cycles of repeated potentiation and depression curves, tested under different numbers of pulses.

(G) Potentiation and depression behavior obtained through differing pulse intervals.

(H) 10 cycles of repeated potentiation and depression curves, tested under different potentiation pulse intervals.

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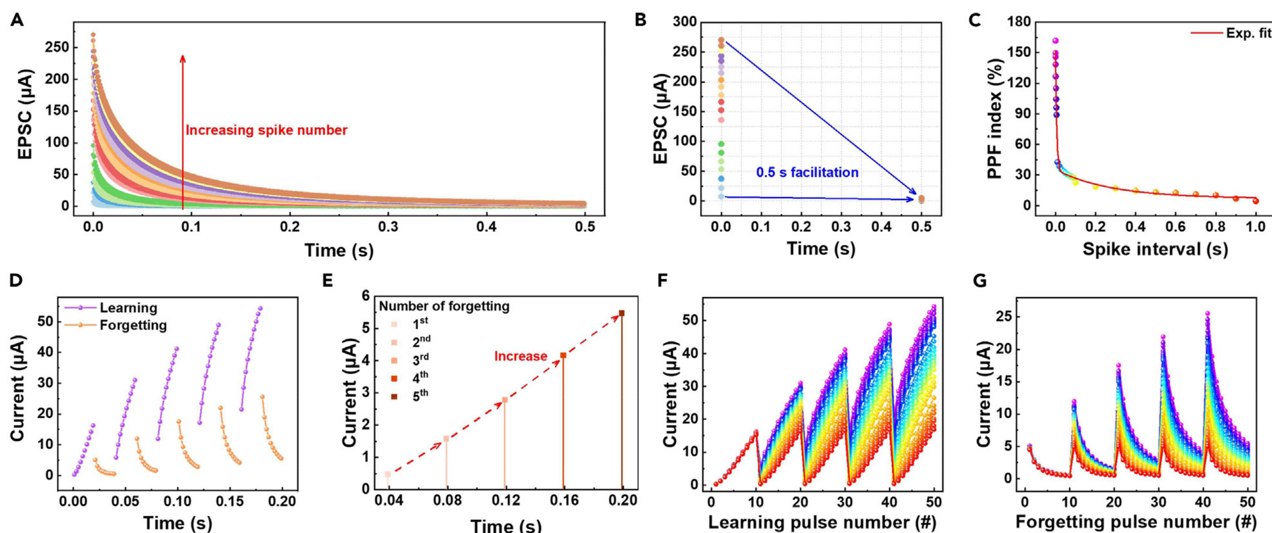

Figure 5. Demonstration of the STM behavior

(A) Observation of STM functions of the $Pt/SnO_x/TiN$ memristor under the application of different numbers of spikes.
(B) Facilitation of current occurring during 0.5 s.
(C) PPF function of the $Pt/SnO_x/TiN$ memristor represented as the change of PPF index as a function of spike intervals.
(D) Learning and forgetting behaviors of the $Pt/SnO_x/TiN$ memristor.
(E) Implementation of increased synaptic plasticity through training rehearsal.
(F) Current changes in the learning property of the memristor, investigated under different learning and forgetting intervals.
(G) Current changes in the forgetting property of the memristor, investigated under different learning and forgetting intervals.

from 5 to 100. Instant facilitation of EPSC occurred after each spike application. After 0.5 s, the applied EPSC saturated into similar levels, showcasing the strong STM functions of the $Pt/SnO_x/TiN$ memristor (Figure 5B). Using these volatile functions of the memristor, PPF was tested, which is a crucial function in biological STM and refers to the relative enhancement between two sequentially arriving spikes.[59,60] Identical spikes of 3 V for 1 ms were applied to the $Pt/SnO_x/TiN$ memristor under different intervals. Owing to the facilitation of current in volatile memristors, longer intervals result in forgetting the previous input, degrading the amount of enhanced current. The term "PPF index" was acquired through the following equation:[61]

$$PPF\ index\ (\%) = \left(\frac{I_2 - I_1}{I_1}\right) \times 100 \quad \text{(Equation 1)}$$

Here, terms I_2 and I_1 represent the current response after the second and first pulses, respectively. Figure 5C displays the PPF index obtained as a function of spike intervals, which indicates a gradual reduction in the PPF index with increasing intervals. This decrease reflected the diminishing enhancement rate due to forgetting associated with longer intervals, mirroring the functions of the biological brain. Additionally, the learning and forgetting behaviors of the biological brain were replicated using the $Pt/SnO_x/TiN$ memristor, as displayed in Figure 5D.[62] The learning process of the memristor involved 10 consecutive learning sections followed by 10 consecutive forgetting sections, each consisting of pulses of 3 V for 1 ms and 0 V for 1 ms. Training the memristor involved applying sequential set pulses, resulting in an increased current, while forgetting entailed a reduction in current due to the absence of training. This behavior mirrors the process in the human brain, where STM gradually decays without rehearsal, resulting in forgetting.[57] Interestingly, Figures 5D and 5E illustrate that throughout the sequential training and forgetting process, there was an overall increase in current. Again, this mirrors the brain function, where rehearsal results in the transition from STM to LTM due to increased synaptic plasticity.[56] The developed memristor's function was further modified by simply tuning the current states under pulse applications, as demonstrated in Figures 5F and 5G. The data indicated varying intervals between each training and forgetting sequence, ranging from 0 to 4 s. As the interval increased (indicated by the red dots), the current enhancement between each training section tended to decrease, resulting in complete forgetting after each forgetting section. Conversely, as the interval decreased (indicated by the purple dots), the current enhancement between each training section tended to increase, resembling stronger synaptic plasticity. This resulted in the transition from STM to LTM through the rehearsal process, as the current after each forgetting sequence increased.

The $Pt/SnO_x/TiN$ memristor also demonstrated modification of the synaptic weight in response to incoming spikes in synaptic connections, adhering to the principle of SRDP.[63] SRDP is a phenomenon observed in synaptic connections where the strength of synaptic transmission changes in response to the rate of neuronal firing or the spike frequency.[64] This mechanism allows synaptic connections to adaptively regulate their strength according to the activity patterns of interconnected neurons, improving the flexibility of neural circuits and facilitating information encoding in the brain. To assess this adaptability, the neural firing patterns of the arriving spikes at the synapse were manipulated

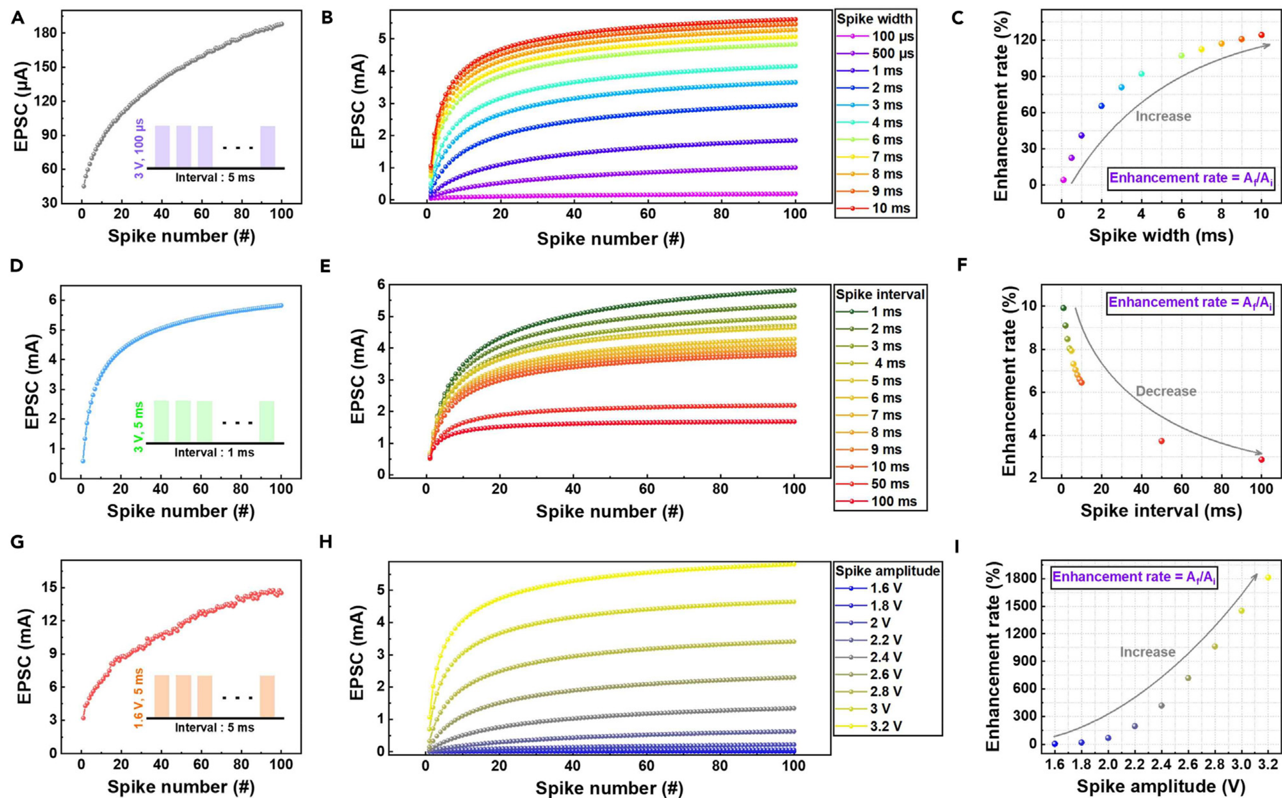

Figure 6. Synapse function emulation

(A) SRDP function of the Pt/SnO_x/TiN memristor. Change of EPSC observed under pulse spike of 3 V for 100 μs with an interval of 5 ms.

(B) SRDP function observed under differing spike widths.

(C) Changes in enhancement rate as a function of spike width.

(D) Changes in EPSC under pulse spike of 3 V for 5 ms with interval of 1 ms.

(E) SRDP function observed under differing spike intervals.

(F) Changes in enhancement rate as a function of spike interval.

(G) Changes in EPSC under pulse spike of 1.6 V for 5 ms with an interval of 5 ms.

(H) SRDP function under differing spike amplitudes.

(I) Changes in enhancement rate as a function of spike amplitude.

under three different conditions, which were categorized based on the altered parameters. Figures 6A–6C depicts the impact of the spike width on synaptic weight change. To investigate this function, pulse sets comprising 100 set pulses of 3 V and 100 μs with intervals of 5 ms were applied to the memristor (inset of Figure 6A), resulting in EPSC enhancement (Figure 6A). Leveraging this spike-induced EPSC enhancement behavior, the width of the spikes was varied across 11 different conditions, ranging from 100 μs to 10 ms, as depicted in Figure 6B. The enhancements observed under different spike width conditions are summarized in Figure 6C, where the term "Enhancement rate" was calculated using the following equation:

$$\textit{Enhancement rate}\,(\%) = \left(\frac{A_f}{A_i}\right) \quad \text{(Equation 2)}$$

Here, terms A_f and A_i denote the EPSC value after 100 spike applications and the initial state, respectively. Figures 6D–6F displays the SRDP behavior based on the spike intervals. To investigate this function, 100 spikes with 3 V over 5 ms were applied to the memristor with an interval of 1 ms (inset of Figure 6D), resulting in EPSC enhancement. Figures 6E and 6F demonstrate the application of varied spike intervals to the memristor, where the intervals were varied into 12 different conditions ranging from 1 to 100 ms. This resulted in a decrease in the enhancement rate as the spike intervals increased, which was attributed to the volatile properties of the Pt/SnO_x/TiN device. Finally, as depicted in Figures 6G–6I, the SRDP behavior was explored based on the spike amplitude intervals. Here, a sequence of 100 set pulses with 1.6 V over 5 ms and an interval of 5 ms was applied to the Pt/SnO_x/TiN memristor to observe the EPSC response, as displayed in Figure 6G. The SRDP function under varied amplitude conditions (1.6–3.2 V), showcasing nine different conditions, is depicted in Figure 6H. This revealed a linear relationship between the spike amplitude and enhancement rate, where stronger spikes resulted in larger synaptic weights.

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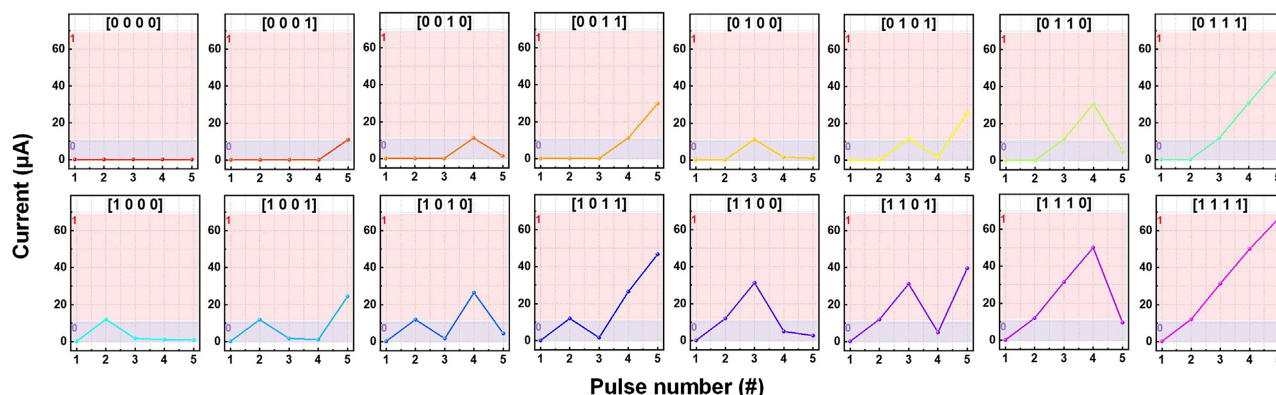

Figure 7. Demonstration of 4-bit edge computing utilizing Pt/SnO_x/TiN memristor

Examining the diverse capabilities of the developed memristor will be vital to provide a more comprehensive understanding of its potential and limitations, allowing us to optimize its effectiveness for specific applications. Moreover, by investigating its flexible functionalities, we could achieve cost savings by integrating various functions into a single memristor, eliminating the requirement for multiple specialized components. This versatility would facilitate enhancing the performance while simplifying the design complexity, ultimately resulting in a more efficient and multifunctional device. Furthermore, in addition to applications in neuromorphic computing, exploring the memristor's ability to emulate synapses opens up possibilities for implementing systems such as edge computing within a single memristor. Edge computing is a partially distributed computing topology where data processing occurs locally at the edge near the user, addressing the challenges in security and efficiency encountered in traditional cloud computing. In contrast to cloud computing, where data generation and usage are centralized at the cloud server, edge computing distributes data processing closer to the source, enhancing security and efficiency.[33] Edge computing enables users to directly access data stored within the memristor, facilitating a power-efficient computing architecture (Figure S4A).[33] In this setup, a series of pulses is categorized into two types, where "1" represents a potentiation pulse of 3 V for 5 ms, while "0" represents a decay pulse of 0 V for 5 ms, followed by a read pulse of 0.7 V to record state changes. Each "1" and "0" denotes the write and erase sequences, respectively. By employing this pulse scheme with distinct "1" and "0" states, 16 different states corresponding to binary numbers from 0 to 15 are possible, allowing successful implementation of 4-bit edge computing using the developed Pt/SnO_x/TiN memristor (Figures 7 and S4B).

Conclusions

The Pt/SnO_x/TiN memristor described in this paper presents a promising avenue for advancing neuromorphic computing and edge computing paradigms. Through its unique resistive switching behavior and versatile functionalities, this memristor offers an efficient and scalable solution for emulating synaptic behavior and implementing complex computing tasks. In terms of neuromorphic computing, the Pt/SnO_x/TiN memristor demonstrated unipolar resistive switching operating under singular voltage polarity. Moreover, its MLC functionality would facilitate high-density memory implementation, while its pulse-modulated conductance updates enable adaptable and flexible operation. The memristor's ability to emulate synaptic plasticity, as evidenced by its SRDP behavior, also opens up avenues for advanced computing systems. By dynamically adjusting the synaptic strength based on spike frequency, the Pt/SnO_x/TiN memristor enhances the adaptability of neural circuits, paving the way for intelligent computing applications. Beyond neuromorphic computing, the Pt/SnO_x/TiN memristor also demonstrates potential for edge computing applications. In addition, its integration within a single device enables efficient and power-conscious computing topologies, addressing the security and efficiency challenges encountered in traditional cloud computing models. Overall, the Pt/SnO_x/TiN memristor represents a versatile and efficient building block for next-generation computing systems, offering opportunities for innovation in diverse fields ranging from artificial intelligence to IoT and beyond.

Limitations of the study

The use of volatile memristors based on SnO_x has facilitated edge computation and versatile synapse functions. Due to their volatility, data generated at the edge are automatically erased without requiring an erase sequence. However, for certain edge computing applications, retaining the generated data might be crucial. Therefore, it is suggested to employ second-order memristors, which exhibit both non-volatile and volatile characteristics, in future edge computing implementations.

STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

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SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.isci.2024.110479.

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AUTHOR CONTRIBUTIONS

Conceptualization, fabrication, formal analysis, investigation, performed the experiments, resources, and writing – original draft, D.J.; writing – review and editing, resources, supervision, project administration, and funding acquisition, S.K.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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STAR★METHODS

KEY RESOURCES TABLE

REAGENT or RESOURCE	SOURCE	IDENTIFIER
Chemicals, peptides, and recombinant proteins		
Ti target (>99.99% purity)	THIFINE	N/A
Sn target (>99.99% purity)	THIFINE	N/A
Pt target (>99.99% purity)	THIFINE	N/A

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources and reagents should be directed to and will be fulfilled by the lead contact, Sungjun Kim (sungjun@dongguk.edu).

Materials availability

This study did not generate new unique materials.

Data and code availability

- Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.
- This manuscript did not generate new data or code.
- All other items: Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

EXPERIMENTAL MODEL AND STUDY PARTICIPANT DETAILS

This study does not use experimental models typical in the life sciences.

METHOD DETAILS

Experimental procedures

Fabrication of memristor

The Pt/SnO_x/TiN stacked memristor was created by sequentially depositing each layer onto a SiO_2/Si substrate. Initially, the substrate was prepared and cleaned with isopropyl alcohol (IPA) and acetone. Then, a 100-nm-thick TiN bottom electrode was deposited using DC reactive sputtering, with a Ti target of 99.99% purity, a main chamber pressure of 3 mTorr, and a DC power of 120 W. Ar and N_2 gases were used at flow rates of 19 and 1 sccm, respectively. Following this, a 40-nm-thick SnO_x insulating layer was deposited on the TiN electrode via RF sputtering, using a Sn target of 99.99% purity at a main chamber pressure of 3 mTorr and an RF power of 60 W. The flow rates of the Ar and O_2 gases were 20 and 10 sccm, respectively. Subsequently, a square-patterned top electrode with a width of 100 μm was patterned on the SnO_x layer using negative photoresist (PR) and photolithography techniques. Finally, a 100-nm-thick Pt top electrode was deposited via DC sputtering using a Pt target of 99.99% purity at a main chamber pressure of 5 mTorr and a DC power of 90 W. Ar gas was used at a flow rate of 20 sccm. A lift-off process in acetone was then employed to finalize acquirement of the Pt electrode.

Structural characterization

For the XPS depth analysis, a Nexsa instrument equipped with a microfocus monochromatic Al-K X-ray source (1486.6 eV) was used with an Ar^+ sputter source, an ion energy of 2 kV, and a beam size of 50 m. Additionally, cross-sectional TEM images were obtained to examine the structural characteristics of the fabricated memristor using equipment from Oxford Instruments (UK).

Electrical measurements

The DC I-V curves and pulse transients of the Pt/SnO_x/TiN memristor were evaluated using a semiconductor parameter analyzer (Keithley 4200-SCS and 4225-PMU ultrafast module, Solon, OH, USA). For testing, a voltage bias was applied to the top Pt electrode while the bottom TiN electrode was grounded under room temperature and pressure conditions.

QUANTIFICATION AND STATISTICAL ANALYSIS

This study does not include statistical analysis or quantification.

ADDITIONAL RESOURCES

Additional resource contains magnified TEM image and electrical properties can be found in the supplemental information.