Heliyon

Mitigation of harmonics and unbalanced source voltage condition in standalone microgrid: positive sequence component and dynamic phasor based compensator with real-time approach

M. Rane [*], **S. Wagh**

Electrical Engineering Department, VJTI, Mumbai, India

* Corresponding author.
E-mail address: msrane_p15@ee.vjti.ac.in (M. Rane).

Abstract

Penetration of Distributed Energy Resources (DER) is in high demand to supply power to the load where the grid is not available. Many of these sources are a single phase source used to form standalone Microgrid (MG). Single phase connectivity of these sources results in an unbalanced source voltage condition (UbSVC). Interfacing power electronic devices also inject the harmonics into Point of Common Coupling (PCC) voltage. The effect of this unbalance and harmonics on the operation of standalone MG is analysed in this paper in a twofold manner. One at a reduced power transfer from DER to load and the other is an error produced in Phase Locked Loop (PLL) operation. Positive Sequence Component (PSC) based and Dynamic Phasor (DP) based compensation techniques are proposed in this paper to mitigate the effect of UbSVC. Simulation validates that both the proposed methods are capable to provide balanced load voltage condition under UbSVC in terms of Voltage Unbalance Factor (V_{UbF}). It also enhances the power transferred from DER to load during an UbSVC. The performance of the proposed compensator during

UbSVC and harmonic presence is validated in real-time simulation using Opal-RT and dSPACE simulators.

Keywords: Electrical engineering

1. Introduction

Three phase power system is operated with sinusoidal generated voltages equal in magnitude, and 120° apart under ideal condition. In practice, the voltages at the distribution end and at PCC found to be unbalanced either in magnitude form or phase form or even both. Various reasons are explored for this unbalance. A significant source of unbalance is the non-uniform distribution of single-phase loads which changes regularly in a random manner. Apart from this, unequal impedances of a transformer, open delta transformer operation and uneven transposition of transmission lines caused unbalance voltage. Modern power electronic converters, variable speed drives who penetrates harmonics in the system is also one of the reasons for unbalanced in the system. The majority of pieces of literature [1], [2], [3], and [4] used energy storage based compensation techniques to compensate for the unbalanced condition mostly based on energy storage elements. They supplied injected energy from energy storage elements [1] such as a battery, the capacitor through a bi-directional converter. This element has limited storage and thus limited to a short duration of compensation. Optimisation of energy storage requirement is studied in [3] using a cascading converter. Voltage compensation using a matrix converter and the flywheel as energy storage is proposed in [2] has put-forward constrained towards long duration voltage compensation. Two methodologies have introduced by [5] based on DVR to compensate voltage sag, swell, flicker and unbalance. It claims that the method is free from the energy storage element, but the operation during fault condition is unclear since the input voltage of DVR reduced to zero under the fault condition. The instantaneous symmetrical component theory was applied by [6] to propose control strategies for load compensation under UbSVC. The author has considered ideal compensator which provides no limitations towards magnitude and duration of compensation. Unbalanced PCC voltage regulation scheme with positive and negative sequence control for the modular multilevel converter (MMC) was proposed in [7] for medium-voltage distribution static synchronous compensator (DSTATCOM). As the MMC uses many switches, control is convoluted. All these kinds of literature discussed were based on the downscale prototype model either on simulation level or experimental level. In reality, grid modelled as infinite source, thus compensating voltage unbalance in any form requires compensator of considerable size, which is

not feasible economically, but in the case of MG, it is feasible to compensate UbSVC due to its limited generating capacity.

An MG is the cluster of DERs along with local load. Under the standalone mode of process, unbalance occurs due to an operation of local single phase load, single phase sources such as Photovoltaic (PV) and Fuel cell (FC). Intermittent operation of these sources also injects the harmonics at the PCC thus distorts the PCC voltage. Three phase balancing techniques have been proposed by [8] using PV surplus generation capacity. The author suggests a negative sequence current injection to suppress voltage unbalance in an MG. Due to the utilisation of surplus capacity, it puts limitations towards compensation of severe unbalance. Cooperative droop control has been proposed by [9], and [10] to share evenly the unbalance current among the converters. Approach to compensate voltage unbalance in an MG through proper control of the DGs interface converter has been proposed by [11]. Negative sequence reactive power has applied to the generation of voltage unbalance compensation reference. Methodology found to be limited towards magnitude unbalance and undefined for harmonic presence. Positive-sequence, negative-sequence, and zero-sequence voltage and current control schemes are proposed [12] in the dq frame for the Voltage Source Converter (VSC)-based distributed generation (DG) units in order to compensate for voltage unbalance in MG. An adaptive capacitive virtual scheme [13] has been proposed on a hierarchical control structure. The experimental results verified that the addition of virtual capacitances distorts the output voltage to reduce unbalanced voltage condition well below the permissible limit. The selective virtual impedance loop, the local voltage unbalance and harmonics compensation block, and the auxiliary selective compensation of PCC voltage characteristic harmonics in MG is used in [14] to compensate the unbalance condition. The particle swarm optimisation (PSO) algorithm has been suggested in [15] to optimise the PI controller coefficient for enhancement of voltage unbalance factor in MG but lacking towards a discussion on improvement during harmonic condition.

Accurate grid phase angle information is required to operate MG under grid connected mode of operation or the island form of operation. Even standalone mode of operation of the MG, need to track the phase angle of the major source. A PLL is a favourite tool used conventionally to monitor phase angle and frequency of the grid. The unbalanced operation of grid or major source in standalone MG introduces errors in the PLL operation. This error in the PLL operation introduces deviation in grid synchronisation and power transfer from individual DER into MG. Under this condition, PV based MG which has a low short-circuit capacity, and the low X/R ratio may lead to the unstable operation of the MG [16]. This makes essential to mitigate UbSVC in a standalone MG. To the best of the author's knowledge limitations observed in the literature are as given below,

- Effect of PCC voltage unbalances on power injection by DER
- The impact of unbalance on synchronisation of DER which may occur due to the error produced by a PLL

Based on the shortcomings in the literature following contributions are addressed in this paper.

- The impact of unbalance on synchronisation of DER and power injection from DER is analysed.
- Dynamic phasor (DP) based approach is used first time to design a compensator which provides active compensation during harmonic presence.
- Positive sequence component based compensator is proposed which considers zero component of *dq0* transformation provides more accuracy in the compensation.
- The performance of the proposed compensator is validated in real-time simulation using Opal-RT and dSPACE simulators, where dSPACE mimics the compensator and Opal-RT as a plant.

This paper is structured as follows. Basic of unbalanced voltage is discussed in Section 2. Section 3 explains the analysis of voltage unbalance in the form of magnitude, and phase angle. Section 4 presents the two algorithms towards mitigation of UbSVC. The validation of both compensation techniques using simulation is described in Section 5. Section 6 focused on the comparison of proposed compensator with the literature. In Section 7, HIL validation for harmonic mitigation is illustrated with architecture and experimental results. Lastly, Section 8 states the conclusion and future scope for further advancement.

2. Background

2.1. Voltage unbalance

IEEE Std $112^{TM} - 2004$ [17] [18] specifies the definition for unbalanced voltage as the ratio of maximum deviation (V_{m_avg}) from the average of the three-phase voltage (V_{avg}) to the average of the three-phase voltage, expressed in percentage as shown in (1). The phase angle unbalance is not mirrored in (1) since it is based only on magnitudes.

$$\%V_{unbalance} = \left(\frac{V_{m\_avg} - V_{avg}}{V_{avg}} \right) \times 100 \tag{1}$$

Another definition expressed concern positive and negative sequence component as the ratio of negative sequence voltage to the positive sequence voltage, expressed in

percentage as shown in (2). It is termed as Voltage Unbalance Factor (V_{UbF}) [18], [19], [20]

$$\%V_{UbF} = \left(\frac{V_-}{V_+}\right) \times 100 \tag{2}$$

where, V_+ and V_- are the positive sequence and negative sequence [20] voltage component of unbalanced voltage respectively. The author has termed it a "Correct Definition" of unbalanced voltage. Permissible value as per various standards $\%V_{UbF}$ is less than 2% for the effective operation of a load on the distribution network. Further, it is classified as uneven voltage magnitudes at the nominal frequency, elemental phase angle divergence and even both inclusive [21]. The cause of unbalance in scale is the result of the dissymmetry of transmission lines, distribution line, and transformer. It is practically impossible to manage perfect balance in the distribution lines. Nonuniform dissemination of load over three phases and the nature of load are the causes of a phase angle unbalance. Compared to conventional power generation where synchronous generators are generating a three-phase voltage which is symmetrical, but in the case of standalone MG where the many DERs like PV are connected at the distribution level in a single phase, form creates unbalanced in the system. Low X/R ratio and lower short circuit level of the system exaggerates the unbalance [22].

3. Analysis

3.1. Analysis of voltage unbalance in magnitude

Three phase balanced voltages are represented as three phases of equal in magnitude with 120° phase difference as given in (3),

$$v_a = V_m \sin\theta; \quad v_b = V_m \sin\left(\theta - \frac{2\pi}{3}\right);$$
$$v_c = V_m \sin\left(\theta + \frac{2\pi}{3}\right) \tag{3}$$

Let 'x', 'y', and 'z' be the unbalanced coefficients of magnitude for 'a', 'b', and 'c' phase respectively thus phase voltages are given as in (4),

$$v_a = x.V_m \sin\theta; \quad v_b = y.V_m \sin\left(\theta - \frac{2\pi}{3}\right);$$
$$v_c = z.V_m \sin\left(\theta + \frac{2\pi}{3}\right) \tag{4}$$

These unbalanced voltages are transformed into $d-q$ form as given below in (5), (6)

$$v_d = \frac{1}{2\sqrt{3}}V_m.\sin2\theta.(z-y) + \frac{1}{6}V_m.\cos^2\theta.(4x+y+z) + \frac{1}{2}V_m.\sin^2\theta.(y+z) \tag{5}$$
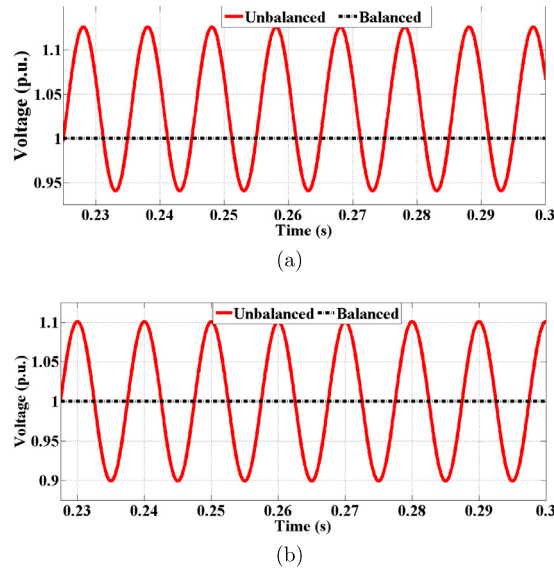
(a)

(b)

Figure 1. d-axis voltage under (a) Magnitude unbalance, (b) Phase unbalance.

$$v_q = \frac{1}{2\sqrt{3}} V_m . cos2\theta . (z - y) + \frac{1}{6} V_m . sin2\theta . (-2x + y + z) \tag{6}$$

Under balanced condition, $V_d = V_m$ and $V_q = 0$ thus compared with (5) and (6) indicates an error in magnitudes of V_d and V_q due to unbalance in the magnitude of voltages.

3.2. Analysis of voltage unbalance in phase angle

Let $\Delta\theta_1$, $\Delta\theta_2$, $\Delta\theta_3$ be the small shift in the phase angle of phase A, B, and C respectively and represented as in (7).

$$v_a = V_m \, sin\left(\theta + \Delta\theta_1\right) \tag{7a}$$

$$v_b = V_m \, sin\left(\theta + \Delta\theta_2 - \frac{2\pi}{3}\right) \tag{7b}$$

$$v_c = V_m \, sin\left(\theta + \Delta\theta_3 + \frac{2\pi}{3}\right) \tag{7c}$$

Voltages under phase unbalanced conditions are transformed into synchronously rotating frame as in (8), (9)

$$v_d = V_m - \frac{V_m . cos2\theta . \left(\Delta\theta_2 - \Delta\theta_3\right)}{2\sqrt{3}} - \frac{V_m . sin2\theta}{3} \left(\Delta\theta_1 - \frac{\Delta\theta_2 + \Delta\theta_3}{4}\right) + \frac{V_m . sin2\theta}{4} \left(\Delta\theta_2 + \Delta\theta_3\right) \tag{8}$$

(a)

(b)

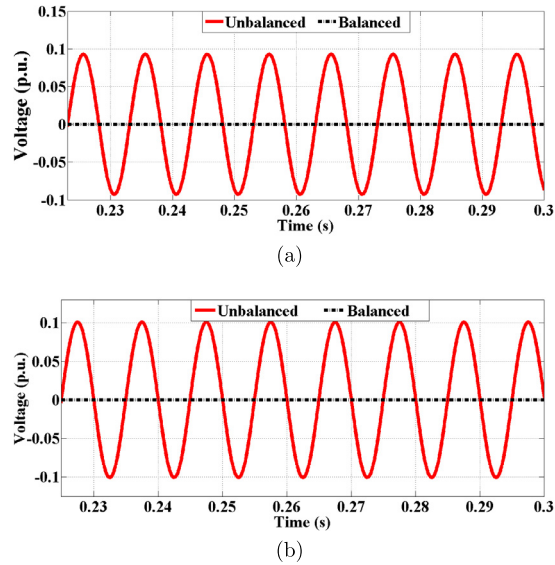**Figure 2.** q-axis voltage under (a) Magnitude unbalance, (b) Phase unbalance.

$$v_q = \frac{V_m.sin2\theta\left(\Delta\theta_2 - \Delta\theta_3\right)}{2\sqrt{3}} + \frac{2V_m.sin^2\theta}{3}\left(\Delta\theta_1 - \frac{\Delta\theta_2 - \Delta\theta_3}{4}\right)$$
$$+ \frac{\sqrt{3}}{2}V_m.cos^2\theta.\left(\Delta\theta_2 + \Delta\theta_3\right) \tag{9}$$

Equations (5), (6), (8), and (9) indicates that unbalanced in magnitude and phase angle of voltages introduces errors in the $d-q$ component with a double frequency component. This effect of magnitude unbalance is shown in Figures 1(a), 2(a) and 3(a) whereas the effect of phase unbalance is shown in Figures 1(b), 2(b) and 3(b). The magnitude unbalance is realised as 1.10 p.u., 1.15 p.u., and 0.85 p.u. whereas phase unbalance is implemented with $-5°$, $-110°$, and $130°$, for A, B, and C phase respectively.

The comparison shows that how error voltage is produced during unbalanced condition. Purpose of conducting this analysis is to explore how unbalanced voltage condition developed error in $dq0$ components of transformed voltages. This error in $dq0$ component causes an error in Phase Locked Loop (PLL) which further causes an error in the synchronisation of DER with the grid and even power transferred from DER to the grid. It also implants, the double frequency component in the system which may propagate to the controllers. A $d-q$ transform is a widely used technique in the power electronic converters for controlling their operation. This operation is regulated through PLL. Synchronisation of these converters also carried out through PLL. Error in $d-q$ component voltages also affects the PI controller operation. The ideal frequency response of the PI controller appears at zero frequency [23]. If the reference signal contains an alternating component of a fundamental frequency, then it produces a steady state error which increases with frequency. During unbalanced
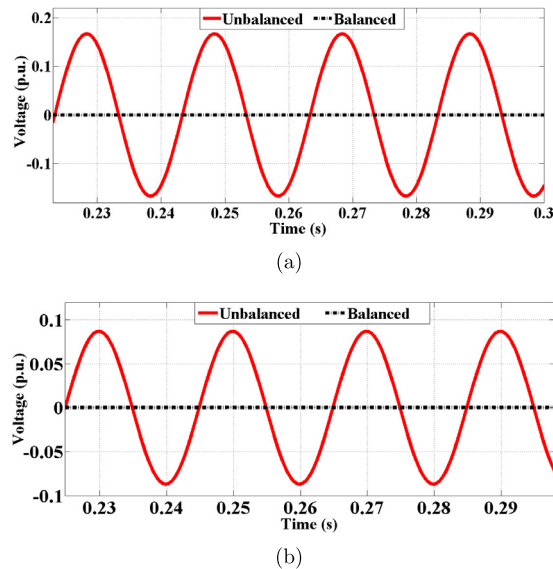
Figure 3. Zero axis voltage under (a) Magnitude unbalance, (b) Phase unbalance.

operation, $d - q$ component voltages generate a sinusoidal signal of a fundamental and double frequency component, thus provides an error in PI controller operation. Controller with less bandwidth design makes the system unstable.

3.3. Impact of UbSVC on MG operation

MG is the cluster of DERs and energy storage systems with local load operated in a grid-connected mode and islanded mode of operation. During grid-connected mode MG operates in a current control mode injecting power into the grid. The grid itself acts as a stiff source maintains the voltage constant. MG operates in island mode only during grid disturbance or fault condition. During this period, it operates in a voltage control mode supplies just power to the local load. Standalone MG operates without any grid connectivity. During this state, DER behaves like grid connected MG at the micro level. MG with comparatively stiffest source operates under voltage control mode, whereas other minor sources inject the power works in the current control mode. Figure 4 shows the general architecture of standalone MG.

DG set is considered as the most reliable source compared to other DER, thus acts like comparatively stiff source maintains the MG voltage whereas another DER operates in a current control mode injects the power into MG. This structure is realised in a simplified form as shown in Figure 5 for analysis. It consists of two sources one shown as a DER_1 who operated in constant voltage mode and DER_2 operated in a current control mode assuming a master-slave configuration. DER_1 source is assumed as a Diesel Generator (DG). Due to limited short circuit capacity, DG set has a stability problem under unbalanced and harmonic environment. For
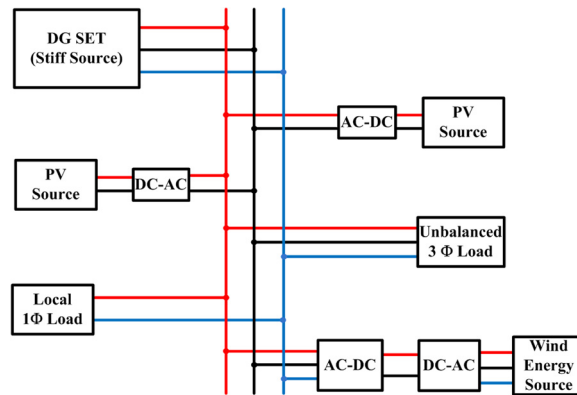
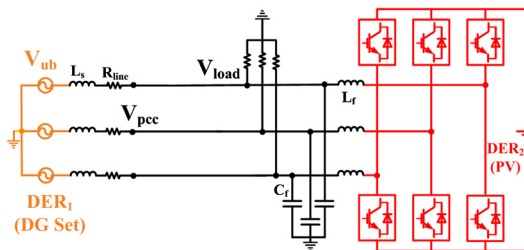**Figure 4.** General architecture of standalone microgrid.

Figure 5. Schematic of standalone microgrid.

simplicity of network and to focused on compensator, controller part is not shown in the diagram.

The error produced in a $d - q$ component of voltages due to unbalanced voltages as discussed in Section 3.1 and 3.2, is analysed by considering standalone MG as shown in Figure 5. Unbalanced voltage is modelled in SG output magnitude and phase form. Magnitude unbalance realised as 1.10, 1.15, and 0.85 pu respectively. Phase form unbalance accomplished as $-5°$, $-110°$, and $130°$, for *A*, *B*, and *C* phase respectively. Active power supplied from the PV source reduces to 600 W from 744 W during magnitude unbalance whereas it remains same during phase unbalance except initial transient as shown in Figure 6. Similar response observed during reactive power transfer as shown in Figure 7. This is because active and reactive power depends upon the $d - q$ components of voltage and current. The error produced in $d - q$ components due to unbalanced voltages also result in an error in the $d - q$ component of current thus affects the power transfer.

Unbalanced voltage not only affects the power transfer from the DER but also delays the synchronisation of minor DER with a major source. This delay happened due to the error, in a $d - q$ component of voltages due to unbalance. A synchronisation process carried out through PLL in which an error signal is formed by subtracting with *q*-component voltages with zero as a reference voltage. This error signal is reduced to zero through a PLL filter and tracks the phase angle of the voltage. PI
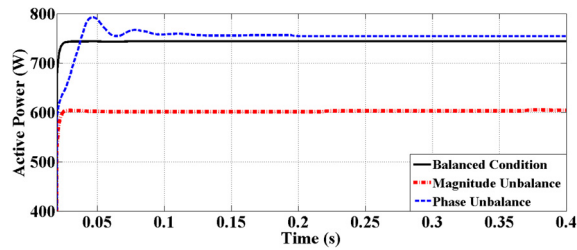
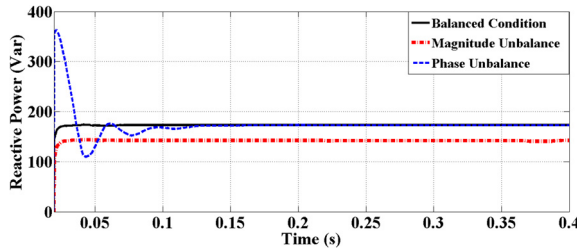**Figure 6.** Active power supplied from DER.

Figure 7. Reactive power supplied from DER.

controller is used as a PLL filter to nullify the error signal. PI controller produces a steady-state error for the input voltage with frequency. This steady-state error generates an error in tracking phase angle, thus delay the synchronisation. This effect is investigated by simulating a three-phase fault at PCC at 0.3 s and restored the system at 0.7 s. As shown in Figure 8, magnitude unbalance produced a delay in re-closing of switch compared to phase unbalance. This way it also affects the stability of the system which concludes that magnitude unbalance causes a severe effect on the power transfer and synchronisation of DER in standalone MG.
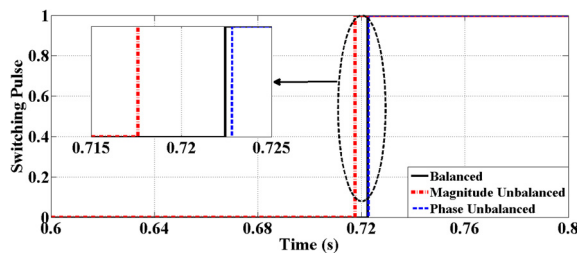

Figure 8. Closing instant of PCC switch.

4. Model

The proposed compensation technique is based on the schematic as shown in Figure 9 in which compensation is provided through a compensating transformer which is energised through a compensator to inject the voltage required to compensate unbalance. Compensator comprises of an inverter which is supplied from any DER like PV with excess capacity is utilised here for a compensation purpose thus,
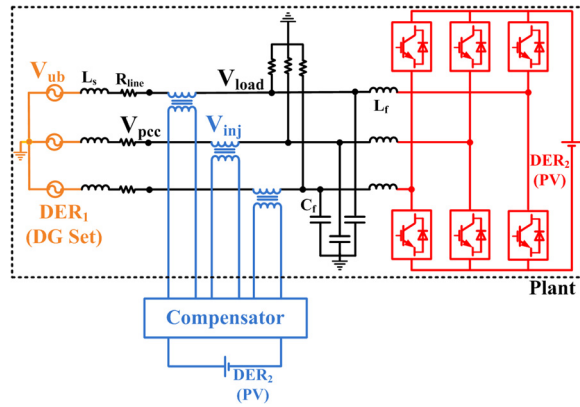
Figure 9. Standalone microgrid with compensator.

the provision of an additional source is avoided. In this paper, two algorithms are proposed to compensate under UbSVC and are given as a) Positive Sequence Component based and b) Dynamic Phasor based.

4.1. Positive Sequence Component (PSC) based compensator

An algorithm to compensate unbalanced voltage in standalone MG is as shown in the Figure 10. In this technique, unbalanced voltage is expressed in the form of symmetrical components. A $dq0$ transformation of unbalanced voltage and positive symmetrical component are compared to produce an error signal which is reconverted into a rotating frame and acts as a reference signal for PWM generation for the switching of compensating inverter. Based on the error between unbalanced voltage and positive sequence voltage, it injects the compensating voltage at the PCC so that the resultant load voltage gets balanced. V^{ref} is the constant corresponds to the peak value of the rated phase voltage. This three-phase unbalanced voltage can be expressed as a positive symmetrical component as given in (10)

$$\begin{bmatrix} V_a^+ \\ V_b^+ \\ V_c^+ \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{10}$$

This positive sequence voltage and three phase unbalanced voltage is transformed into a rotating frame as given by (11) and (12) respectively.

$$\begin{bmatrix} V_d^{ub} \\ V_q^{ub} \\ V_z^{ub} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ -sin\theta & -sin\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a^{ub} \\ V_b^{ub} \\ V_c^{ub} \end{bmatrix} \tag{11}$$
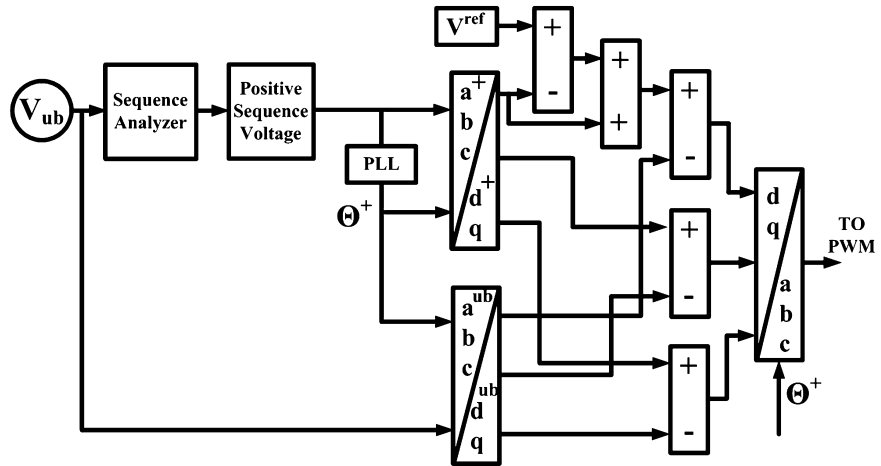
Figure 10. Symmetrical component based compensator.

$$
\begin{bmatrix} V_d^+ \\ V_q^+ \\ V_z^+ \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ -sin\theta & -sin\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a^+ \\ V_b^+ \\ V_c^+ \end{bmatrix} \tag{12}
$$

Subtracting (11) from (12) to get the error signal as shown in (13)

$$
\begin{bmatrix} V_d^+ \\ V_q^+ \\ V_z^+ \end{bmatrix} - \begin{bmatrix} V_d^{ub} \\ V_q^{ub} \\ V_z^{ub} \end{bmatrix} = \begin{bmatrix} V_d^{err} \\ V_q^{err} \\ V_z^{err} \end{bmatrix} \tag{13}
$$

This error voltage is transformed into three-phase abc as given in (14)

$$
\begin{bmatrix} V_a^{err} \\ V_b^{err} \\ V_c^{err} \end{bmatrix} = \begin{bmatrix} cos\theta & -sin\theta & 1 \\ cos\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ cos\left(\theta + \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} V_d^{err} \\ V_q^{err} \\ V_z^{err} \end{bmatrix} \tag{14}
$$

Thus, a voltage to be implanted is generated through a single phase inverter is given as (15) where 'm' is the modulation index and V_{dc} is the input voltage of the inverter. Three single phase inverter gives the independent control of compensation. This injected voltage acts as a primary voltage of the compensating transformer.

$$
V_{inj}^{abc} = m^{abc} \cdot \left(\frac{V_{dc}}{2}\right) \tag{15}
$$

4.2. Dynamic phasor based compensater

4.2.1. Dynamic phasor approach

Any complex time domain waveform $x(\tau)$ is approximated in the interval of $(t - T, t)$ with a Fourier series representation as given by (16) where, $\omega_s = \frac{2\pi}{T}$, T is the length of moving window and $X_k(t)$ is the kth time-varying coefficient in complex form and termed as "Dynamic Phasor". It is defined as,

$$
\begin{aligned}
X_k(t) &= \frac{1}{T} \int_t^{t-T} x(\tau) e^{-jk\omega_s \tau} d\tau \\
&= \frac{1}{T} \int_t^{t-T} x(\tau) \left(\cos\left(k\omega_s t\right) - j \sin\left(k\omega_s t\right) \right) = \langle x \rangle_k
\end{aligned}
\tag{16}
$$

The selected set of DPs, or N with, defines the approximation accuracy of the waveform such that $k \in N$. For example, for DC variables and signals the index set only includes the component $k = 0$, and for purely sinusoidal waveforms with the window length equal to one period gives $k = 1$. The waveforms with fundamental and higher harmonics, for example, the 3rd harmonic, [24] the index set can be chosen at $N = \{1, 3\}$. The addition of more DP index increases the accuracy of the waveform, but reduces the speed of simulation as it increases the complexity of the modelling. It was introduced by [25] and claims that the method is more powerful compared to generalized averaging during small ripple conditions. The author has applied the technique to the series resonant converter and switched mode DC–DC converters. A novel approach has described in [26] to the dynamical modelling of asymmetries in electric machines and polyphase like one with unbalanced supply voltages. Author remarked that dynamic phasors had provided accurate descriptions of transients. The DP modelling technique [24] has been applied to multi-source, multi-frequency systems. The author also proposed a model of varying frequency system and claimed that DP concept is used in almost all types of electric power systems. DP modelling of single-phase inverter is used to analyse [27] the performance of single-phase inverter. Literature interprets that DP modelling is useful for analysing complex network with interconnected devices that operate with a nominal frequency but operate with multiple internal frequencies.

In the $dq0$ reference frame, underbalanced steady-state operation, the electrical quantities have constant values. If the power system is in balanced, the steady-state current contains only the positive sequence component, which is time independent and constant. For balanced operation, the frequency content of the transients will be centred around DC [28], which leads to faster simulation times under balanced conditions, as the variety of variables in the $dq0$ reference frame are much slower

than the original variables in the three-phase ABC reference frame or even constant at steady-state. The $dq0$ transformation is a single reference frame transformation as the reference frame rotates with system frequency. Therefore, the simulations in the $dq0$ reference frame will be efficient around system frequency, which is the case in balanced, symmetrical systems, but if there are unbalanced conditions in the system or other harmonics, this efficiency can decrease drastically. During unbalanced operation due to the presence of negative sequence and zero sequence component, $dq0$ transformation produces a signal which is not stationary but having frequency components along with the stationary signal. This presence double frequency component decreases the speed of simulation. These harmonics with $2\omega_s$, and ω_s during unbalanced condition are inherent to the $dq0$ representation of symmetrical components.

The DP concept is an extension of the frequency-shift phasor in which instead of shifting spectrum by $-\omega_0$ [24], the DP concept is to shift all the band-limited components about $k\omega_0$ by $-k\omega_0$. This results in all harmonics based band components as shown Figure 11. This property allows the DP to handle power system with harmonics more effectively. The DP model represents the system state by a Fourier series expansion over a moving time window. It is based on the generalized averaging technique which uses more terms in the Fourier series to represent more details on the model, thus represent a more accurate model [29]. It has several advantages such as:
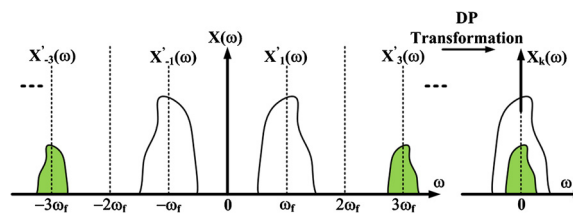

Figure 11. Representation of dynamic phasors from base band signals with higher harmonics.

1. The alternating waveforms of AC networks become constant or moderately-changing in the DP domain, and different frequency components can be handled individually with convenience. This characteristic permits broad step sizes in numerical simulations and makes simulation potentially faster than conventional time-domain models even in unbalanced conditions.

2. As the Performance of PI controller improves in case of slow moving signals, thus a more efficient operation of the PI controller is also possible in the DP domain.

3. Since dynamic phasor X_k are all narrowly banded baseband signals, they can be numerically computed more efficiently.

4. DP provides a platform for power electronic converters to develop a more simplified mathematical form of a model by transforming the switched system into a continuous system.

DP generator is proposed in [29] to transform any AC variable into a dynamic phasor variable as shown in Figure 12 represents the (16) in which T be the time interval of a sliding time window of the integral. DP generator is used for extracting DP variable when x is a function of time. If the model is fully developed in DP then this DP generator is not required. In our topology, we use the DP calculator to convert stationary signals for providing a control signal to the compensator which injects necessary voltage for compensation. As shown in Figure 13 DP based compensator
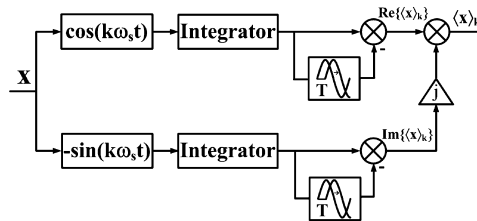

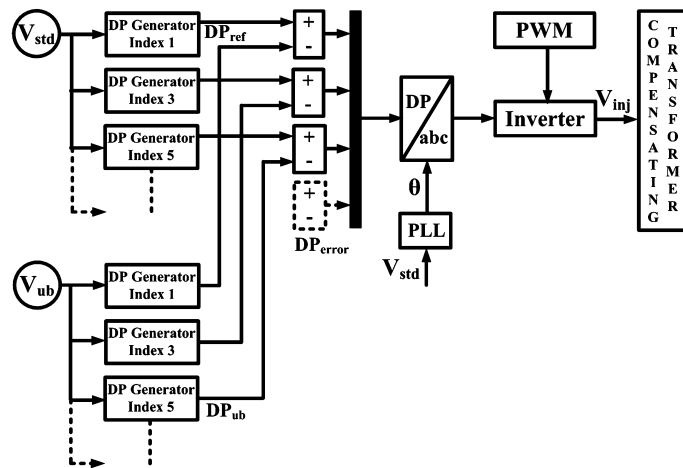**Figure 12.** DP generator [29].

Figure 13. Dynamic phasor based compensator.

consists of DP generator corresponding to as many harmonic orders as a need to eliminate. Selection of higher indices increases the complexity of the system. In our DP formation we used $N = \{1, 3, 5, 7\}$ for better accuracy of the distorted waveform. DP variable for these indices is obtained for both distorted voltage and the standard reference voltage. Variables corresponding to distorted voltage are compared with respective standard voltage variables to generate DP_{error}. Summing all individual DP_{error} and transforming it into a rotating frame produces a control signal for each
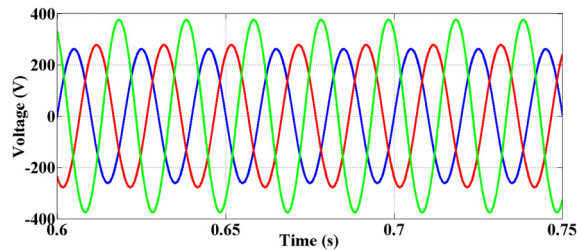
Figure 14. Unbalanced PCC voltage.

single-phase inverter. Thus, depending upon the extent of unbalanced magnitude, voltage is injected into the compensating transformer. This single phase voltage injection provides an advantage of decoupling voltages.

5. Results

Simulation of a network under an UbSVC with harmonic content is carried out in MATLAB/Simulink to analyse the effectiveness of both proposed algorithms, as shown in Figure 9 with parameters, as given in Table 1. The validation of both the

Table 1. Parameters considered for simulation.

Parameter	Value	Parameter	Value
L_s	0.2 mH	R_{line}	0.001 Ω
V_{dc}	325 V	L_f, C_f	0.1 mH, 50 μF

proposed compensator is performed with 80%, 85% and 115% of the rated three phase voltage magnitude having as shown in Figure 14. Voltage Unbalanced Factor (% V_{UbF}) of the PCC voltage is observed as 12%.

5.1. PSC based compensation

The compensated load voltage along by PSC based compensation is as shown in Figure 15a Active power supplied by DER is enhanced to 775 W during PSC based compensation technique as compared to 530 W in an uncompensated case as shown in Figure 15b. The injected voltage supplied by the compensator is as shown in Figure 15c.

5.2. DP based compensation

Load voltage after compensation is as shown in Figure 16a. Active power supplied by DER has enhanced to 765 W during DP based compensation as compared to
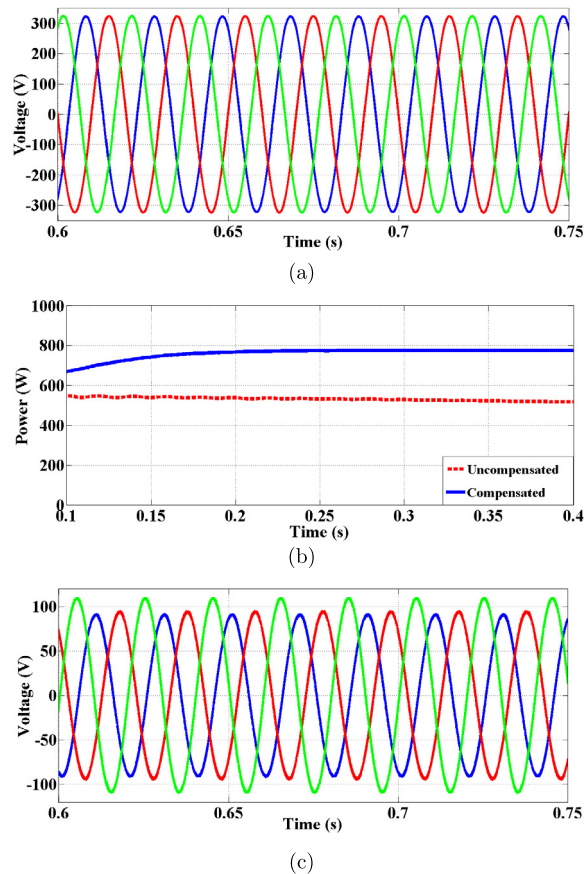
Figure 15. (a) Load voltage and (b) Active power supplied by DER, (c) Injected voltage by compensator during PSC based compensation.

530 W during uncompensated condition as shown in Figure 16b. The injected voltage supplied by the compensator is as shown in Figure 16c.

6. Discussion

The effectiveness of both the compensator is analysed on the basis of Voltage Unbalance Factor ($\%V_{UbF}$) with the methodologies proposed in the literature.

1. The integration of a positive and a negative-sequence SRF-PI controller of inverter output voltage has been proposed in [30]. It has used two pi controller in two rotating reference frames. One of the PI controllers was controlling the positive sequence load current to produce the desired positive sequence voltage and another PI controller was regulating negative sequence current to minimize the unbalanced condition. The method uses an only single inverter with the load to consider unbalanced compensation and observed to be effective, but its
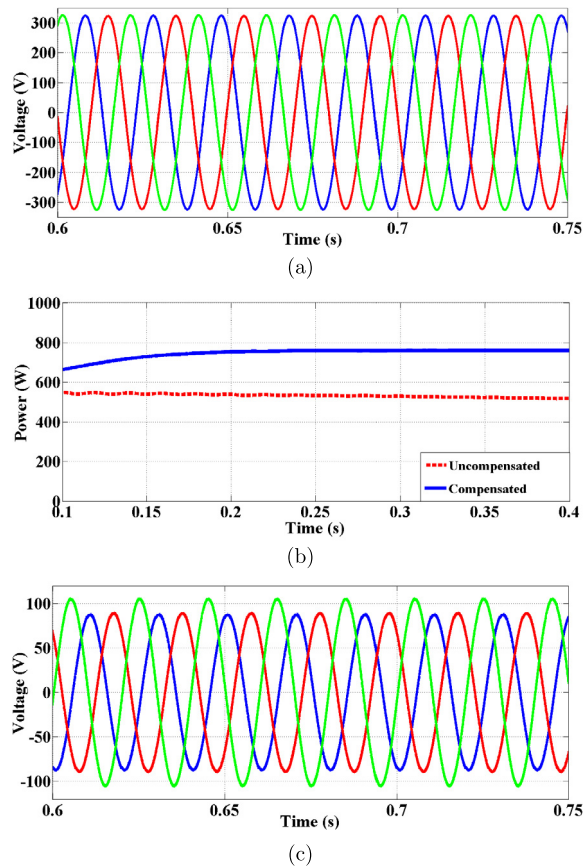
Figure 16. (a) Load voltage and (b) Active power supplied by DER, (c) Injected voltage by compensator during DP based compensation.

applicability in MG environment comprises of an inverter with different control techniques and different DER dynamics not considered in the paper.

2. Negative sequence component voltage and current have been used in [11] to calculate negative sequence reactive power. This negative sequence reactive power is used for generation of a reference signal used for unbalanced compensation. The method is specifically applicable to droop controlled inverters thus its applicability in the case of centralised and multi-layer (hierarchical) control architecture is not discussed in the paper. It is important from the perspective of the increased penetration level of DER where the reliability of decentralised control is drastically reduced.

3. The decentralised $Q^- - G$ droop control has been proposed [9] along with conventional p-f and Q-V droop control. $Q^- - G$ effectively divides the negative-sequence reactive power among the converters, thus optimise the negative sequence voltage and reduces the unbalanced condition in the MG. The method is found to be effective towards DER of different capacities. As the method is based on droop control, thus its applicability in the case of centralised and

multi-layer (hierarchical) control architecture is not discussed in the paper. It is important from the perspective of the increased penetration level of DER where the reliability of decentralised control is drastically reduced.

4. The switched capacitor bank has been proposed [31] to accomplish the desired voltage balancing in an island MG for achieving synchronisation. Switching capacitor banks to enhance voltage unbalance condition is possible only in case of a drop in voltage, but can not be used in case voltage rise condition which is inherent in case unbalanced condition. Switching of capacitor banks also creates switching transients may affect the enhancement of unbalanced condition.

All the methods summarised above have a common limitation about the lacking in harmonic mitigation. Even in case of balanced rated voltage condition with the harmonic presence, they will not be effective. All the methodologies illustrated in the literature were found to be potent towards the restitution of unbalanced condition as they reduced the unbalanced condition, well below the required standards as discussed in Table 2. However, the loading of converters also affect the effectiveness, but not considered here to maintain simplicity in comparison.

Table 2. Comparisons between various voltage unbalance compensation techniques.

Details	Technique used for compensation	$\%V_{UbF}$
Literature 1 [30]	SRF-PI controller	1.21
Literature 2 [11]	$Q^- - G$ droop control	0.7
Literature 3 [9]	Stationary frame control	1.57
Literature 4 [31]	Switched capacitor control	1.85
Proposed compensator 1	Positive sequence component based	0.1
Proposed compensator 2	Dynamic phasor based	0.15

7. Experimental

The effectiveness of the proposed compensator is validated by running the MG model on Opal-RT and compensator on dSPACE.

7.1. Real time hardware-in-loop implementation

The proposed system is realised based on the RT-LAB environment of Opal-RT, using RT toolbox and dSPACE environment in MATLAB/Simulink. The detailed architecture of the HIL system [32] used to corroborate the PSC based compensator and DP based compensator is depicted in Figure 17. On HIL platforms, the plant (refer Figure 9) was deployed in Opal-RT module OP4500 and compensator was in dSPACE DS1104. The RT-LAB simulator has two 3.33-GHz cores dedicated for
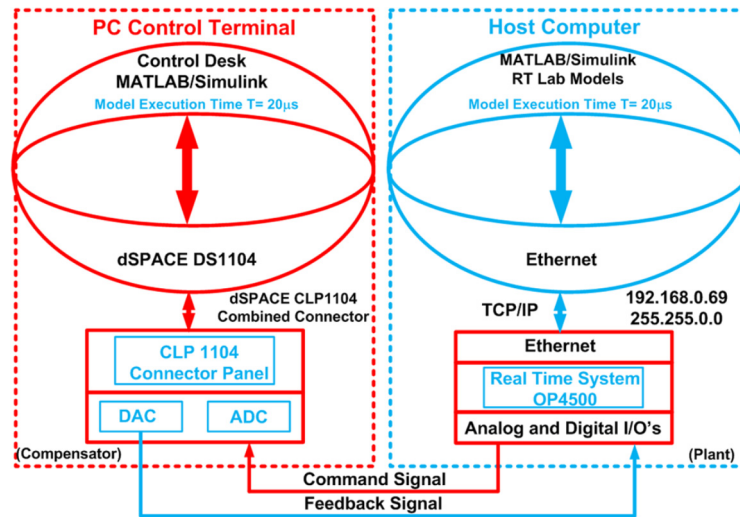
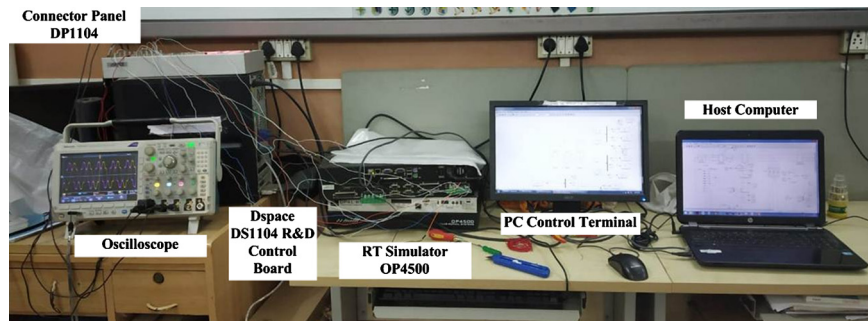**Figure 17.** Opal-RT HIL architecture.

Figure 18. HIL experimental set-up.

parallel computation. The Red Hat Linux operating system based targets is controlled through a Windows-based host computer using a TCP/IP connection. The real-time interfacing between OP4500 and DS1104 is handled through 32-Analog and 64-Digital I/Os of OP4500 [33] and DAC and ADC of DS1104. The experimental setup required for HIL interface is demonstrated in Figure 18. The visual clip of the simulation conducted is referred in the section Additional information. The detailed structure of this specific simulation allows for real-time interaction through the general purpose input output (GPIO) of a field-programmable gate array (FPGA) DE2 board, which receives an input voltage at PCC (V_{ub}). The DE2 board computes, the control signal voltage of the compensating inverter in both the compensator respectively. The sampling period of 20 μs gives sufficient time for the DSP to execute the algorithm. The DSP also communicates to the PC running the dSPACE [34] through the dSPACE CLP1104 combined connector.
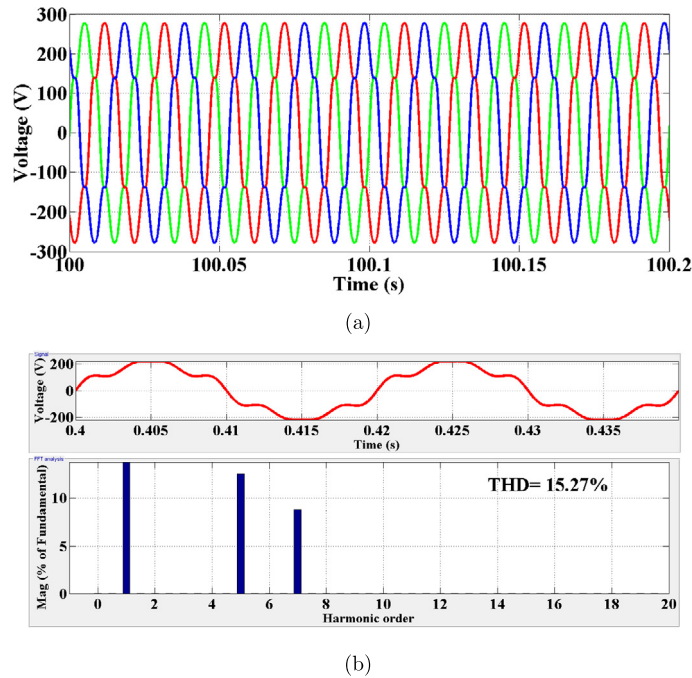
(a)

(b)

Figure 19. HIL results: (a) PCC voltage, (b) FFT analysis of PCC voltage without compensation.

## 7.2. Hardware-in-loop experimental results

The HIL is running in real time under the same parameters as considered for the simulation by building a plant in Opal-RT and compensator in dSPACE. In order to scrutinise the clout of both the compensator towards harmonics mitigation, the source voltage of unbalanced voltage 80% rated voltage in magnitude, 12.5% of the 5th harmonic and 8.75% of the 7th harmonic component is used as shown in Figure 19a. Total Harmonic Distortion (THD) of the PCC voltage is after conducting an FFT analysis is observed to be well above as 15.27% as shown in Figure 19b.

Load voltage after PSC based compensation is as shown in Figure 20a. FFT analysis of this load voltage as shown in Figure 20b concludes that THD was compensated to 0.17%, which is much below than the standards.

Figure 21a shows the injected voltage by the compensating transformer. Active power of 810 W is injected to the grid during this compensation as shown in Figure 21b. Similarly, Load voltage after DP based compensation is as shown in Figure 22a. FFT analysis of this load voltage as shown in Figure 22b concludes that THD was compensated to 0.11%, which is also much below than the standards. Figure 23a shows the injected voltage by the compensating transformer. Active power of 855 W is injected to the grid during this compensation as shown in
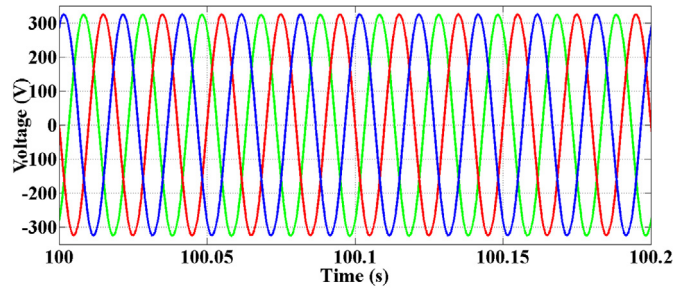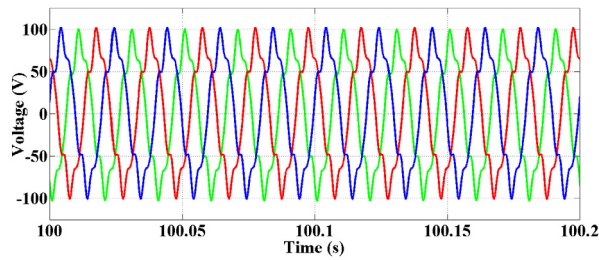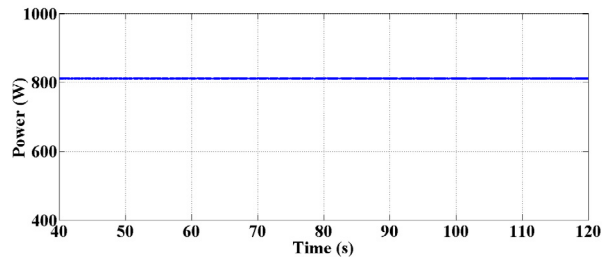
(a)
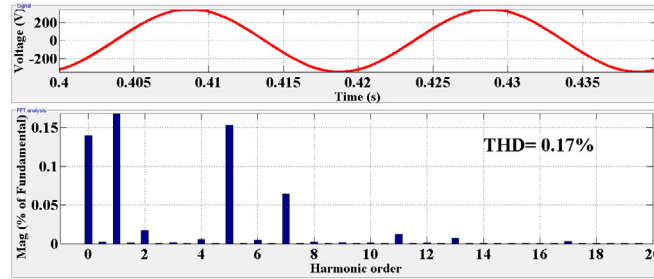
(b)

Figure 20. HIL results for PSC based compensation: (a) Load voltage, (b) FFT analysis of Load voltage.

(a)

(b)

Figure 21. HIL results for PSC based compensation: (a) Injected voltage, (b) Active power supplied by DER.

Figure 23b. Both the methods found to be efficient towards harmonic mitigation to maintain well below the required standards. Active and reactive power observed to be improved in both cases of compensator compared to an uncompensated condition.

This enhancement more precisely potent in the case of DP based compensation due to larger step size sampling in real time environment.
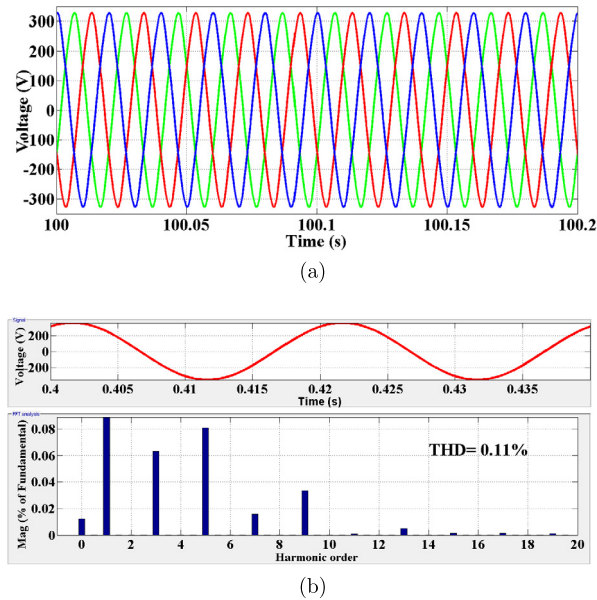

Figure 22. HIL results for DP based compensation: (a) Load voltage, (b) FFT analysis of load voltage.
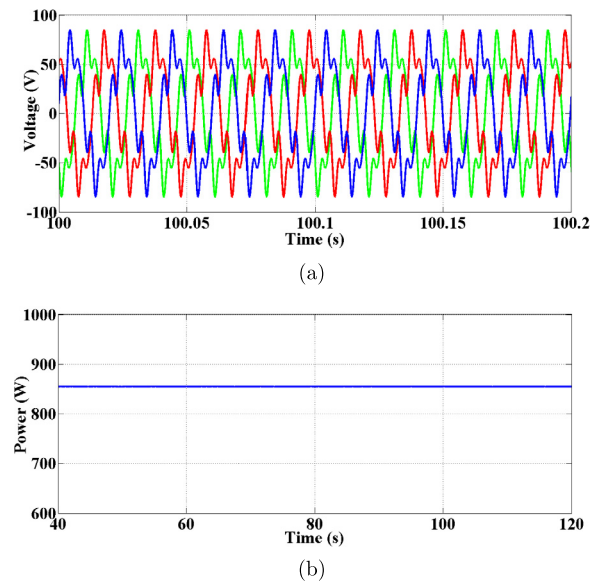

Figure 23. HIL results for DP based compensation: (a) Injected voltage, (b) Active power supplied by DER.

Oscilloscope results are shown in Figures 24 and 25 to support validation of HIL results presented in the paper.

(a)   (b)

Figure 24. Oscilloscope observation of PSC based compensator (a) Load voltage, (b) Injected voltage.

(a)   (b)
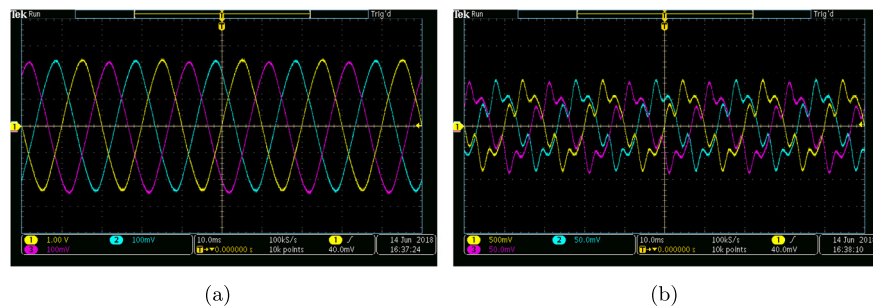
Figure 25. Oscilloscope observation of DP compensator (a) Load voltage, (b) Injected voltage.

8. Conclusions

Impact of UbSVC on the operation of standalone MG is analysed in this paper. A mathematical expression is derived to represent the error in PLL operation. Simulation of PLL operation is carried out as a phase and the magnitude unbalanced condition which validated that deviation is produced dq component causes anomaly in PLL operation. This error also causes a deviation in the synchronizing of DER with the major source. It was observed that it also reduces the power transferred from the DER. PSC based and DP based Compensator is proposed to mitigate this problem. Simulation concluded that 46% enhancement in power transferred from DER is observed in the case of PSC based compensation in comparison to 44% in the case of DP based compensation along with load voltage compensation. The effectiveness of both the compensator observed in terms of $\%V_{UbF}$ as 0.1% and 0.15% respectively from 12%. The effectiveness of both compensator towards harmonic mitigation is validated through experimental results exhibit validated the performance of the proposed compensator to mitigate the harmonics. It is endorsed in the HIL structure using Opal-RT and dSPACE. Both the compensator results are in close vicinity to each other and well below the required permissible limit.

Declarations

Author contribution statement

Mahendra Rane: Conceived and designed the experiments; Performed the experiments; Analyzed and interpreted the data; Wrote the paper.

Sushama Wagh: Contributed reagents, materials, analysis tools or data.

Competing interest statement

The authors declare no conflict of interest.

Additional information

Supplementary content related to this article has been published online at https://doi.org/10.1016/j.heliyon.2019.e01178.

References

[1] J.G. Nielsen, F. Blaabjerg, A detailed comparison of system topologies for dynamic voltage restorers, IEEE Trans. Ind. Appl. 41 (5) (2005) 1272–1280.

[2] B. Wang, G. Venkataramanan, Dynamic voltage restorer utilizing a matrix converter and flywheel energy storage, IEEE Trans. Ind. Appl. 45 (1) (2009) 222–231.

[3] h. Al-Hadidi, A. Gole, D. Jacobson, A novel configuration for a cascade inverter based dynamic voltage restorer with reduced energy storage requirements, in: 2008 IEEE Power and Energy Society General Meeting – Conversion and Delivery of Electrical Energy in the 21st Century, 2008, p. 1.

[4] A.K. Ramasamy, R.K. Iyer, V.K. Ramachandaramuthy, R.N. Mukerjee, Dynamic voltage restorer for voltage sag compensation, in: 2005 International

Conference on Power Electronics and Drives Systems, vol. 2, 2005, pp. 1289–1294.

[5] E. Babaei, M.F. Kangarlu, M. Sabahi, Mitigation of voltage disturbances using dynamic voltage restorer based on direct converters, IEEE Trans. Power Deliv. 25 (4) (2010) 2676–2683.

[6] M.K. Mishra, A. Ghosh, A. Joshi, H.M. Suryawanshi, A novel method of load compensation under unbalanced and distorted voltages, IEEE Trans. Power Deliv. 22 (1) (2007) 288–295.

[7] C. Xu, K. Dai, X. Chen, Y. Kang, Unbalanced PCC voltage regulation with positive- and negative-sequence compensation tactics for MMC-DSTATCOM, IET Power Electron. 9 (15) (2016) 2846–2858.

[8] M. Hojo, Y. Iwase, T. Funabashi, Y. Ueda, A method of three-phase balancing in microgrid by photovoltaic generation systems, in: 2008 13th International Power Electronics and Motion Control Conference, 2008, pp. 2487–2491.

[9] P. Cheng, C. Chen, T. Lee, S. Kuo, A cooperative imbalance compensation method for distributed-generation interface converters, IEEE Trans. Ind. Appl. 45 (2) (2009) 805–815.

[10] T. Wang, H. Nian, Z.Q. Zhu, H. Huang, X. Huang, Flexible PCC voltage unbalance compensation strategy for autonomous operation of parallel DFIGs, IEEE Trans. Ind. Appl. 53 (5) (2017) 4807–4820.

[11] M. Savaghebi, A. Jalilian, J.C. Vasquez, J.M. Guerrero, Autonomous voltage unbalance compensation in an islanded droop-controlled microgrid, IEEE Trans. Ind. Electron. 60 (4) (2013) 1390–1402.

[12] N.R. Merritt, C. Chakraborty, P. Bajpai, New voltage control strategies for VSC-based DG units in an unbalanced microgrid, IEEE Trans. Sustain. Energy 8 (3) (2017) 1127–1139.

[13] M. Savaghebi, Q. Shafiee, J.C. Vasquez, J.M. Guerrero, Adaptive virtual impedance scheme for selective compensation of voltage unbalance and harmonics in microgrids, in: 2015 IEEE Power Energy Society General Meeting, 2015, pp. 1–5.

[14] Y. Han, P. Shen, X. Zhao, J.M. Guerrero, An enhanced power sharing scheme for voltage unbalance and harmonics compensation in an islanded ac microgrid, IEEE Trans. Energy Convers. 31 (3) (2016) 1037–1050.

[15] S.F. Eilaghi, A. Ahmadian, M.A. Golkar, Optimal voltage unbalance compensation in a microgrid using PSO algorithm, in: 2016 IEEE 7th Power India International Conference, PIICON, 2016, pp. 1–6.

[16] M. Rane, S. Wagh, Stability enhancement of transformered PV system using inrush mitigation techniques, in: 2017 North American Power Symposium, NAPS, 2017, pp. 1–6.

[17] IEEE Standard Test Procedure for Polyphase Induction Motors and Generators, IEEE Std 112-2017 (Revision of IEEE Std 112-2004), 2018, pp. 1–115.

[18] A. von Jouanne, B. Banerjee, Assessment of voltage unbalance, IEEE Trans. Power Deliv. 16 (4) (2001) 782–790.

[19] A.I. Maswood, G. Joos, P.D. Ziogas, J.F. Lindsey, Problems and solutions associated with the operation of phase-controlled rectifiers under unbalanced input voltage conditions, IEEE Trans. Ind. Appl. 27 (4) (1991) 765–772.

[20] P. Pillay, M. Manyage, California electricity situation, IEEE Power Eng. Rev. 21 (5) (2001) 10–12.

[21] A.K. Singh, G.K. Singh, R. Mitra, Some observations on definitions of voltage unbalance, in: 2007 39th North American Power Symposium, 2007, pp. 473–479.

[22] J. Driesen, T. Van Craenenbroeck, Voltage disturbances: introduction to unbalance, Power Quality Application Guide, Copper Development Association 5 (3).

[23] S. Bacha, I. Munteanu, A.I. Bratcu, et al., Power Electronic Converters Modeling and Control, Advanced Textbooks in Control and Signal Processing, 2014, p. 454.

[24] T. Yang, S. Bozhko, G. Asher, Multi-generator system modelling based on dynamic phasor concept, in: 2013 15th European Conference on Power Electronics and Applications, EPE, 2013, pp. 1–10.

[25] S.R. Sanders, J.M. Noworolski, X.Z. Liu, G.C. Verghese, Generalized averaging method for power conversion circuits, IEEE Trans. Power Electron. 6 (2) (1991) 251–259.

[26] A.M. Stankovic, S.R. Sanders, T. Aydin, Dynamic phasors in modeling and analysis of unbalanced polyphase ac machines, IEEE Trans. Energy Convers. 17 (1) (2002) 107–113.

[27] A. Coronado-Mendoza, M.A. Pérez-Cisneros, J.A. Domínguez-Navarro, V. Osuna-Enciso, V. Zúñiga-Grajeda, K.J. Gurubel-Tun, Dynamic phasors modeling for a single phase two stage inverter, Electr. Power Syst. Res. 140 (2016) 854–865.

[28] T. Demiray, Simulation of Power System Dynamics Using Dynamic Phasor Models, Ph.D. thesis, ETH, Zurich, 2008.

[29] T. Yang, Development of Dynamic Phasors for the Modelling of Aircraft Electrical Power Systems, Ph.D. thesis, University of Nottingham, 2013, http://eprints.nottingham.ac.uk/13548/1/PhD_Thesis_Final.pdf.

[30] P. Hsu, M. Behnke, A three-phase synchronous frame controller for unbalanced load [invertor operation], in: PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference, Cat. No.98CH36196, vol. 2, 1998, pp. 1369–1374.

[31] N. Lidula, A. Rajapakse, Voltage balancing and synchronization of microgrids with highly unbalanced loads, Renew. Sustain. Energy Rev. 31 (2014) 907–920.

[32] R.V. Meshram, M. Bhagwat, S. Khade, S.R. Wagh, A.M. Stanković, N.M. Singh, Port-controlled phasor hamiltonian modeling and IDA-PBC control of solid-state transformer, IEEE Trans. Control Syst. Technol. 27 (1) (2019) 161–174.

[33] OPAL-RT Technologies Inc., OP4500 RT-LAB-RCP/HIL system user guide, 2015 [Online]. Available: http://www.opal-rt.com. (Accessed 21 April 2018).

[34] DS1104 R&D Controller Board [Online]. Available: https://www.dspace.com/shared/data/pdf/2018/dSPACE_DS1104_Catalog2018.pdf. (Accessed 22 April 2018).