

## Article

# Concurrent-Mode CMOS Detector IC for Sub-Terahertz Imaging System

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**Abstract:** A CMOS detector with a concurrent mode for high-quality images in the sub-terahertz region has been proposed. The detector improves output-signal coupling characteristics at the output node. A cross-coupling capacitor is added to isolate the DC bias between the drain and gate. The detector is designed to combine a 180° phase shift based on common source operation and an in-phase output signal based on the drain input. The circuit layout and phase shift occurring in the cross-coupled capacitor during phase coupling are verified using an EM simulation. The detector is fabricated using the TSMC 0.25- $\mu\text{m}$  mixed-signal 1-poly 5-metal layer CMOS process, where the size, including the pad, is 1.13 mm  $\times$  0.74 mm. The detector IC comprises a folded dipole antenna, the proposed detector, a preamplifier, and a voltage buffer. Measurement results using a 200-GHz gyrotron source demonstrate that the proposed detector voltage responsivity is 14.13 MV/W with a noise-equivalent power of 34.42 pW/ $\sqrt{\text{Hz}}$ . The high detection performance helps resolve the 2-mm line width. The proposed detector exhibits a signal-to-noise ratio of 49 dB with regard to the THz imaging performance, which is 9 dB higher than that of the previous CMOS detector core circuits with gate-drain capacitors.



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**Keywords:** CMOS detector; concurrent-mode; differential detector IC; imaging SNR; integrated folded-dipole antenna; sub-terahertz imaging; voltage responsivity

## 1. Introduction

Terahertz (THz) waves represent frequencies of the 0.1–10 THz bands of the frequency spectrum. Located between radio and light waves, THz waves with high transmittance and directivity are expected to be widely used in the fields of security imaging, radio astronomy, medical imaging, and art [1–7]. A THz imaging system is capable of nondestructive inspection owing to the low ionization energy with regard to frequency. In recent times, the THz wave has been of interest as a frequency resource to replace the millimeter wave, as it can be used in communication beyond the limit of short-wavelength waves [8].

Unlike millimeter wave infrastructure, an active full-wave structure is required to develop a safe and high-resolution THz imaging system. The performance of an active system can be expressed by the signal-to-noise ratio (SNR), in which a measurement target is independently placed between a transmitter and a receiver, and the receiver detects and outputs the signal reflected or transmitted from the target. The SNR of the image quality factor can be calculated as the ratio between the output signals when the transmitted signal is reflected away by a metal target and when the transmitted signal passes through a nonreflective target; the reflected transmission output measures the noise of the detector. The image quality of the output can be measured using high-power sources; however, the implementation of the high-powered transmitter at the THz frequency band is difficult and expensive to fabricate. A receiver with high sensitivity characteristics improves the

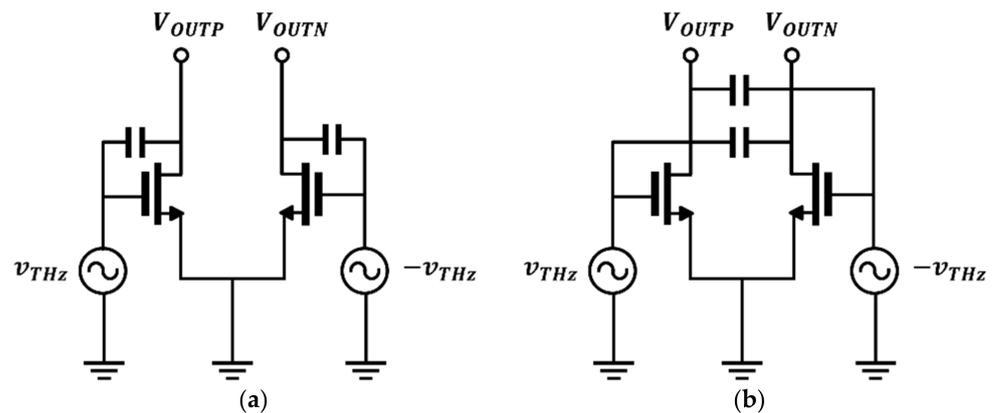
performance of an imaging system. The sensitivity of the receiver is measured based on voltage responsivity ( $R_V$ ) and noise-equivalent power ( $NEP$ ).  $R_V$  represents the output voltage magnitude as a function of the input signal power, and  $NEP$  demonstrates the noise characteristics of the detector. A receiver with low  $NEP$  exhibits a smaller power threshold to distinguish between signal and noise, allowing for more sensitive operation. High  $R_V$  detectors can minimize  $NEP$ , resulting in high performance [9].

The surface plasma phenomenon of field-effect transistors, which was first introduced by M. Dyakonov and M. Shur, exhibited potential for sensing in the THz band using a standard complementary metal-oxide-semiconductor (CMOS) process [10,11]. A CMOS detector capable of detecting a signal above the operating frequency is known as a self-mixing detector or a square row detector, and outputs a direct current (DC) voltage [12]. Body bias control can modify the electrical characteristics of the detector core to improve the performance by changing the subthreshold slope [13]. In addition, a CMOS detector with body bias control has demonstrated a wide dynamic range with strong voltage responsivity [13]. Detector bias changes the electric field effect of the detector, which requires various operating parameters. Cascode topology allows a detector to operate similar to a general amplifier, where the source, gate, and drain interfaces are simplified, thereby significantly improving the detector performance [14–18]. CMOS detector topologies have been proposed with commonly used gate and drain input structures, where the phase is determined by adding transconductance terms using Taylor expansion [19]. The analysis confirmed that detection performance can be improved based on the differential phase input with drain bias. A detector circuit with weak inversion mode operation characteristics can help improve performance through the phase coupling of the output signal and unbiased drain.

In this study, a concurrent-mode CMOS detector integrated circuit (IC) with phase-coupled operation at the output node with input signals routing through cross-coupled capacitors is proposed. The proposed detector IC comprises a differential-folded dipole antenna, the proposed differential detector core, a pre-amplifier to convert a signal from a differential to single-ended mode, and a voltage buffer with low gain. The performance of the detector can be improved by combining the two signals of the dual detection output in one core circuit; as a result, the proposed IC functions as a high-quality THz imaging system. Section 2 describes the core configuration and operating principle of the CMOS concurrent-mode detector with phase combination. A phase difference occurs between the gate of the input node and the drain of the output node owing to the cross-coupled capacitors. The proposed detector IC was implemented using the TSMC 0.25- $\mu\text{m}$  CMOS 1-poly 5-metal (1P5M) process. Section 3 presents the measurement results of the performance of the detector IC and results obtained using 200-GHz raster-scanned imaging. Section 4 concludes the study.

## 2. Proposed Detector Circuit

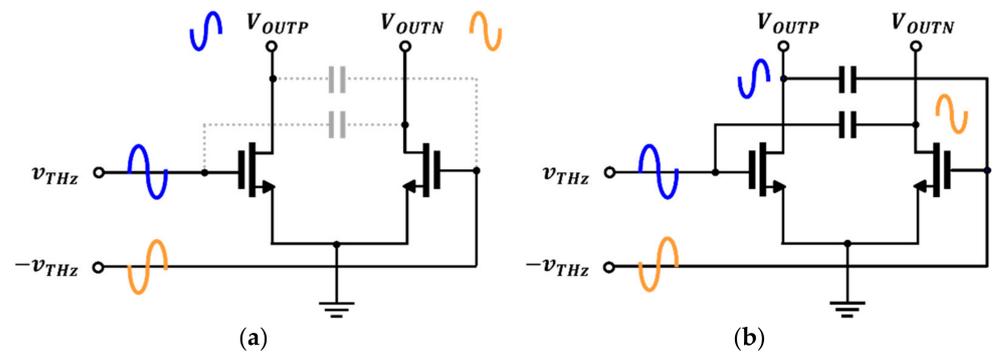
The detector circuit with a gate-drain capacitor used to enhance the potential difference between the drain and source terminals is shown in Figure 1a. Extra gate-drain capacitors are added to a CMOS-based single gate input circuit and exhibit a high potential difference. Despite its high performance, the previous topology is sensitive to the capacitor size, making it difficult to guarantee operational safety. The limitations of the process model and layout used to optimize the capacitor size can prevent the detector from achieving optimal performance. A high-performance concurrent-mode detector circuit with safe operation via cross-coupled structure for dual operation has been proposed.



**Figure 1.** CMOS detector configuration: (a) Previous detector circuit with gate-drain capacitors; (b) proposed concurrent-mode detector.

### 2.1. Proposed Detector Core Configuration

The proposed detector with a concurrent-mode operation circuit, as shown in Figure 1b, improves the quality of the THz imaging system; the circuit operates based on the square root detection of the input power and outputs a voltage signal. The proposed detector consists of the same components as the detector circuit with gate-drain capacitors, except for cross-coupled capacitors. The cross-coupled capacitors were used to transmit the THz signal to the drain of an adjacent detection transistor. Unlike the gate-drain capacitor circuit, which improves the drain-source potential difference, the capacitor blocks the gate input DC bias and only transmits the in-phase signal. The detector structure can be interpreted as a combination of the gate input and drain input circuits. The proposed detector has two operation modes. One of the operation modes of the proposed detector can be analyzed in the same method as the general common-source stage amplifier shown in Figure 2a. The output signal is inverted from the input signal, with a  $180^\circ$  difference.

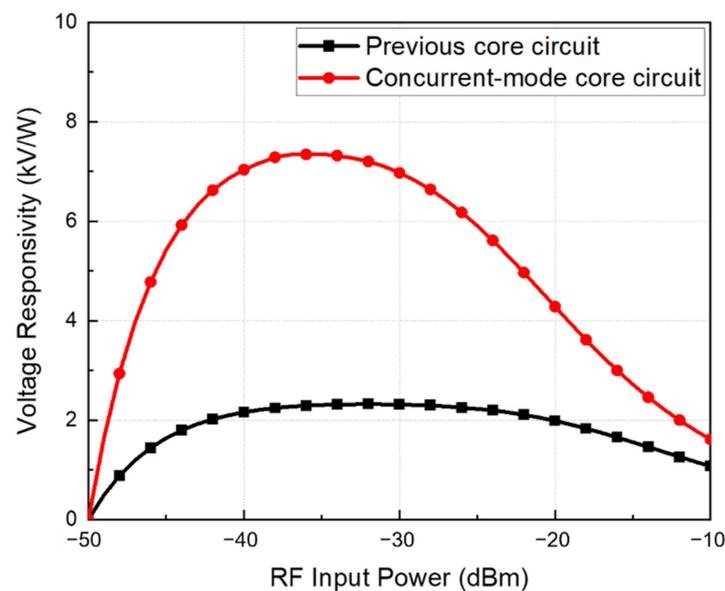


**Figure 2.** Two operations in the proposed circuit: (a) gate input topology; (b) drain input topology.

Figure 2b shows drain input detection operation using cross capacitors connected to the drain nodes of the two transistors. The output signal of the drain input circuit exhibits the same phase as the gate input without any phase shift and is, therefore, phase-coupled to the output drain terminal. Both detector inputs include gate bias for weak inversion operation at the gate node. The operating principle of the proposed detector is defined as the concurrent-mode operation, in which an incident signal is simultaneously applied to the gate and drain of the single detector core. The concurrent-mode operating characteristics are designed using cross-coupling capacitors; a sufficient capacitance is required for high-frequency coupling. The same phase at the final output node is important for combining the two detector outputs. The proposed detector circuit was designed to incorporate the cross-coupled capacitor layout and additional core circuit phase shifts and

was validated using electromagnetic simulation performed using the Keysight Advanced Design System software.

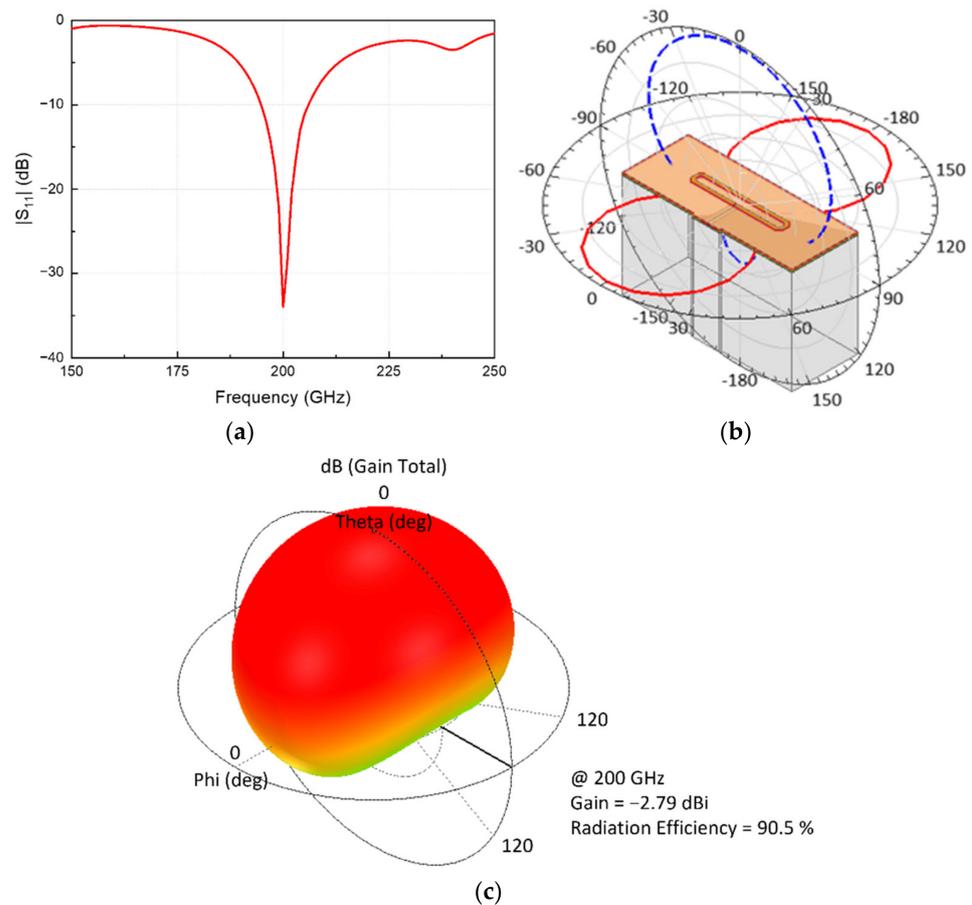
The performance of the two detector cores, as shown in Figure 1, was simulated using Cadence Spectre. Although achieving the impedance-matching condition is essential for optimizing detector characteristics, two detector cores were used as transistors of the same size to compare the performance based on the detector configuration. Figure 3 shows the simulated voltage responsivities between the previous and proposed detector cores. The proposed concurrent-mode detector core exhibited a voltage responsivity of 1.5–3.3 times higher than that of the previous detector core based on the input power. The performance improvement owing to phase coupling is confirmed above the power level at which the two detection operation outputs are significant. However, beyond a certain power level, a sufficiently large power signal is incident on the gate node, and the output of the gate input circuit becomes dominant, decreasing the performance difference.



**Figure 3.** Simulated voltage responsivity of the detector core with gate-drain capacitors and the proposed concurrent-mode detector core.

## 2.2. Folded Dipole Antenna

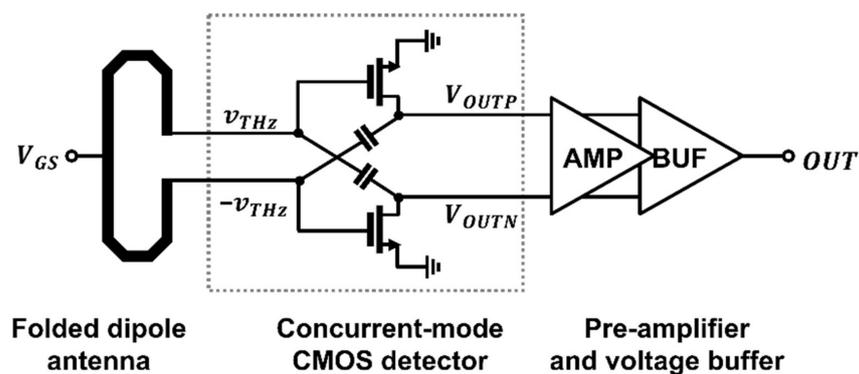
A non-frequency selective detection circuit is determined for operating frequencies using an integrated antenna. A differential integrated antenna with an operating frequency of 200 GHz was designed to obtain input signals whose frequencies are higher than the device operating frequency. A grounded guard ring was placed at a sufficient distance from the antenna metal to focus on the internal electric field. The total area of the antenna, including the guard ring, is  $500 \mu\text{m} \times 200 \mu\text{m}$ . Compared with a patch antenna, the proposed antenna has a smaller area and exhibits similar performance, which is advantageous for a large-scale array. The on-chip antenna was configured as a folded dipole antenna to assume the operational mode of the detector circuit by applying a gate bias through a virtual ground. The radiating metal was folded at  $45^\circ$  to balance the paths of the inner and outer lengths. Chamfered radiating metal edges can prevent distortion from the antenna owing to processing changes. The simulation results using the 3-D EM simulation tool, ANSYS Electronics, demonstrate 11 GHz of  $-10$  dB bandwidth corresponding to 195–206 GHz, as depicted in Figure 4a. The simulation data in Figure 4b represent the E-field and H-field characteristics in the far field. As shown in Figure 4c, the antenna radiation gain is simulated at  $-2.79$  dBi at 200 GHz, exhibiting a peak radiation efficiency of 90.5%. In the far field, the simulated data confirm that the antenna performance is omnidirectional and suitable for image measurement.



**Figure 4.** Simulation results of the integrated folded dipole antenna: (a) reflection coefficient  $|S_{11}|$ ; (b) far-field radiation pattern at 200 GHz; (c) 3D radiation pattern at 200 GHz.

### 2.3. CMOS Detector IC Implementation

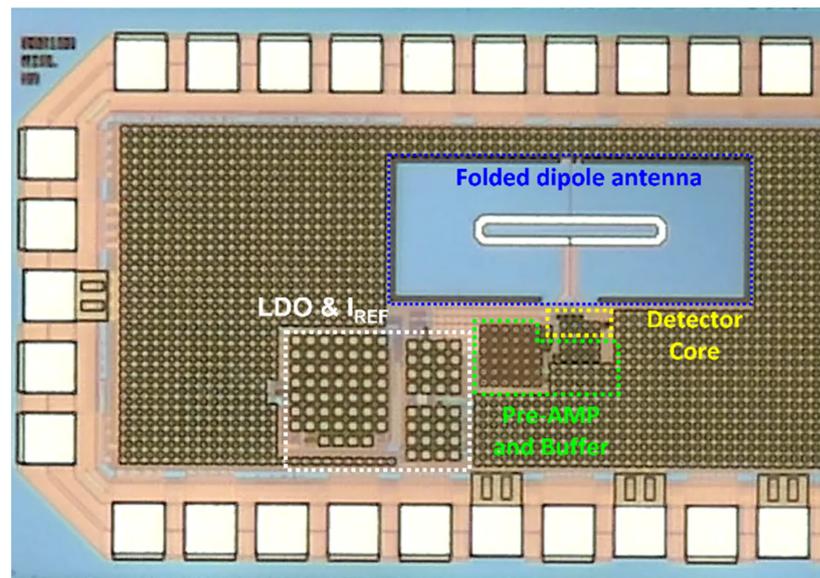
The CMOS detector IC, including the in-phase coupled detector, is illustrated in Figure 5. The final output signal was generated using a differential-to-single-ended preamplifier and monitored using an impedance-converting voltage buffer. A validated preamplifier and voltage buffer used the same circuit to compare the inherent detector core circuits [19].



**Figure 5.** CMOS detector IC comprising a 200-GHz folded dipole antenna, the proposed detector, a differential-to-single-ended preamplifier, and a voltage buffer.

Figure 6 shows the circuit used to monitor the output. Voltages  $V_{B1}$ ,  $V_{B2}$ ,  $V_{B3}$ , and  $V_{B4}$  are biased in the circuit based on a current reference circuit. A common gate transistor, M2, acting as a level shifter and isolator, was used to change the output voltage of the



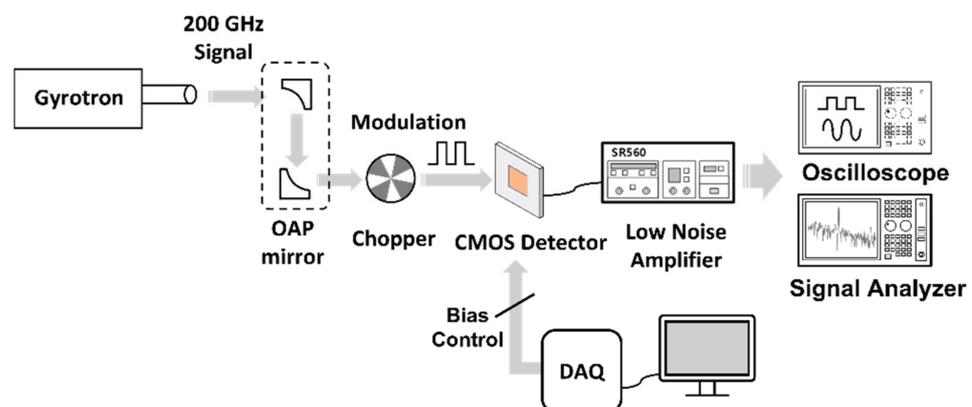


**Figure 7.** Die photograph of the proposed detector IC implemented using the TSMC 0.25- $\mu\text{m}$  mixed-signal CMOS process comprising a 200-GHz folded dipole antenna, the proposed detector core, a pre-amplifier, and a voltage buffer.

### 3. Measurement Results and Discussions

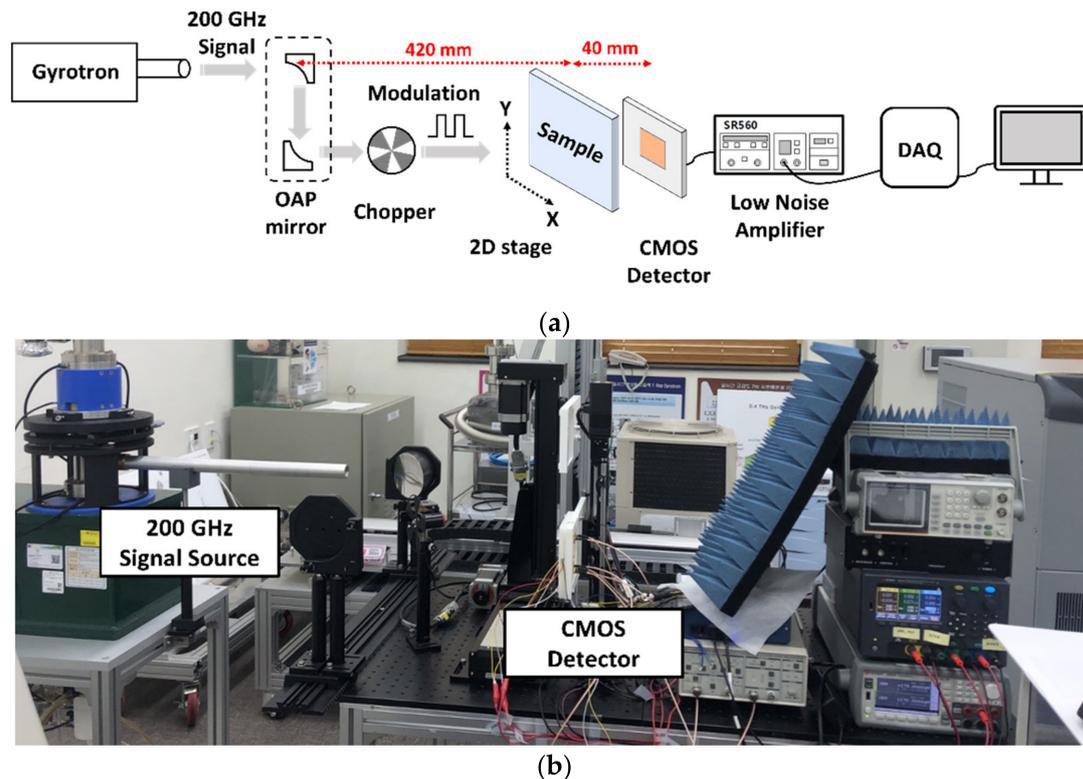
#### 3.1. Measurement Setup

The setup used to measure the performance of the proposed detector is illustrated in Figure 8. The 200-GHz signal generated by the gyrotron source demonstrates Gaussian beam characteristics, whose focal plane is aligned by off-axis parabolic (OAP) mirrors [20] with a focal length of 15.24 cm. A physical chopper located in the focal plane reduces the flicker noise by transmitting the detected output DC voltage along with an AC signal. The measurements were conducted with a modulation frequency of 200 Hz for avoiding the effect of switching noise from the power supply. To monitor the constant voltage output of the LDO regulator, digital 4-bit control signals were applied using the National Instruments (NI) data acquisition board (DAQ). Before reaching the monitoring equipment, the detector IC output was amplified with a gain of 5 through a bandpass filter of 100–300 Hz using an SR560 low-noise voltage amplifier manufactured by Stanford Research Systems.  $R_V$  was measured using an oscilloscope, and  $NEP$  was measured using the Keysight N9010B signal analyzer. The unamplified detector performance was measured by dividing the measurement with the amplifier gain.



**Figure 8.** Measurement setup to analyze the performance of the proposed detector IC. An oscilloscope to measure  $R_V$  and a signal analyzer to obtain noise-equivalent power have been used.

In the THz imaging system test, as shown in Figure 9a, the distance between the mirror and the sample was 420 mm, and that between the sample and the proposed CMOS detector IC was 40 mm; the sample was placed on the XY stage. During image acquisition, the DAQ generated a digital 4-bit control code and analyzed the measurement data. The output signals were acquired using the NI DAQ hardware and NI LabVIEW software tools. The sample was moved at intervals of 1 mm in the measurement environment, as shown in Figure 9b, and the final output image was obtained using 2-D raster scanning.



**Figure 9.** Measurement setup: (a) block diagram for THz imaging using raster scanning; (b) experimental setup.

### 3.2. Proposed Detector IC Performance

The performance of sub-THz CMOS detectors is determined by  $R_V$  and  $NEP$ .  $R_V$  is defined as the change in the output voltage based on the presence or absence of the incident signal with the specific power applied to the detector; it is calculated as:

$$R_V = \frac{V_{OUT} - V_{DCOFF}}{P_{IN}} = \frac{V_{OUT} - V_{DCOFF}}{P_D \cdot A_{EFF}} \quad [V/W], \quad (1)$$

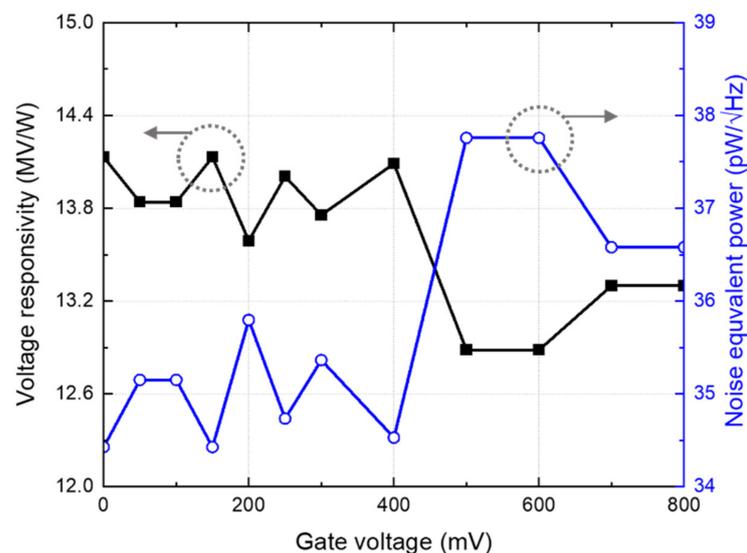
where  $V_{OUT}$  is the output voltage when the input power  $P_{IN}$  is applied to the detector,  $V_{DCOFF}$  is the output voltage without the incident signal,  $P_D$  is the power density incident to the detector IC, and  $A_{EFF}$  is the effective antenna area, which includes the integrated antenna and wavelength characteristics [9,13].  $NEP$  is defined as the input power level that becomes equal to the noise generated from the detector itself; it is expressed using  $R_V$  as:

$$NEP = \frac{\sqrt{N_V}}{R_V} \left[ W/\sqrt{Hz} \right], \quad (2)$$

where  $N_V$  denotes the noise spectral density [9].

When using a receiver antenna to transmit a THz signal to a detector, it is vital to determine the characteristics of the detector antenna and consider the input power equation of the detector to accurately analyze and measure the detector performance. The

unit power density of the gyrotron measured at the detector position is  $0.5 \text{ W/m}^2$ , and the effective area considering the receiving antenna gain at 200 GHz is  $9.62 \times 10^{-8} \text{ m}^2$  [13]. The input power was calculated based on the measured performance, considering the difference in antenna gain according to the radiation area and similar antenna simulation values [21]. Figure 10 shows the measured  $R_V$  and  $NEP$  values of the proposed CMOS detector with different gate bias voltages. The results exhibit high  $R_V$  and low noise when the gate bias is lower than the threshold voltage.  $R_V$  and  $NEP$  were 14.13 MV/W and  $34.42 \text{ pW}/\sqrt{\text{Hz}}$ , respectively, under the gate bias condition of 150 mV. Table 1 lists the performance comparison of the proposed CMOS detector with previously developed detector core configurations. The proposed CMOS detector exhibits higher  $R_V$  compared with the other detectors. As a result of comparing detectors with the same minimum gate length, the proposed detector showed the lowest  $NEP$  and highest  $R_V$ . In previous studies, while calculating the effective area of an antenna, the difference in the radiation area between the antenna simulations and measurements was not considered. The performance of the proposed detector was calculated using the simulation data of the integrated antenna, which includes the ground guard ring in the simulation model for providing the same radiation area as the fabricated IC.



**Figure 10.** Measurement results of the voltage responsivity and the noise-equivalent power using the proposed CMOS detector IC at 200 GHz.

**Table 1.** Comparisons of CMOS detector performance.

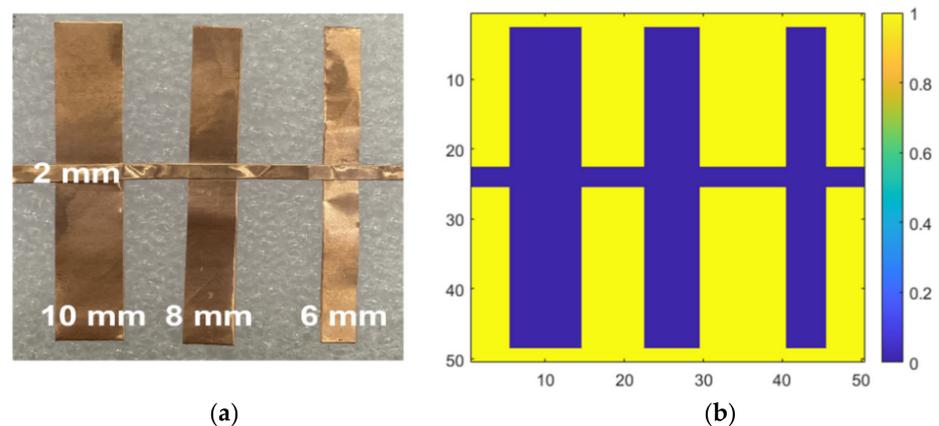
| Ref.       | Process (nm) | Freq. (GHz) | Detector Core Configuration | $R_V$ (kV/W) | $NEP$ ( $\text{pW}/\sqrt{\text{Hz}}$ ) |
|------------|--------------|-------------|-----------------------------|--------------|--|
| [13]       | 250          | 200         | Gate-drain cap.             | 5696         | 62.4                                   |
| [16]       | 65           | 310         | Drain input                 | 2            | $3.5^1$                                |
| [19]       | 250          | 200         | Gate-drain cap.             | 357.1        | 57.3                                   |
| [22]       | 250          | 200         | Gate-drain cap.             | 2020         | 76                                     |
| [23]       | 90           | 365         | Gate source input           | 1200         | 200                                    |
| [24]       | 250          | 200         | Gate-drain cap.             | 2990         | 46.3                                   |
| This works | 250          | 200         | Concurrent-mode             | 14,130       | 34.42                                  |

<sup>1</sup> Measured in a Faraday cage.

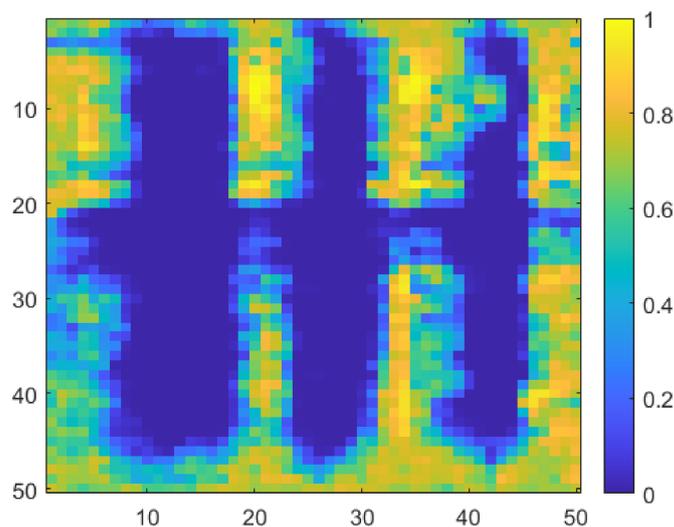
### 3.3. Images Obtained Using the Proposed Detector IC

Copper foil tapes of different thicknesses were placed on the Styrofoam substrate to measure the resolution of the proposed detector, as shown in Figure 11a. The sample size was  $50 \text{ mm} \times 50 \text{ mm}$ . Considering that the wavelength of 200 GHz in the air is 1.5 mm, the sample was manufactured considering a thickness of  $\geq 2 \text{ mm}$ . The real sample

was digitized, as shown in Figure 11b, for a digital area comparison using MATLAB. The sub-THz imaging at 200 GHz yielded results that are 63.6% identical to those of the digitalized sample. As shown in Figure 12, imaging results obtained using the proposed detector demonstrated that a 2-mm thick conductive target could be distinguished from the background. The measurement image is more distributed than the physical sample, as the passing waves are dispersed over the distance of 40 mm between the detector and sample. Considering the difficulty in identifying the wavelength width of the metal using a CMOS detector owing to the distance between the sample and detector, the measurement result exhibits a high-resolution image. All the images were compared by normalizing them to either maximum or minimum ratios.



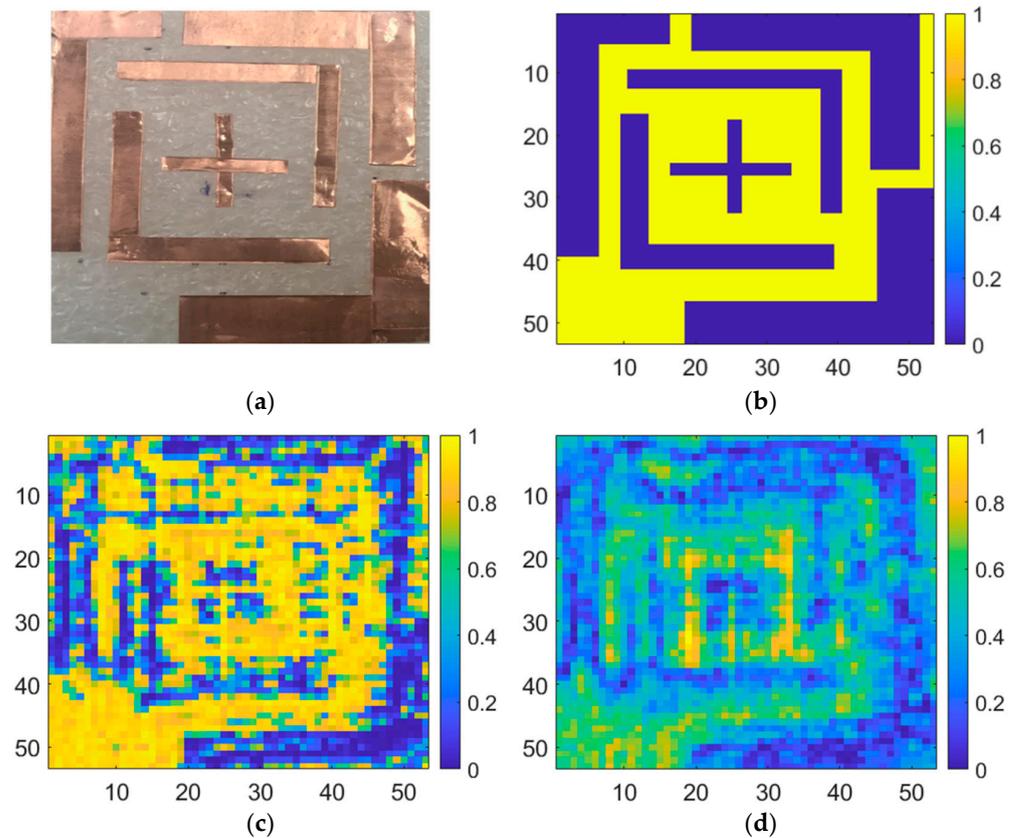
**Figure 11.** Sample target for sub-THz imaging: (a) photograph of a sample with different copper widths; (b) digitalized image of the sample to image correlation.



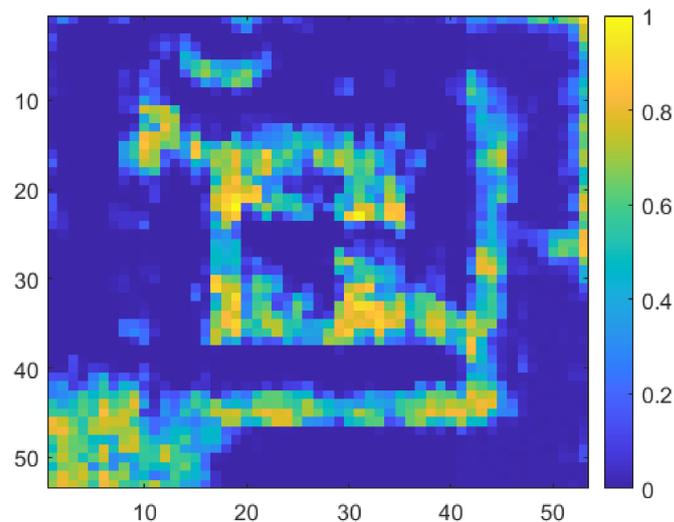
**Figure 12.** Measurement image using the proposed CMOS detector IC.

As illustrated in Figure 13a, the sample is used to compare the effect of the difference in the detector core circuit, and the individual detectors are considered under the optimal detection performance conditions [23]. Figure 13b shows the image obtained using the model capacitor, which is supported by the process design kit (PDK). Figure 13c shows an image obtained from a detector designed to achieve optimal detection performance using a customized capacitor in the same core circuit structure. The proposed detector, as shown in Figure 14, exhibited a 59.37% match with the normalized image, whereas previous studies demonstrated correlations of 41.4% and 53.7%. The concurrent-mode detector containing the cross-coupled capacitors better resolves the inner plus-shaped copper foil, which was impossible to identify in previous studies. The image results show that the image SNR

of a single frame is 49 dB, which is 9 dB higher than that of the image obtained using the previous detector in one frame.



**Figure 13.** Sub-THz imaging in the previous study [23]. (a) Photograph of a real sample; (b) digitized image; (c) using a common-source detector circuit with the standard capacitors in the process design kit; (d) using a common-source detector circuit with the customized capacitors.



**Figure 14.** Imaging measurement using the proposed concurrent-mode detector at 200 GHz.

#### 4. Conclusions

A CMOS detector with concurrent in-phase coupling was proposed to achieve high-quality images using THz imaging systems. The cross-capacitor structure possessed two detecting operations in a common source and a drain input structure while considering

general amplifier analysis. The simulation results demonstrated that the proposed detector exhibits higher detection performance than the previously studied detector topology using gate-drain capacitors. At the output stage, the detector performance with regard to phase coupling was improved by 1.5–3 times higher than that of the previous detector core based on the input power. The detector, manufactured by a TSMC 0.25  $\mu\text{m}$  CMOS process, comprised a differential folded dipole antenna, as the proposed core was connected by cross-coupled capacitors, a pre-amplifier, and a low-gain voltage buffer amplifier. The values of  $R_V$  and  $NEP$  at 200 GHz were 14.13 MV/W and 34.42 pW/ $\sqrt{\text{Hz}}$ , respectively, at a gate bias of 150 mV. In contrast to the previous detector studies, the proposed detector structure has a smaller detector IC area with higher detection performance. At 200 GHz, the measurements of a THz imaging system using samples of copper foil tape attached to Styrofoam substrates demonstrated that the proposed detector can resolve wavelengths (approximately 200 GHz) of 2-mm thickness with a high correlation coefficient. The proposed detector demonstrated an improved correlation of 59.37% with the actual sample, 1.4 times higher than the previous detector under identical conditions, except for the circuit structure. The image SNR, which indicates the image quality, was 49 dB, which was 9 dB higher than that obtained using the model capacitor of the process. The THz image quality was improved using the proposed concurrent-mode CMOS detector without the need for an additional circuit.

**Author Contributions:** Conceptualization, J.-R.Y.; methodology, M.-J.L., G.-E.L. and J.-R.Y.; software, M.-J.L. and H.-N.L.; validation, M.-J.L. and J.-R.Y.; formal analysis, M.-J.L. and J.-R.Y.; investigation, M.-J.L.; resources, S.-T.H. and J.-R.Y.; data curation, M.-J.L. and J.-R.Y.; writing—original draft preparation, M.-J.L., H.-N.L., G.-E.L. and J.-R.Y.; writing—review and editing, M.-J.L., S.-T.H. and J.-R.Y.; visualization, M.-J.L.; supervision, J.-R.Y.; project administration, J.-R.Y. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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