SCIENCE AND TECHNOLOGY OF ADVANCED MATERIALS
2023, VOL. 24, NO. 1, 2212112
https://doi.org/10.1080/14686996.2023.2212112

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Solution-processed zirconium acetylacetonate charge-trap layer for multi-bit nonvolatile thin-film memory transistors

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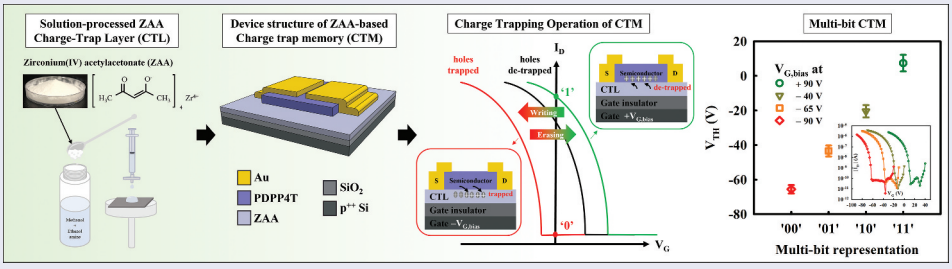
ABSTRACT

The charge trap property of solution-processed zirconium acetylacetonate (ZAA) for solution-processed nonvolatile charge-trap memory (CTM) transistors is demonstrated. Increasing the annealing temperature of the ZAA from room temperature (RT) to 300°C in ambient, the carbon double bonds within the ZAA decreases. The RT-dried ZAA for the *p*-type organic-based CTM shows the widest threshold voltage shift ($\Delta V_{TH} \approx 80$ V), four distinct V_{THs} for a multi-bit memory operation and retained memory currents for 10^3 s with high memory on- and off-current ratio ($I_{M,ON}/I_{M,OFF} \approx 5 \times 10^4$). The *n*-type oxide-based CTM (Ox-CTM) also shows a ΔV_{TH} of 14 V and retained memory currents for 10^3 s with $I_{M,ON}/I_{M,OFF} \approx 10^4$. The inability of the Ox-CTM to be electrically erasable is well explained with simulated electrical potential contour maps. It is deduced that, irrespective of the varied solution-processed semiconductor used, the RT-dried organic ZAA as CTL shows the best memory functionality in the fabricated CTMs. This implies that the high carbon double bonds in the low-temperature processed ZAA CTL are very useful for low-cost multi-bit CTMs in flexible electronics.



ARTICLE HISTORY
Received 16 March 2023
Revised 19 April 2023
Accepted 4 May 2023

KEYWORDS
Zirconium acetylacetonates; solution-processes; charge-trap layers; thin-film memory transistors; multi-bits

1. Introduction

Nonvolatile memory devices such as flash memories with floating gates have received much attention due to the high demand on storage space and its possibility of NAND connection, multi-bit storage, and high memory density [1]. However, the charge-trap memory (CTM) transistor, similar to the floating-gate flash memory, rather uses an insulating layer with trap sites to trap and store charges instead of the conductor-based floating gate for high memory retention [2]. The CTM is characterized by many advantages compared with other nonvolatile memories including non-destructive writing/reading, feasibility of being integrated with traditional complementary metal-oxide semiconductor technique, single device identification in a complex circuitry and finally the implementation of NAND flash memory [3]. Programming and erasing processes of the CTMs are performed by trapping and de-trapping charges respectively within the charge storage insulating layer. Silicon nitride (Si_3N_4) has been extensively used as a charge storage layer for most commercialized CTM products [4]. However, there is a high possibility of charge leakage due to the small conduction band barrier at the Si_3N_4/SiO_2 interface. Therefore, extensive research is currently being conducted on high-*k* dielectrics such as the metal oxides (Ta_2O_5 [1], TiO_2 [5], HfO_2 [6], ZrO_2 [7]) as charge trap layers, because of the higher conduction band barrier at the interface with SiO_2 compared to the Si_3N_4 for better charge retention.

Among the high-*k* metal oxides, zirconium oxide or zirconia (ZrO_2) has received much attention for

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Supplemental data for this article can be accessed online at https://doi.org/10.1080/14686996.2023.2212112.

various low-voltage electronic applications such as memory devices [7], light-emitting diodes [8], thin-film transistors (TFTs) [9] and solar cells [10] due to its high trap-state density, optical transparency and large band gap as a result of the low valence band energy level. In order to form high-quality ZrO_2 layers, various vacuum deposition methods such as sputtering [11] and atomic layer deposition [7] have been used. These processes are characterized by sophisticated equipment and complex procedures making them highly costly. This has recently called for prevalent use of simple and cost-effective deposition methods such as solution-process for large area production. There have been a number of reported solution-processed CTLs which are mainly polymers with poor thermal properties and relatively smaller memory window with respect to the applied programming voltages on Si substrates or with high-vacuum processed semiconductors [12,13]. Instead of the traditional Si semiconductor-substrate or relatively expensive high-vacuum deposited semiconductors, the solution-processed organic and oxide semiconductors have widely been embraced for the production of cost-effective futuristic electronic devices including CTMs due to their low-cost solution processability and other viable processing flexibilities. We previously reported CTM with solution-processed semiconductor and solution-processed Si_3N_4-based inorganic CTL with good memory functionality and good thermal property [14], however the organic-based CTL with high-*k* dielectric will be much preferred.

The solution-processed ZrO_2 is mostly a high thermal decomposition sol-gel product from different precursors through a series of chemical reactions with specific activation energies [15]. Hsu et al. [16] formed ZrO_2 as a CTL by spin-coating a $ZrCl_4$ precursor and then thermally treated over 900°C in an oxygen atmosphere by using rapid thermal annealing for SOZOS (Poly-Si/SiO_2/ZrO_2/SiO_2/Si) memory device on a *p*-type Si substrate. Moreover, the extremely high annealing temperature (>900°C) of the ZrO_2 is a major concern for future printed and flexible electronic devices, therefore, the need for low temperature processes to suit most flexible substrates. To increase the usability of a particular material as CTL, it should be suitable for most of the recent high-performing semiconductors regardless of the processing methods. Therefore, irrespective of the desired low-temperature processed CTL, the optimized CTL should have good thermal properties, mechanical stability, good scalability, and to withstand the possible harsh processing conditions of semiconductors in multi-layered vertically stacked device structures. Acetylacetonate precursor, a carbon-containing bidentate ligand, is known to be a good precursor for organometallic deposition of a wide range of metals including Zr with notably high stability constant and thermally stable [17,18]. A low-temperature processed zirconium acetylacetonate (ZAA) $Zr(C_5H_7O_2)_4$ is promising for high efficient CTMs, which is applicable to a wide variety of substrates and semiconductors owing to its favorable high thermal properties. Additionally, there is a high need of cost-effective multi-bit memories due to the high demand of storage space which is well explored in solution-processed ferroelectric memory transistors (FeMTs) [19,20], but the read operations or the dipoles of these FeMT are easily disturbed by relatively high voltages while the CTMs can stably operate in high voltages. However, multi-bit storage has been a grey area in charge-trap memories and the few reported multi-bit CTMs have multiple stacked layers with high vacuum-processed gate dielectrics [21,22]. A solution-processed organic-based CTL with good thermal properties such as the ZAA, higher trapping effect or wider memory window and a possibility of multi-bit operation will be phenomenal. CTMs based on high performance solution-processed semiconductors with high memory on- and off-current ratio and larger memory window are necessary for cost-effective flexible nonvolatile multi-bit memory devices, and needs to be developed.

In this study, nonvolatile multi-bit CTM with solution-processed organic ZAA CTL and *p*-type organic polymer was demonstrated, and the good thermal property of the ZAA CTL with high temperature processed *n*-type oxide semiconductor-based CTM was also exhibited. X-ray photoelectron spectroscopy (XPS) and Fourier transform infrared (FTIR) spectra revealed changes in the chemical composition of the ZAA layer when the annealing temperature (T_A) increases, such that the ratio of carbon double bonds decreases while the zirconium (Zr) and oxygen (O) contents increased. The effect of the chemical composition changes of the ZAA CTL with temperature on CTMs were examined with solution-processed *p*–type polymer semiconductor, PDPP4T [(poly[2,5–bis(2–octyldodecyl) pyrrolo[3,4–c] pyrrole–1,4(2 H,5 H)–dione –3,6–diyl)–alt–(2,2';5',2'';5'',2'''–quaterthiophen–5,5'''–diyl)])] and *n*–type indium gallium zinc oxide (IGZO) semiconductor. The *p*-type organic PDPP4T-based CTM (PD-CTM) with low-temperature processed ZAA showed a wide memory window of ~80 V and multi-bit operation with four distinct threshold voltages with respective programming voltages. The *n*-type oxide semiconductor-based CTM (Ox-CTM) with low-temperature annealed ZAA also showed a reduced memory window of 14 V due to the high thermal process of the oxide semiconductor. Irrespective of the semiconductor and its thermal process, the ZAA CTL served as a good CTL with good memory functionality and well retained memory states. It was finally deduced that the carbon-

containing ZAA in the low-temperature processed ZAA gives the best memory functionality irrespective of the type and thermal process of the semiconductor used. Finally, the technology computer-aided design (TCAD) simulation was used to investigate and clarify why PD-CTM is both electrically programmable and erasable, while the Ox-CTM is only electrically programmable but optically erasable.

2. Experimental section

2.1 Preparation of CTL

The charge-trap layer (CTL) was prepared by dissolving 40 mg/mL zirconium (IV) acetylacetonate (487.66 g/mol, Sigma-Aldrich) in methanol (32.04 g/mol, Sigma-Aldrich) and adding monoethanolamine (61.08 g/mol, Sigma-Aldrich) as the stabilizer. Silicon wafers were sequentially cleaned in acetone and isopropyl alcohol for 15 min each by ultrasonication and then dried for 30 min. Prior to the spin-coating the ZAA solution, methanol was spin-coated on the substrate and annealed on a hot plate at 65°C for 5 min to enhance coating quality of the ZAA solution. The ZAA solution was spin-coated in ambient conditions at 3000 rpm for 30 s on the methanol-treated substrates, followed by a two-step thermal treatment; all samples were annealed at 65°C for 10 min to evaporate the solvent, and then some were kept in ambient to dry at room temperature while others were annealed at 200°C and 300°C for 60 min in the same ambient condition.

2.2 Fabrication of TFT and CTM devices

2.2.1 P-type organic semiconductor-based CTM

For the *p*-type organic TFT fabrication, the polymer semiconductor, PDPP4T ($(C_{62}H_{90}N_2O_2S_4)_n$), was purchased from Ossila limited and dissolved in a concentration of 5 mg/mL with chloroform. The prepared solution was spun on the cleaned heavily doped silicon substrate with SiO_2 and the ZAA CTL (spin coated on the SiO_2) and annealed in a closed nitrogen atmosphere at 150°C for 20 min to form a 50-nm thick semiconductor layer for the *p*-type PDPP4T-TFT and PDPP4T-CTM respectively. For the improved retention characteristic, the tunneling layer, (poly(9,9-bis(4-hydroxyphenyl) fluorene-co-decafluorobiphenyl) simply known as BHPF solution was prepared by dissolving in 0.3 wt% BHPF in toluene. The prepared BHPF solution was spun on the substrate with ZAA CTL and annealed at 200°C sandwiched between the ZAA and the PDPP4T. To complete the bottom-gate top-contact (BG-TC) device structure, gold (Au) electrodes were formed as source/drain (S/D) by thermal deposition under the pressure of 10^{-6} Torr to a thickness of 35 nm. The channel width to length ratio (W/L) of 5 was used for all the fabricated TFT and CTMs.

2.2.2 N-type oxide semiconductor-based CTM

The *n*-type oxide semiconductor-based TFT or CTM was fabricated on the same cleaned Si/SiO_2 substrates. The IGZO solution was prepared from a 99.9% trace of In, Ga and Zn metals with nitrate hydrate precursors (from Sigma-Aldrich) dissolved in 5 mL of 99.8 anhydrous 2-methoxyethanol to obtain a 0.1 M concentration. The IGZO solution was spin-coated, prebaked at 110°C for 10 min, and then annealed at 450°C for 180 min in ambient conditions respectively to enhance film quality. During the annealing process at high temperature, oxidation of the metal components occurs as well as large quantities of the nitrates and hydrates were removed to the atmosphere to form the dense film [23]. Consequently, a 30 nm-thick IGZO was formed on the Si/SiO_2 substrates without or with ZAA CTL for the Ox-TFT and Ox-CTM respectively. To complete the BG-TC device structure similar to the PDPP4T-TFT and PDPP4T-CTM, 120 nm aluminum (Al) serving as top-contact S/D with a W/L of 5 was thermally evaporated under the pressure of 10^{-6} Torr through a shadow mask.

2.3 Device characterization and simulation

XPS measurements were conducted using PHI 5000 VersaProbe (Ulvac-PHI, Japan) and the thickness of all the various layers was measured using the α-step (D300 Profiler, KLA-Tencor, USA). To calculate the dielectric constant of the respective ZAA layers, simple Si/SiO_2–ZAA–Al devices were fabricated and the capacitance-voltage measurements were done using an impedance analyzer (CompactStat.h, Ivium technologies, Netherlands) to find the total capacitance of the SiO_2 and ZAA (C_{total}). The SiO_2 was added for more accurate capacitance measurements instead of the single ZAA layer which is prone to high leakage and the respective capacitance of the ZAA layers (C_{ZAA}) were deduced from the capacitors in series equation;

$$1/C_{total} = 1/C_{SiO_2} + 1/C_{ZAA} \quad (1)$$

with prior calculation of the capacitance of the SiO_2 (C_{SiO_2}). The dielectric constant of the ZAA was finally calculated from the equation;

$$dielectric\ constant = (C \times d)/(\varepsilon_0 \times A) \quad (2)$$

where C and d are the capacitance and the thickness of the ZAA layer between the two electrodes, ε_0 is the permittivity of free space and A is the area of the overlapped parallel electrodes. To measure the electrical characteristics of the TFTs and CTMs,

a semiconductor parameter analyzer (HP4155A, Hewlett Packard, Japan) was used.

A two-dimensional (2D) finite-element numerical solver (ATLAS, Silvaco, USA) was utilized for the theoretical investigation of the TFTs. The simulator self-consistently solves the coupled Poisson's and drift-diffusion equations over a discrete 2D mesh, which is user-defined to mimic an actual physical device. Materials input parameters were either taken from the literature or fine-tuned to reproduce the experimental transfer characteristics of the devices. These parameters include the ionization energy of 5.26 eV and electron affinity of 4 eV for PDPP4T, the ionization energy of 7.15 eV and electron affinity of 4.1 eV for IGZO, the Au work function of 4.7 eV, the Al work function of 4.2 eV, and the dielectric constant of ZAA of 25.

3. Results and discussion

3.1 Effect of ZAA annealing

We first investigated the chemical compositional changes of the ZAA layer [$Zr(C_5H_7O_2)_4$] at various annealing temperatures. Since the acetylacetonate is a carbon-containing precursor with bidentate ligands bonding with the Zr to form the ZAA, chemical structural changes such as redistribution of electrons or cleavage of the carbon-carbon and/or carbon-oxygen bonds, formation of carbanion or carbocation through various decomposition processes are expected with increasing T_A. Figure 1(a–c) shows the pristine ZAA powder and its chemical structure, the preparation and deposition process of the solution-based ZAA, and finally the drying at RT or thermal treatment at two different temperatures (200°C and 300°C) in ambient condition. These temperatures were carefully selected for possible future flexible electronics applications since most of the commercialized advanced flexible substrates have glass transition temperatures below 350°C [24].

To identify the elemental intensities, chemical compositional changes and bond formations with respect to the T_A, XPS measurements were performed. Figure 2(a–c) shows the carbon (C1s), oxygen (O1s), and zirconium (Zr3d) XPS results of the ZAA layer, respectively. As notably seen in the XPS data, increasing the T_A, the intensity of C1s decreases while those of the O1s and Zr3d increase. The decomposition of the ZAA starts at temperatures within 150°C to 200°C and continues as the T_A increases due to redistribution of electrons and different bond formations or conversions in the conjugated acetylacetonate [$(C_5H_7O_2)_4$] [17]. The increase of the O1s and the Zr3d is mainly due to the annealing temperature in atmospheric conditions with enough oxygen to form zirconium oxide

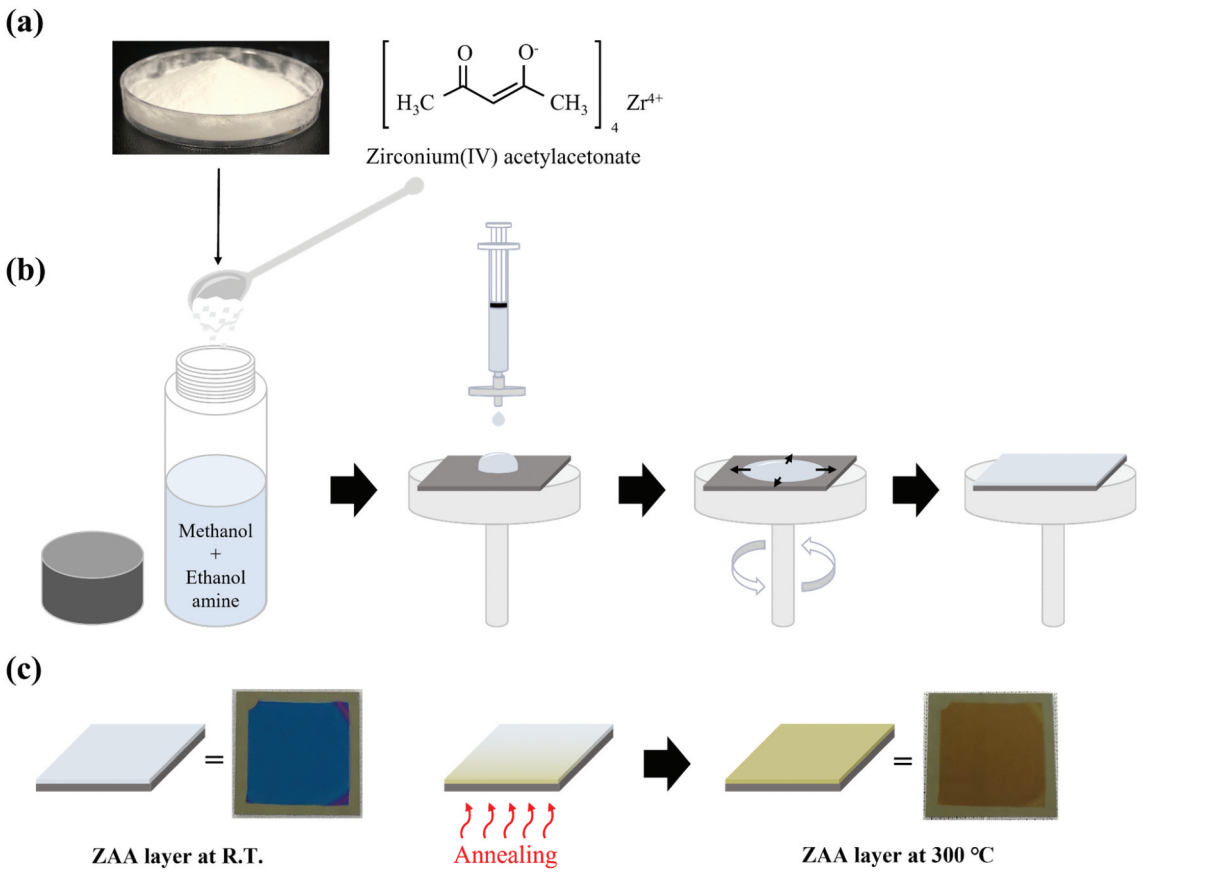

Figure 1. (a) a picture of the powdered ZAA and the corresponding schematic structure. (b) the preparation and spin-coating process and (c) two different thermal processes (drying and annealing at 300°C) of the ZAA layer.

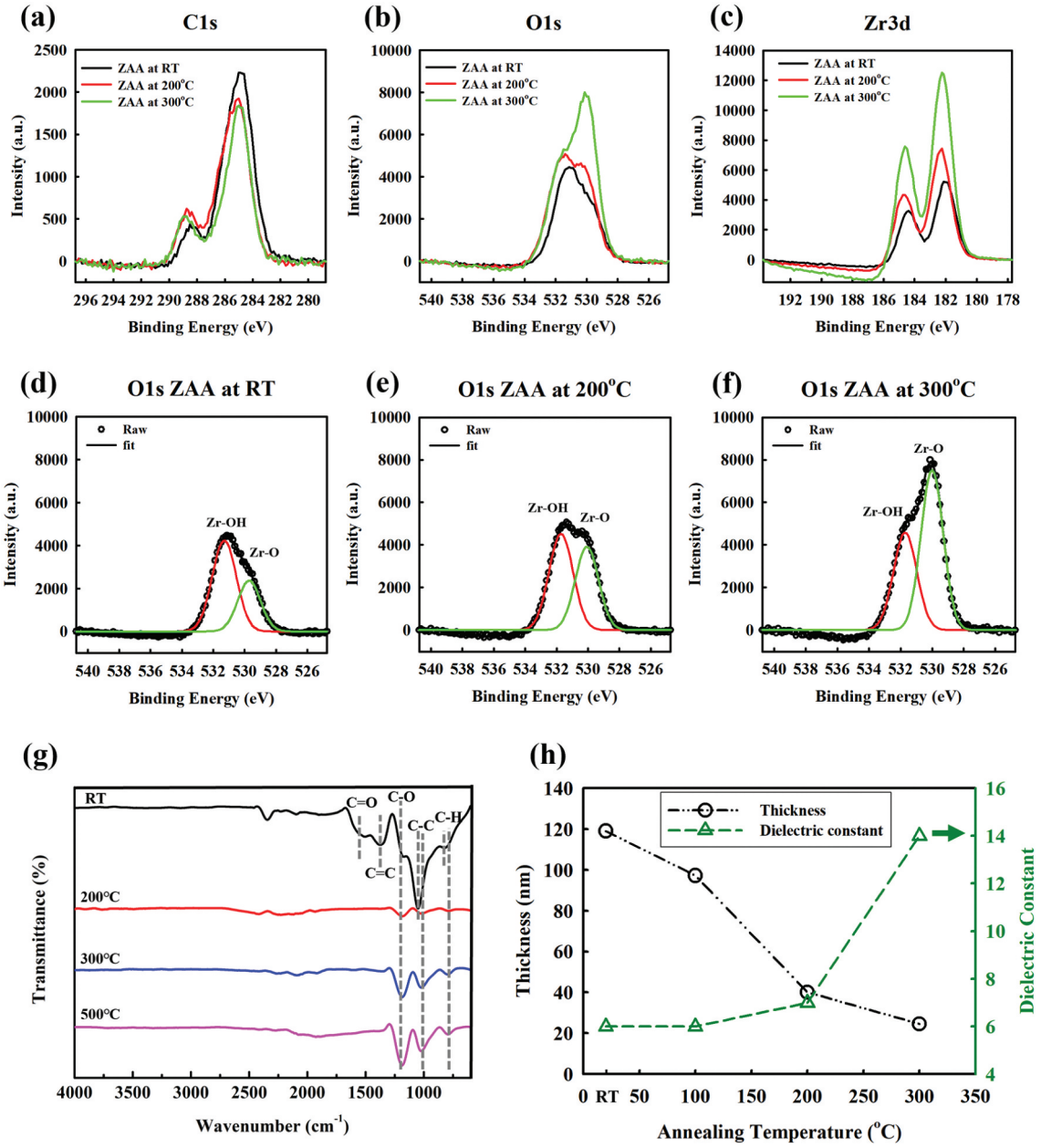

Figure 2. XPS data analysis showing the (a) C1s, (b) O1s, and (c) Zr3d peaks of the ZAA annealed at different temperatures. The deconvoluted XPS peaks of O1s in ZAA (d) dried at RT, (e) annealed at 200°C and (f) 300°C. (g) FTIR spectra at different temperatures and finally, (h) the thickness and dielectric constant variation against annealing temperatures.

bonds (Zr–O). Figure 2(d–f) shows the significant increase in the Zr–O bonds as the temperature increases in the deconvoluted XPS peaks of the O1s with the peak intensity at 530.0 eV which is the conventional quantitative binding energy of Zr–O [25].

The increase of the oxygen is further confirmed by the FTIR spectra in Figure 2(g) where the C–O bonds increase as the T_A increases in ambient conditions. The FTIR spectra also show the drastic reduction of the C=C and C=O bonds as the T_A increases from RT to 500°C. The two main double carbon bonds (C=C and C=O) relatively disappear and form single carbon bonds with annealing temperatures of 200°C and above due to the thermal treatment. Furthermore, the deconvoluted XPS peaks of the C1s also confirms the reduction of the C–C bond as the T_A increases (supplementary Figure S1). Since the carbon-carbon double bonds of hydrocarbons including the acetylacetonate mostly consist of stronger sigma bonds and weaker pi (π) bonds, the π bonds are easily broken resulting in carbon-carbon single bonds conversion. The FTIR spectra show a gradual increase of the C–C and C–O as the T_A increases from 200°C to 500°C due to the breaking of the π bonds and redistribution of electron pairs to change the double carbon bonds to single carbon bonds. Hence, the XPS and FTIR data proved that as the T_A of the ZAA layer increases, there is high formation of Zr–O bonds due to the high oxygen content in the ambient condition and redistribution of electrons changing the double carbon bonds to single carbon bonds.

To analyze the effect of the T_A and chemical compositional changes on the electrical and physical properties of the ZAA layer, the dielectric constant and thickness of the ZAA layer depending on the T_A were examined. As shown in Figure 2(h), the thickness of the ZAA layer decreases from about 120 nm to 25 nm as the T_A increases from RT to 300°C. This film thickness variation is attributed to the evaporation of moisture within the acetylacetonate solvent and the feasible carbon byproducts as the T_A increases. The evaporation of the reaction byproducts also results in the reduction of the density of defects within the Zr–acetylacetonate which occupies relatively larger volumes compared to the Zr–O and Zr–OH bonds formed as the T_A increases resulting in thickness reduction of the ZAA layer [26]. In contrast, the dielectric constant increases from 6 to 14 as the T_A increases from RT to 300°C. The release of the various carbon reaction byproducts and the increase of Zr–O bonds gradually turns the ZAA layer to a high-k metal oxide. Note that as the T_A of the ZAA layer is further increased above 300°C to over 800°C for a possible complete decomposition of the carbon molecules, the ZAA thin film is sequentially changed to ZrO_x which has a dielectric constant of 25 [27,28]. This explains the gradual increase of the dielectric constant of the ZAA films with increasing T_A. It can finally be deduced from the dielectric data results that the RT-dried ZAA layer has a relatively lower dielectric constant although higher than that of the SiO_2 (3.9) and similar to $SiON_x$ (~7) [14] which are conventionally used as gate dielectric and charge-trap materials respectively.

3.2 ZAA-based CTM with p-type organic semiconductor

The conventional high temperature processed ZrO_x and other vacuum processed metal oxides for single-bit small memory window charge trap memories led to the exploration of the low temperature solution-processed organic-based metal acetylacetonate material as CTL for multi-bit CTM in flexible electronics.

In order to ascertain the charge trapping effect of the ZAA layer, the electrical properties and memory functionalities were examined by first fabricating a reference thin-film transistor (TFT) with recently used high performance p-type polymer semiconductor (PDPP4T) [14,29]. The transfer characteristic curves of the initial state (no gate-bias) and the transfer curves after programming and erasing were measured to confirm the charge trap effect of the p-type TFT. To perform the programming and erasing operations, –90 V and +90 V with a pulse width of 320 ms were applied to the gate for 11 steps, respectively, while 0 V was applied to both source and drain electrodes. The respective transfer curves were later measured with drain voltage (V_D) of –30 V. The high gate-bias voltage (±90 V) is mainly necessary due to the commercially used Si wafers with very thick SiO_2 (200 nm) which consumes about 75 V of the applied gate-bias voltage. Considering the commercialized CTM with a total thickness of about (20–30) nm using a programming voltage of 20 V, our fabricated CTM can proportionally be used for practical applications when the thickness of the SiO_2 is drastically reduced. The output curves for the PDPP4T-based TFT (PD-TFT) were measured and showed conventional p-type output characteristic curves for the various gate voltages (supplementary Figure S2). Figure 3(a) shows the transfer curves of PD-TFT without ZAA. The selected threshold voltages (V_{TH}) of the initial state and after being programmed and erased are −3 V, −1 V and 24 V respectively. The V_{TH} is selected as the gate voltage which causes 1 nA drain current to flow within the TFT [30] and this analogy was used throughout the data analyses for consistency. Compared to the V_{TH} of the initial state (−3 V), there was negligible change in the V_{TH} from the initial state after applying the programming voltage ($\Delta V_{TH,P}$), however, there was a significant change in the initial V_{TH} to the positive direction after erasing ($\Delta V_{TH,E}$) with high positive gate bias. The $\Delta V_{TH,E}$ is caused by electrons being trapped at the interface between PDPP4T and SiO_2 by a large positive gate-bias voltage similar to reported organic semiconductor/dielectric interfaces [31,32].

To fabricate the three different PDPP4T-based CTMs (PD-CTMs), dried and thermally treated ZAA at RT, 200°C, and 300°C sandwiched between the SiO_2 and the PDPP4T to act as a CTL were fabricated respectively. The same programming and erasing technique for the PD-TFT was applied to the PD-CTMs and the transfer curves of the initial state, and after programming and erasing were measured to confirm the charge trap effect of all the CTMs. Figure 3(c–e) respectively shows the transfer characteristic curves of the PD-CTMs with ZAA treated at RT, 200°C, 300°C. In contrast to the PD-TFT, all the PD-CTM devices with ZAA CTL showed large $\Delta V_{TH,P}$ to the negative direction signifying high hole traps with high negative gate-bias voltage [33]. With the high negative biased gate voltage at the interfaces of the SiO_2, ZAA and the semiconductor, the conjugated structure of the pristine Zr-acetylacetonate can easily react with protons or holes from the semiconductor and stored within the ZAA layer. The bidentate acetylacetonate with enough electron pairs undergo nucleophilic reactions at two different bonding areas [34] by accepting holes from the p-type semiconductor which aids in the hole trapping effect of the ZAA layer. Additionally, the double carbon-carbon bonds containing reactive π bond electron pairs are more reactive to assist in double or high hole trapping [35] compared to the single carbon-carbon bonds. That is, the high negative gate bias voltage assists the

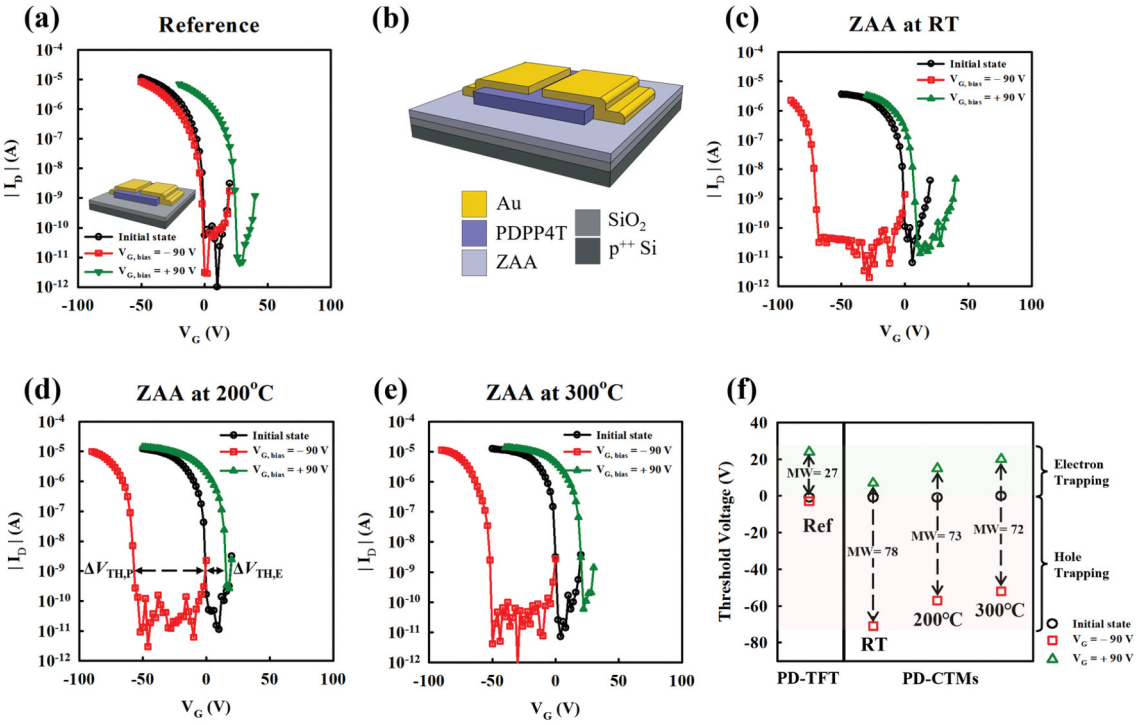

Figure 3. The transfer curves ($V_D = -30$ V) of the (a) PDPP4T-TFT (inset shows the device structure of PDPP4T-TFT). (b) the device structure of the PDPP4T-based CTM and its respective transfer curves with ZAA (c) dried room temperature (RT) and annealed at (d) 200°C and (e) 300°C. (f) the threshold voltage shift against the annealing temperatures of ZAA.

movement of holes from the *p*-type semiconductor to react with the 'C=O and C=C' bonds in the conjugated ZAA structure. The hole trapping effect or the magnitude of the $\Delta V_{TH,P}$ decreases from 70 V in the PD-CTM with ZAA dried at RT (PD-CTM$_{\mathbf{RT}}$) to 52 V in the PD-CTM with ZAA annealed at 300°C (PD-CTM$_{\mathbf{300}}$). Therefore the PD-CTM$_{\mathbf{RT}}$ has the highest trap sites and as the T_A increases, the number of trap sites to accept holes decreases due to the reduction of more reactive double bonds (C=O, C=C) resulting in a narrow $\Delta V_{TH,P}$. In spite of that, there is still enough C1s for hole traps within the PD-CTM$_{\mathbf{300}}$ far greater than the PD-TFT as the Zr-acetylacetonate nucleophilic reactions still exist and the carbon fully decomposes over 500°C. Another point to note is the decrease of the on-current in the PD-CTM$_{\mathbf{RT}}$ compared to the PD-TFT which is mainly due to the strong polaronic coupling effect between the charge carriers of the semiconductor and the dipoles of the ZAA CTL [36]. The saturation carrier mobility (μ_{sat}) which is also likely to be affected is evaluated from Equation (3);

$$I_D = \frac{WC\mu_{sat}}{2L}(V_{GS} - V_{TH})^2 \quad (3)$$

where W and L are the width and length of the transistor, C is the capacitance of the gate dielectric and V_{GS} is the gate-to-source voltage [37]. The mobility of the PD-TFT and that of the PD-CTM$_{RT}$ were calculated to be 0.15 $cm^2V^{-1}s^{-1}$ and 0.04 $cm^2V^{-1}s^{-1}$ respectively and this reduction is better than other reported CTMs with similar structural configuration [14]. Furthermore, to evaluate the bias-stress effect on the PD-CTM$_{RT}$, the transfer characteristic curves were measured with high negative gate-bias voltage of −90 V applied to the PD-CTM$_{RT}$ for 3.2 s, 6.4 s and 12.8 s (supplementary Figure S3) and they all showed the same mobility of 0.05 cm^2-$V^{-1}s^{-1}$ and slight negative shift of the V_{TH} as the stress time increased.

The $\Delta V_{TH,E}$ of PD-CTMs signifying electron traps after applying the high positive voltage rather increases as the T_A increases. PD-CTM$_{\mathbf{RT}}$ showed the least $\Delta V_{TH,E}$ or electron traps since the high level of electron-pairs and nucleophilic reaction in the PD-CTM$_{\mathbf{RT}}$ makes it difficult to trap electrons. However, when the T_A increases, there is an increase in oxygen concentration from the ambient and hydroxyl groups (–OH) are gradually formed which aids in electron traps. Alternatively, there is possible carbocation generated from the terminating alkyl of the ZAA as the T_A increases which makes the residual ZAA attract few electrons possible for the small $\Delta V_{TH,E}$. The electron traps within the PD-TFT are even higher or similar to the PD-CTMs since the ZAA CTL suppresses electron traps or may not be a good CTL for electron traps. It is evidently seen that the ZAA CTL is the main component of charge traps within the PD-CTMs and it mainly traps holes and few electrons depending on the processing temperature of the ZAA. Figure 3(f) compares the memory window of the PD-TFT and PD-CTMs calculated as the total change in threshold voltage (ΔV_{TH}) after the high negative and positive gate bias extracted from the measured transfer curves,

i.e. $\Delta V_{TH}=\Delta V_{TH,P}+\Delta V_{TH,E}$. The PD-CTMs have a wider memory window compared to the PD-TFT due to ZAA CTL and the PD-CTM$_{\mathbf{RT}}$ showed the largest memory window (78 V) while the PD-CTM$_{\mathbf{300}}$ showed the least memory window (72 V) among the PD-CTM. The sequential programming and writing of the PD-CTMs were also measured to show the repeatability and stability of the memory devices (supplementary Figure S4).

In order to investigate the ability of the fabricated PD-CTMs to retain its memory states and store the charges within the CTL after high positive and negative gate bias, the respective memory output drain currents ($I_{M,OUTs}$) were observed for 10^3 s for the PD-TFT and PD-CTMs with reference gate voltage for reading ($V_{G,REF}$) and V_D of −5 V each. These low voltages for reading the memory states are good for low power consumption memory devices and also negligible read-out disturbances of the memory states for the retention period. The high positive voltage for the electron trap showed the higher $I_{M,OUT}$ and was classified as on-state and vice versa at the same $V_{G,REF}$ and V_D. As shown in Figure 4(a), the $I_{M,OUTs}$ rapidly degrade in PD-TFT devices, due to the lack of a CTL. However, the PD-CTMs with a ZAA CTL showed a small reduction in the on-states and relatively stable off-states as seen in Figure 4(b–d) signifying relatively small charge loss. The PD-CTM$_{\mathbf{RT}}$ had the highest memory on- and off-current ratio ($I_{M,ON}/I_{M,OFF}$ = 5×10^4) even after 10^3 s while the PD-CTM$_{\mathbf{200}}$ and PD-CTM$_{\mathbf{300}}$ showed $I_{M,ON}/I_{M,OFF}\approx 10^3$ because the trapped charges were stably stored within the ZAA CTL irrespective of the T_A.

For improved retention characteristics, a thin fluorinated polymer (BHPF) was used as a tunneling layer between RT-dried ZAA and PDPP4T. The transfer characteristic curves showed a similar memory window (78) and the retention operations showed a more stable $I_{M,OUTs}$ with slightly higher $I_{M,ON}/I_{M,OFF}$ (10^5) compared to that of the PD-CTM$_{\mathbf{RT}}$ (supplementary Figure S5). Therefore, the main component for the memory retention is the low-temperature annealed ZAA CTL and other device modifications or additional layers possibly improve the memory functionalities of the ZAA-based PD-CTMs.

Considering the wide memory window and relatively high $I_{M,ON}/I_{M,OFF}$ measured for the PD-CTMs, the PD-CTM$_{\mathbf{RT}}$ was further explored for multi-bit memory

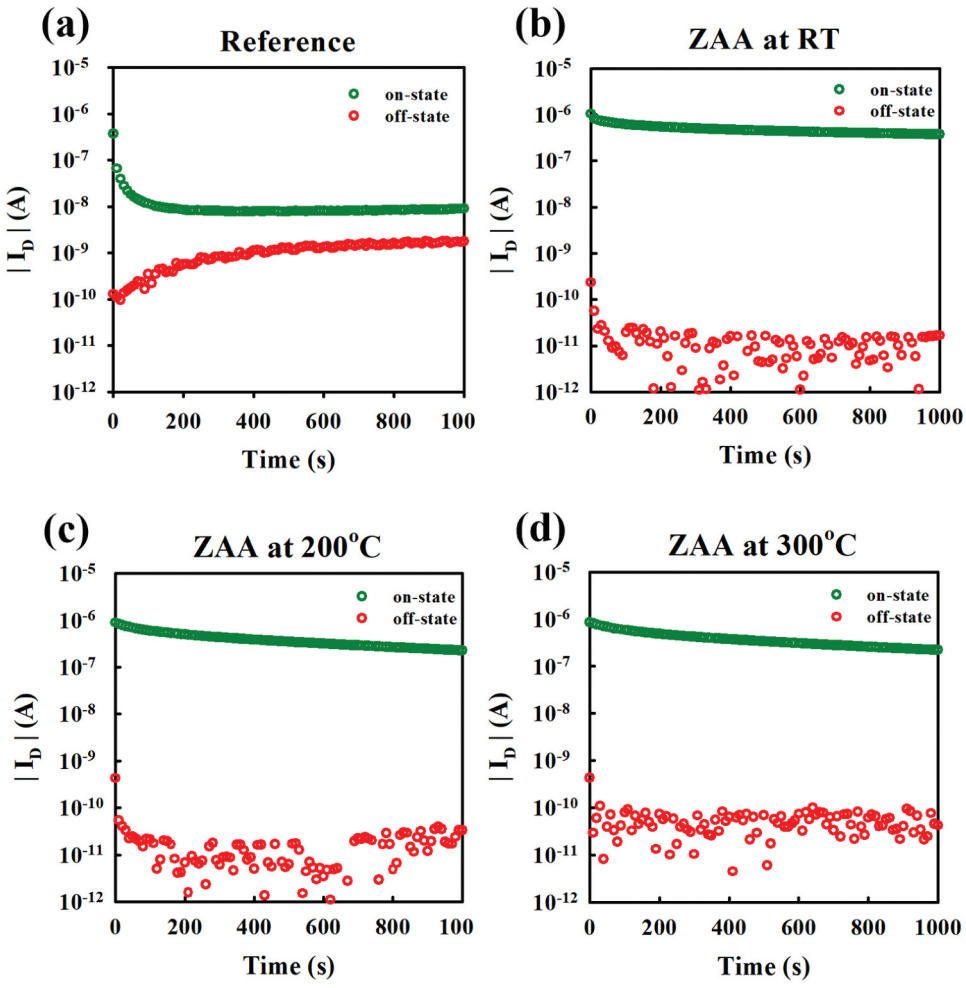

Figure 4. The output memory drain current of the (a) PDPP4T-TFT and PDPP4T-based CTMs with ZAA layer annealed at (b) RT, (c) 200°C (d) 300°C at programming voltages of ±90 V and reading gate reference voltage and drain voltage of −5 V each.

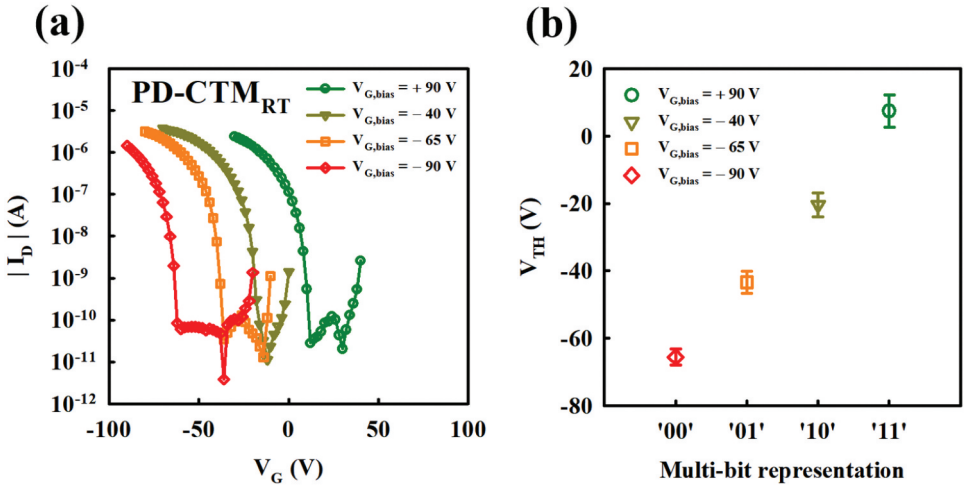

Figure 5. The (a) transfer curves and (b) respective V_{TH} against the multi-bit representation the four selected programming voltages (−90 V, −65 V, −40 V and+90 V) representing each memory state.

functionality. For the CTM to serve as a 2–bit memory cell, there should be at least four distinct V_{TH} distributions across the programming or erasing voltage range to represent each paired bit ('00', '01', '10' and '11'). Figure 5(a) shows the four transfer curves from the full programming and erasing voltages of ±90 V and then two other carefully selected gate bias voltages (−40 V, −65 V). The V_{TH} distributions from the transfer curves of the selected programming voltages showed respective V_{THs} of −65 V, −43 V, −20 V, +7 V and are plotted against the multi-bit representation in Figure 5(b). The individual multi-bit state of the CTM is read out effectively as long as the V_{TH} distributions do not overlap each other. The measured V_{THs} are separated from each other by at least a 20 V gap which makes room for possible error margins for practical application and easier selection of the reference read voltage lines to distinguish each memory state for reading and writing operations. Since each V_{TH} represents a particular programmed memory state within the CTM, the respective four independent well-spaced V_{THs} represent the multi-bit memory states in the fabricated PD-CTM. In addition, to check the stability, durability and repeatability of the multi-bit PD-CTM, the V_{THs} of the respective multi-level states were sequentially and repetitively measured for over 10^3 s and showed distinct and clear memory margins between each of the group of 2-bit memory representations ('11', '10', '01', and '00') (supplementary Figure S6).

3.3 ZAA-based CTM with n-type oxide semiconductor

In order to investigate the charge trap effect and good thermal property of the ZAA CTL, IGZO-based TFT (Ox-TFT) and IGZO-based CTM with ZAA CTL (Ox-CTM) annealed under same T_A conditions (RT, 200°C, 300°C) were examined. The IGZO semiconductor was processed at 450°C to enhance the film quality. Same high gate bias voltages (±90 V) were used to program and possibly erase the memory states. Figure 6(a) shows the transfer curves of the Ox-TFT with no notable shifts of the transfer curves (V_D = 30 V) after applying both high gate-bias voltages. This indicates that there is no charge trap effect in Ox-TFT without ZAA CTL. The output curves for the Ox-TFT for various gate voltages were also measured and showed conventional *n*-type output characteristic curves to confirm the good performance of the reference Ox-TFT device (supplementary Figure S7). The device structure of the fabricated Ox-CTM is shown in Figure 6(b) while Figure 6(c–e) respectively shows the corresponding transfer curves of the Ox-CTMs with ZAA CTL treated at RT, 200°C, 300°C. Electrons are trapped in Ox-CTM with ZAA CTL annealed at RT (Ox-CTM$_{RT}$), showing a positive V_{TH} shift of 14 V after the positive gate bias and gradually reduced to 6 V in the Ox-CTM with ZAA annealed at 300°C (supplementary Figure S8).

The Ox-CTM$_{RT}$ showed the highest electron trap density and the positive shift of the V_{TH} decreases as the T_A increases signifying the reduction of the electron traps. This is similar to the earlier report on the reduction of electron traps in the Ox-CTM using the solution-processed Si_3N_4-based inorganic CTL [14]. The electron traps within the Ox-CTM$_{RT}$ are attributed to the residual carbon within the ZAA dried at RT since partial decomposition of the carbon occurs below 500°C. The effective temperature of the ZAA dried at RT is possibly 500°C due to the annealing process of the upper layered IGZO. However, the V_{TH} shift or electrons trap reduction as the T_A of the ZAA increases is due to the earlier reduction of the carbon content by the 200°C, 300°C annealing processes and the further thermal treatments. Additionally, there is gradual formation of ZrO_x as the effective T_A increases and the ZrO_x/IGZO interface does not induce many electron traps

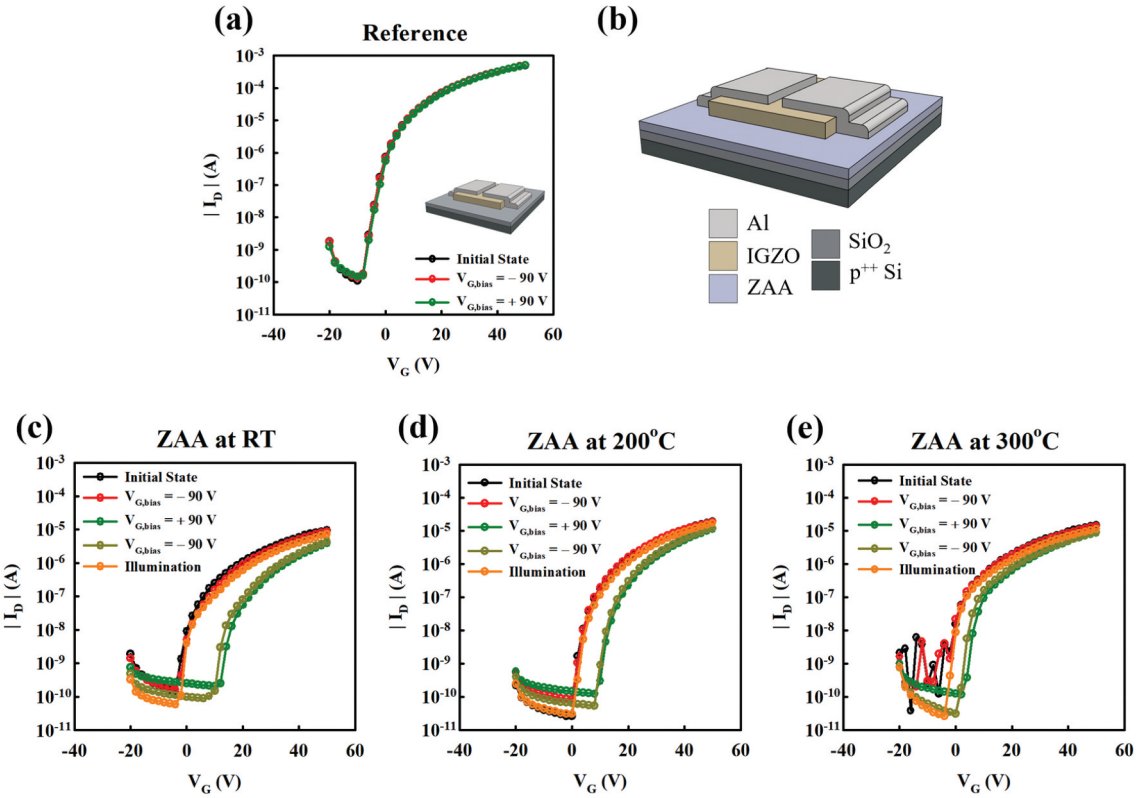

Figure 6. The transfer curves (V_D = 30 V) of the (a) Ox-TFT (inset shows the device structure of Ox-TFT). (b) the device structure of the Ox-based CTM and its respective transfer curves with ZAA (c) dried room temperature (RT) and annealed at (d) 200°C and (e) 300°C.

due to the small electron trap density at the interface, hence, the reduction of the electron traps [38].

When a large negative voltage (−90 V) is applied to the gate for erasing after applying the positive programming voltage for electron traps, the threshold voltage hardly shifts to the negative direction in all the Ox-CTMs. This implies that erasing electrically is not possible in the Ox-CTM as earlier reported in other studies [14,39]. To solve this problem and de-trap the electrons within the ZAA CTL, white light with a power density around 1.8 mW/cm^2 is irradiated for 10 s onto the Ox-CTM which induces the generation of excess electrons or oxygen vacancies (V_O^{2+}) in the semiconductor and effectively releases the trapped electrons. The memory retention of the Ox-CTM$_{\mathbf{RT}}$ was measured with $V_{G,REF}$ of 4 V, V_D of 5 V and showed retained $I_{M,OUTs}$ for 10^3 s and a $I_{M,ON}/I_{M,OFF}$ of 3.7 $\times 10^3$ (supplementary Figure S9). Ox-CTM showed smaller ΔV_{TH} compared to PD-CTM mainly due to the high thermal process of the oxide semiconductor resulting in the further decomposition of the carbon within the ZAA, however, the charge trapping effect of the ZAA is successfully demonstrated in both the *p*-type organic polymer-based-CTM and high annealed *n*-type oxide semiconductor-based CTM. Table 1 compares the remarkable results of the solution-processed ZAA CTL for CTMs with other relatable reported CTMs to show the high prospects of this study. The number of charges stored per area (Δn) within the CTL was calculated from

$$\Delta n = \frac{\Delta V_{TH} C_i}{e} \quad (4)$$

where C_i is the capacitance of the gate insulator and ΔV_{TH} is the threshold voltage shift and e is the elementary charge.

3.4 Programming/erasing simulation

The inability of most oxide semiconductor-based CTMs including the fabricated Ox-CTM to be electrically erasable like the organic polymer based-CTMs has been a major current issue. Therefore, the potential distributions for both the PD-CTM and Ox-CTM were theoretically examined at their programming and erasing cycles. Technology computer-aided design (TCAD) simulation was conducted to obtain 2D electric potential contour maps and corresponding one-dimensional (1D) vertical cross-section profiles when the gate bias of −90 V and +90 V were applied to program and erase the PD-CTM respectively. For simplification, region 'A' is defined from the bottom of the source and drain electrodes (S/D) to the gate and region 'B' as the area between the two 'A' regions. In order to trap holes in the ZAA CTL of the PD-CTM, a negative programming voltage is applied. As a result, holes are injected from the S/D into the PDPP4T and the potential is shown to rather uniformly vary from 0 to −90 V from the PDPP4T to

Table 1. Comparison of the solution-processed ZAA CTL for CTMs with other relatable reported CTMs.

CTL Material	Annealing temperature of CTL [°C]	Semiconductor	Memory window (Operating voltage)	Thickness of SiO_2 gate insulator	Number of stored charges, Δn [$\times 10^{12} cm^{-2}$]
Solution-processed ZAA	**27**	**Solution-processed PDPP4T**	**78 V (+90 V/−90 V)**	**200 nm**	**8.42**
Solution-processed PαMS [40]	60	Thermally deposited pentacene	90 V (200 V/−100 V)	300 nm	6.47
Solution-processed PHPS [14]	27	Solution-processed PDPP4T	59 V (+90 V/−90 V)	200 nm	6.37
Solution-processed Au-NPs [41]	100	Thermally deposited pentacene	43 V (+80 V/−150 V)	300 nm	3.09
PS-brush [42]	170	Solution-processed N2200+TIPS-PEN	55 V (−120 V/+100 V)	300 nm	3.96
Solution-processed ZrO_2 [16]	900	Si substrate	2.7 V (+15 V/−15 V)	30 nm	1.94
Atomic layer deposited HfO_2 [6]	250	Sputtered a-IGZO	4.1 V (+15 V/−15 V)	100 nm	0.88

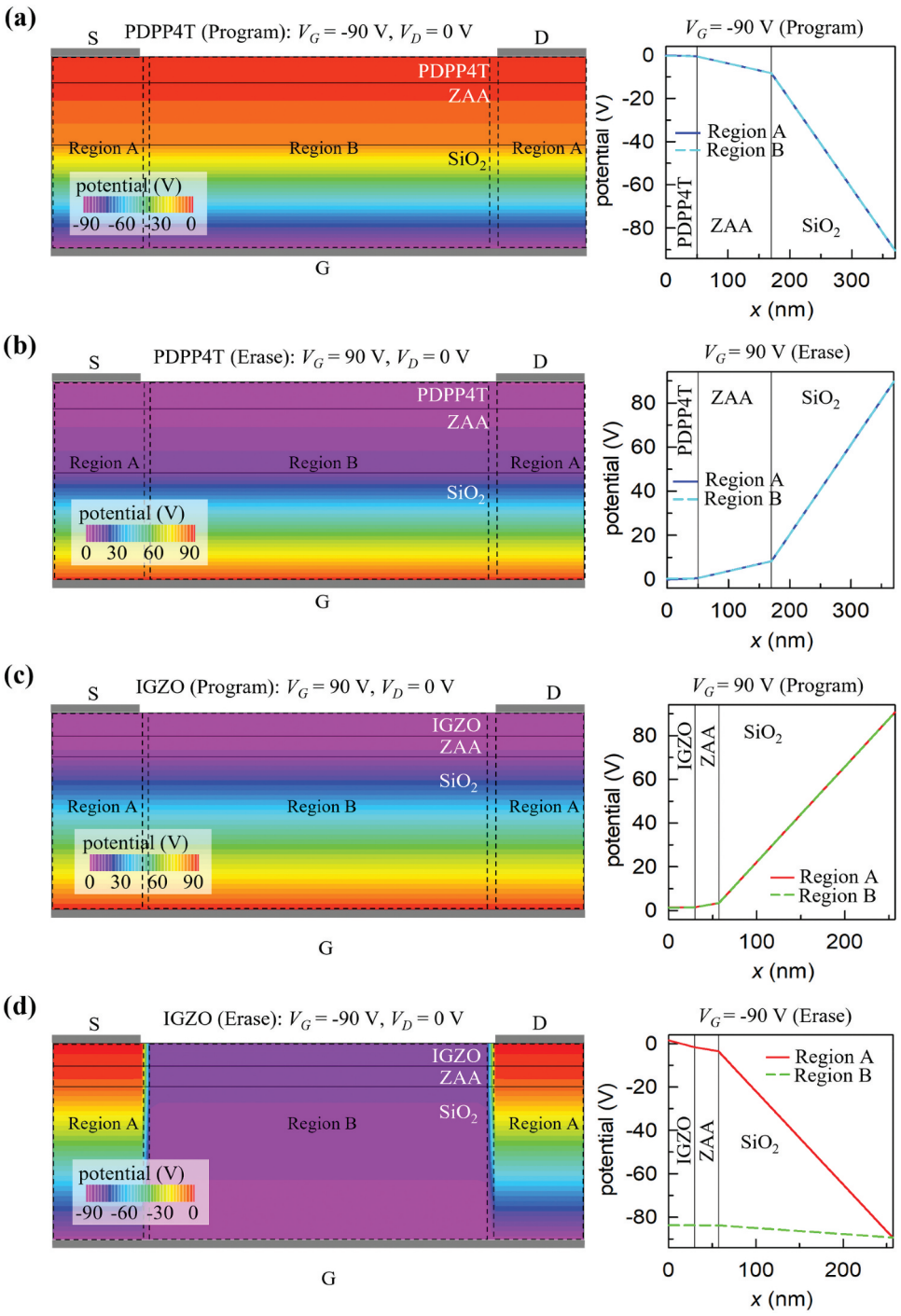

Figure 7. 2D electric potential contour maps and the corresponding 1D vertical cross-sectional profiles of the simulated PDPP4T-CTM at (a) programming (−90 V) and (b) erasing (+90 V) cycles; and of the IGZO-based CTM at (c) programming (+90 V) and (d) erasing (−90 V) cycles (G: gate, S: source, and D: drain).

the gate electrode in both region 'A' and 'B' as shown in Figure 7(a). Thus, holes are trapped in ZAA CTL at the regions 'A' and 'B' due to the generated electric field in the direction of the gate electrode. Also, the trapped holes cause the negative shift of $V_{TH,P}$ as shown in transfer curves of the PD-CTMs. In contrast to the programming of PD-CTM, positive erasing voltage (V_{ER}) was applied to de-trap holes or trap electrons. As a result, electrons are injected from S/D to the PDPP4T and uniform voltage distributions are presented in both regions 'A' and 'B' as shown in Figure 7(b). Thus, holes are de-trapped (electrons are trapped) causing a positive shift of $V_{TH,E}$ as also shown transfer curves of the PD-CTMs. Therefore, it is concluded that the PD-CTM is electrically programmable and erasable as the applied gate-biases are distributed across all the layers. Likewise, the electrical potential map for the Ox-CTM was then examined with programming and erasing voltages applied to the gate. Electrons are injected from S/D to IGZO when a programming voltage of +90 V is applied and Figure 7(c) shows well distributed electric potential across regions 'A' and 'B'. Thus, the high positive gate bias induces electron traps from the IGZO to the ZAA, causing a positive shift of $V_{TH,P}$ as shown in transfer curves of the Ox-CTM. However, when the V_{ER} of −90 V is applied to the gate electrode of the Ox-CTM, there is only a uniform potential distribution at regions 'A' but only a small vertical potential drop occurs in region 'B' as seen in Figure 7(d). The striking difference in the non-uniform potential distribution at the channel and the S/D regions is attributed to the inability of holes to be injected from the IGZO to the CTL even at a high negative gate bias. This issue mainly comes from the lack of mobile holes in the valence band [43] of the IGZO and the wide band gap of the metal-oxide semiconductors. The organic polymer semiconductor (PDPP4T) has a small band gap allowing both electron and hole injection while the oxide semiconductor (IGZO) has a wide band gap which favors the unipolar injection of electrons. The large band gap of IGZO caused the large injection barrier between the S/D electrode (Al) and the valence band of the IGZO.

IGZO therefore operates like an insulator when the high negative voltage is applied which causes a large potential difference between regions 'A' with the S/D electrodes and channel region 'B' as shown in Figure 7(d). A small potential difference (<10 V) is seen in the channel region ('B') from the cross-sectional profile which is apparently very weak to induce the de-trapping electrons when the high negative gate bias voltage is applied to the Ox-CTM. It is deduced that the Ox-CTM is therefore not electrically erased and needs other mechanisms such as light illumination for the de-trapping of the electrons.

4. Conclusion

The charge trap characteristics of the solution-processed ZAA layer for solution-processed CTMs were presented. As the annealing temperature of the ZAA increased from RT to 300°C, the Zr−O bonds in the ZAA thin film increased while the double carbon bonds decreased or were converted to single carbon bonds. The PDPP4T-based CTM with ZAA dried at RT showed the best memory performance with wide memory window of 80 V, retained memory currents for 10^3 s with a high $I_{M,ON}/I_{M,OFF}$ of 5 X 10^4. Due to the wide memory window, the PDPP4T-based CTM also showed multi-bit memory states with well distinguished four threshold voltages. To confirm the good thermal property of the ZAA CTL, the IGZO-based CTM with RT-dried ZAA showed a relatively smaller memory window of 14 V and retained its memory states for 10^3 s. The possibility of the low-temperature processed ZAA to be successfully used with different high performance semiconductors with varied thermal processes and still showed good memory functionality, makes the ZAA an ideal CTL for the fabrication of cost-effective multi-bit charge-trap memories in recent flexible electronics.

Disclosure statement

No potential conflict of interest was reported by the author(s).

Funding

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education [2018R1A6A1A03026005] and by the Korea government (MSIT) [NRF-2021R1A2C2011560].

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