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High-Performance WS_2 MOSFETs with Bilayer WS_2 Contacts

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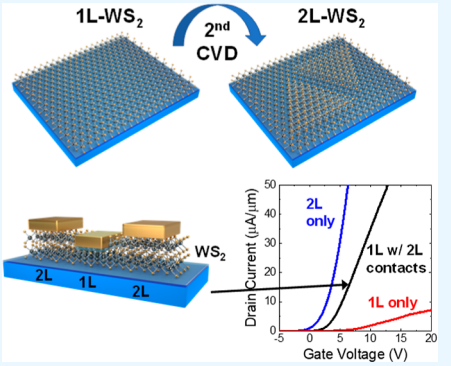
ABSTRACT: WS_2 is a promising transition-metal dichalcogenide (TMDC) for use as a channel material in extreme-scaled metal-oxide-semiconductor field-effect transistors (MOSFETs) due to its monolayer thickness, high carrier mobility, and its potential for symmetric n-type and p-type MOSFET performance. However, the formation of stable, low-barrier-height contacts to monolayer TMDCs continues to be a challenge. This study introduces an innovative approach to realize high-performance WS_2 MOSFETs by utilizing bilayer WS_2 (2L-WS_2) in the contact region grown through a two-step chemical vapor deposition process. The 2L-WS_2 devices demonstrate a high I_{ON}/I_{OFF} ratio of 10^8 and a saturated drain current, $I_{D(SAT)}$, of 280 μA/μm (386 μA/μm) at room temperature (78 K), even while still using conventional metal (Pd or Ni) contacts. Devices featuring a 1L-WS_2 channel and 2L-WS_2 in the contact regions were also fabricated, and they exhibited performance comparable to that of 2L-WS_2 devices. The devices also exhibit good stability with nearly identical performance after storage over a 13 month period. The study highlights the benefits of a hybrid channel thickness approach for TMDC transistors.



INTRODUCTION

As metal-oxide-semiconductor field-effect transistors (MOSFETs) continue their relentless march in the sub-10 nm regime, addressing the challenges of extending Moore's law becomes increasingly imperative.[1] One key approach to confronting these challenges is the exploration of novel channel materials for future nanoelectronics applications. Among the promising candidates, transition-metal dichalcogenides (TMDCs) have tremendous potential for realizing MOSFETs with extreme scalability due to their ability to be controllably synthesized as single-unit-cell monolayers. The scalability of these devices has been demonstrated theoretically, and the development of large-area synthesis techniques lends credence to their potential for large-scale integration on a 300 mm wafer platform.[2,3] However, the ability to form low-resistance, stable contacts remains an outstanding challenge that needs to be overcome before TMDCs can be considered to be a legitimate contender for integrated circuit applications.

The contact resistance in MOSFETs is determined in part by the Schottky barrier height (SBH) at the metal−semiconductor (M−S) interface. In the simplest model, the SBH is determined by the difference between the work function of the metal and the electron affinity of the semiconductor. However, due to metal-induced gap states (MIGSs) in the semiconductor, Fermi level pinning (FLP) is widely observed in experiments[4−6] where the SBH at the M−S interface exhibits little dependency on the metal work function value.

Recently, low-work-function semimetals have attracted tremendous interest as contacts for TMDC-based n-MOSFETs.[7−10] Due to the low density of states at the Fermi level in semimetals, MIGS in the semiconductor can be effectively reduced. This helps to position the Fermi level near or within the conduction band of the semiconductor, resulting in an extremely low contact resistance in n-MOSFETs. Among Bi, Sb, and As semimetallic contacts, Bi has the lowest work function and has demonstrated the lowest contact resistance to TMDC-based MOSFETs.[4,11] Nonetheless, its practical utility is constrained by its low thermal stability, primarily attributed to a relatively low melting point (271.5 °C).[8,12] This, in turn, leads to degradation of device stability and compatibility during fabrication.

Several strategies have been used to establish pristine van der Waals contacts, including mechanical transfer of metals[13] or graphene,[14] direct evaporation of soft metal alloys such as In/Au,[15] and the formation of metal−semiconductor heterostructures through vapor epitaxy growth.[16] Notably, vapor-phase epitaxy stands out as an effective method for creating high-quality van der Waals contacts. Transport simulations have revealed that bilayer (2L) TMDCs outperform their monolayer (1L) counterparts due to their enhanced intrinsic mobility and density of states.[17,18] Furthermore, the durability of 2L materials against fabrication-induced damage helps

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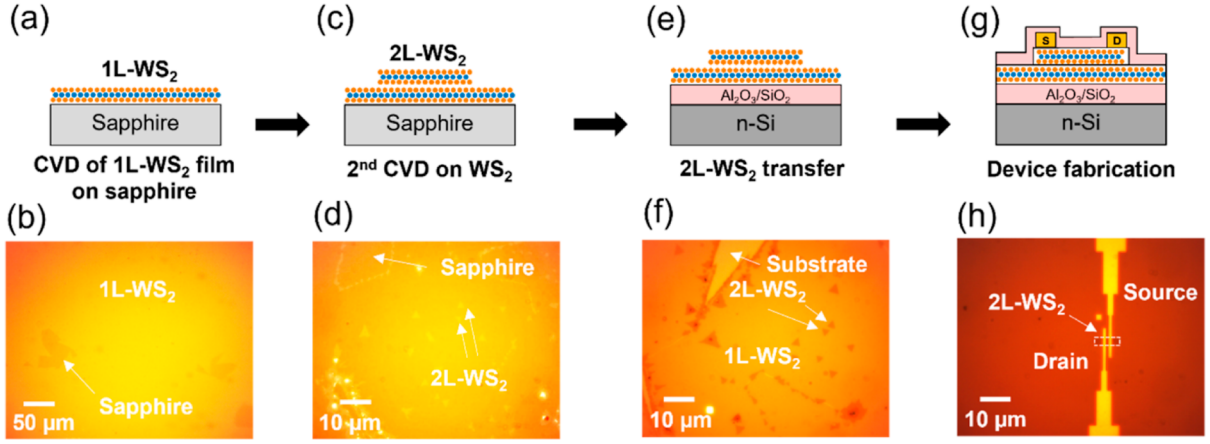

Figure 1. Fabrication process of 2L-WS_2 MOSFETs. The top row shows cross-sectional schematics of 2L-WS_2 growth and device fabrication, while the bottom row shows optical micrographs for the corresponding steps. (a,b) First chemical vapor deposition (CVD) of 1L-WS_2 on the *c*-plane sapphire substrate, (c,d) CVD of the second layer of WS_2 on 1L-WS_2, (e,f) transfer of the 1L/2L-WS_2 film onto $Al_2O_3/SiO_2/Si$ substrates, and (g,h) fabrication of bottom-gated MOSFETs using 2L-WS_2.

mitigate extrinsic disorder-induced gap states, thereby alleviating FLP and reducing the SBH at the M−S interface. Among TMDCs, WS_2 has attracted increasing research interest for its application in MOSFETs owing to its large band gap, high mobility, high saturation velocity, and its potential for symmetric n-type and p-type FET performance.[19,20]

Recently, high-performance CVD 1L-WS_2 and 2L-WS_2 devices have been reported in the literature. Serval noteworthy 1L-WS_2 devices with Bi contacts are summarized in Table S1. For instance, when compared at V_{DS} = 1 V, Shen et al. reported a current density of 150 μA/μm (L_{DS} = 100 nm),[7] Li et al. achieved 250 μA/μm (L_{DS} = 135 nm),[21] while our previous work reported 105 μA/μm (L_{DS} = 320 nm).[8] Notably, recent advancements in ultrashort channel CVD 1L-WS_2 MOSFETs have shown an on-current of 320 μA/μm (L_{DS} = 30 nm) with Ni contacts.[22] The pinnacle of performance in CVD 2L-WS_2 devices was achieved by Shi et al.,[18] who reported an on-current of 635 μA/μm at V_{DS} = 1 V, with an ultrashort channel length of 18 nm and Ni contacts (Table S2). Meanwhile, Lin et al. demonstrated an on-current of 310 μA/μm for a CVD 2L-WS_2 device with an L_{DS} of 100 nm.[23] It is worth noting that while the improved on-current of the 2L-WS_2 device can be partially attributed to its higher channel mobility, the influence of 2L-WS_2 on contact quality remains an aspect yet to be fully explored.

In this study, we investigate 2L-WS_2 contacts as an alternative solution for contact engineering, with the potential for low contact resistance but with improved thermal and temporal stability. N-MOSFETs were fabricated on both 1L-WS_2 and 2L-WS_2. In addition, n-MOSFETs with 1L-WS_2 channels were fabricated with 2L-WS_2 in the contact regions. The 2L-WS_2 devices exhibited a saturated drive current of 280 μA/μm at room temperature (RT) and 386 μA/μm at 78 K. Similarly, the 1L-WS_2 device with 2L-WS_2 contacts demonstrated high performance, displaying a comparable scaled drive current per channel length under the same biasing conditions as the 2L-WS_2 devices.

RESULTS AND DISCUSSION

The key steps of the fabrication process are described in Figure 1. The fabrication started with the growth of a continuous 1L-WS_2 film on a *c*-plane sapphire substrate, as shown in Figure 1a. The first 1L-WS_2 film was grown via chemical vapor deposition (CVD) and showed a smooth and continuous monolayer, as shown in Figure 1b. On top of this layer, a second CVD layer was grown, where the growth was noncontinuous and formed only small islands (Figure 1c) of 2L-WS_2, while the remaining regions remained single layer. The growth of the second set of WS_2 regions is evident by the emerging triangular flakes on 1L-WS_2 in Figure 1d in contrast to the as-grown clean 1L-WS_2 film, which remained continuous and intact. Full details of both CVD growths are described in the Methods section.

The device fabrication started with an n-type Si wafer, which served as a bottom-gate electrode. On top of this wafer, 16 nm of SiO_2 was grown by thermal oxidation, followed by deposition of 30 nm of Al_2O_3 by atomic layer deposition (ALD). The equivalent oxide thickness (EOT) of the bottom-gate dielectric is calculated as 30.6 nm (Figure S1 and Table S3), where dielectric constants of $K(SiO_2)$ = 3.9 and $K(Al_2O_3)$ = 8.0 were assumed. Next, the WS_2 film was transferred onto the bottom-gate dielectric using a wet transfer process described previously[24] using a poly(methyl methacrylate) (PMMA) supporting layer. A 25% hot KOH solution was used to separate the PMMA/WS_2 stack from the sapphire. This process is shown in Figure 1e,f. For all patterning steps, electron-beam lithography (EBL) was used. After fabrication of alignment marks, mesa isolation was performed using EBL, followed by dry etching to define the active area. Next, source/drain lithography was performed, followed by Pd/Au (10/100 nm) metallization and solvent lift off. Three types of devices were fabricated: (1) 1L-WS_2 devices with Pd/Au contacts, (2) 2L-WS_2 devices with Pd/Au contacts, and (3) devices with 1L-WS_2 channels and 2L-WS_2 in the contact regions. After contact formation, a 1 nm thick Al seed layer was evaporated and oxidized in air, and then the devices were passivated by 30 nm of Al_2O_3 deposited by ALD. A cross-sectional schematic diagram and an optical micrograph of a completed 2L-WS_2 device are shown in Figure 1g,h.

The WS_2 layers were characterized by using Raman and photoluminescence (PL) spectroscopy. Raman spectra of both 1L-WS_2 and 2L-WS_2 are shown in Figure 2a, revealing characteristic WS_2 out-of-plane E^1_{2g} and in-plane A_{1g} vibration modes. The frequency difference between these modes is 60.35

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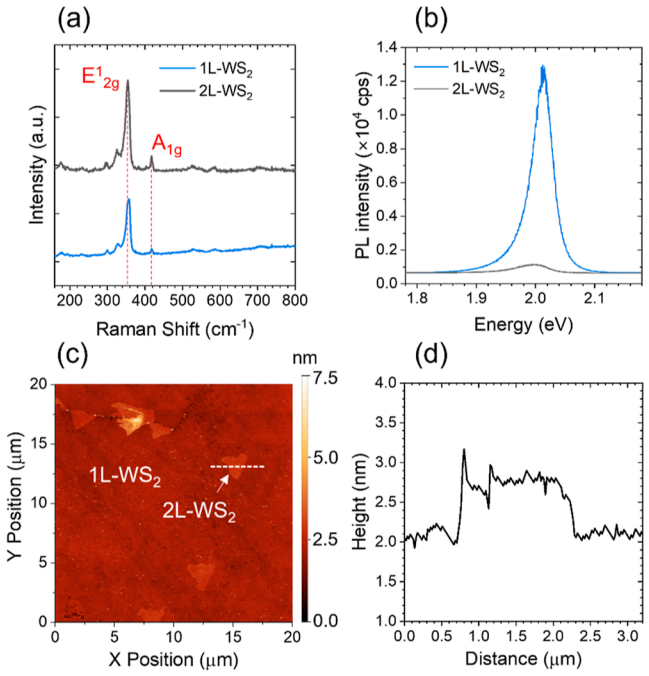

Figure 2. Characterization of as-grown 1L-WS_2 and 2L-WS_2. (a) Raman spectra from regions corresponding to 1L-WS_2 (blue curve) and 2L-WS_2 (black curve). WS_2 characteristic peaks for in-plane A_{1g} and out-of-plane E_{2g}^1 vibration modes are labeled. (b) PL spectra from regions of 1L-WS_2 (blue) and 2L-WS_2 (black). (c) AFM height map of a 20 × 20 μm area depicting the growth of a second layer of WS_2 on a continuous 1L-WS_2. (d) Height profile extracted along the dashed line shown in (c).

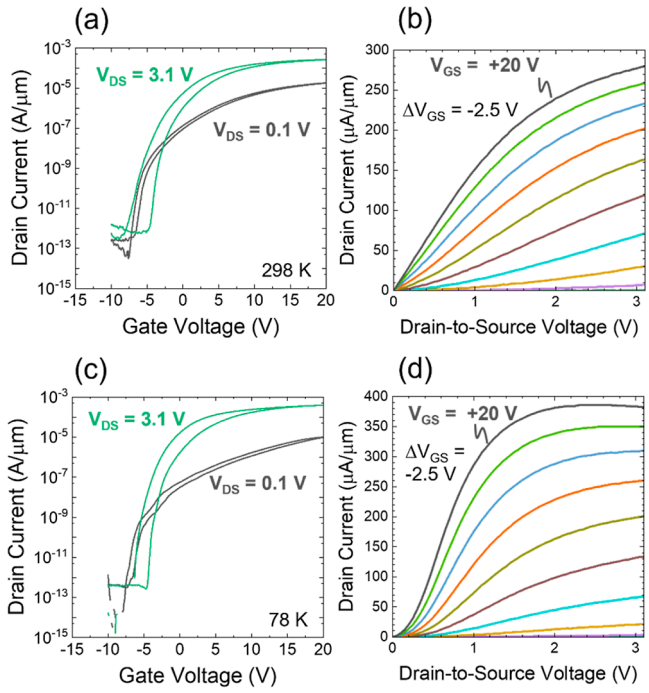

Figure 3. Transfer and output characteristics of a bottom-gated 2L-WS_2 MOSFET with L_{DS} = 0.3 μm and W_{ch} = 3 μm. (a,b) RT characteristics showing (a) linear and saturation transfer characteristics and (b) output characteristics using pulsed-mode sweep where I_D is measured using 0.5 ms pulses on V_{DS} with 5% duty cycle. (c,d) Measurements of the same device at 78 K, measured under the same conditions as in (a,b). In both (a,c), the hysteresis is clockwise.

cm^{-1} for 1L-WS_2 and 62.16 cm^{-1} for 2L-WS_2 (Figure S2). This wavenumber difference has been used previously as a fast approach for determining the WS_2 thickness. Multilayer WS_2 is expected to exhibit a larger frequency difference due to van der Waals interactions between layers.[25] In Figure 2b, the PL spectra of both 1L-WS_2 and 2L-WS_2 are compared. A substantial reduction in light emission from 2L-WS_2 was observed, which can be attributed to the direct-to-indirect gap transition when progressing from 1L-WS_2 to 2L-WS_2.[26] The surface of the film grown after the two-step CVD was characterized using atomic force microscopy (AFM), and the resulting height map of a 20 × 20 μm region is displayed in Figure 2c. The map illustrates a continuous 1L-WS_2 film (Figure S3) with the presence of 2L-WS_2 flakes grown on the surface. The height profile along one of the 2L-WS_2 flakes is shown in Figure 2d. The measured thickness, which is sub-1 nm, corresponds to the thickness of a single additional layer of WS_2. The composition of 2L-WS_2 was confirmed through cross-sectional transmission electron microscopy (TEM) and energy-dispersive X-ray (EDX) spectroscopy characterizations, as shown in Figure S4. In the 2L-WS_2 region, strong signals for W and S were detected. This observation aligns with the Raman results in Figure 2a, which also reveal characteristic WS_2 peaks in the 2L-WS_2 region.

Electrical measurements of all devices were conducted in vacuum using an Agilent 4156C semiconductor parameter analyzer. Figure 3a,b displays the transfer and output characteristics, respectively, of a 2L-WS_2 MOSFET with Pd contacts with drain-to-source spacing, L_{DS} = 0.3 μm at RT. The device demonstrated n-type behavior, exhibiting a high I_{ON}/I_{OFF} ratio of 10^8, as shown in Figure 3a. The saturated drain current, $I_{D(SAT)}$, reaches 280 $\mu A/\mu m$ at gate-to-source and drain-to-source voltages of V_{GS} = +20 V and V_{DS} = +3.1 V, respectively, at RT. In the device saturation regime where V_{DS} = +3.1 V, the device exhibits a maximum transconductance, g_m, of 18.6 $\mu S/\mu m$, along with an extracted field-effect mobility, μ_{FE}, of 15.9 $cm^2/(V\ s)$ (Figure S5). Here, the output characteristics were measured using pulsed-mode sweep where I_D is measured using 0.5 ms pulses on V_{DS} with 5% duty cycle. The pulsed measurement scheme was used not to address self-heating but rather to overcome dielectric charge-trapping effects, which become more severe at forward gate bias. In Figure 3b, a relatively linear I_D vs V_{DS} response is observed at V_{GS} = +20 V in the low-V_{DS} regime, suggesting the presence of Ohmic-like contacts. However, the contact becomes somewhat Schottky-like at low V_{GS}, indicating the existence of a slight potential barrier at the semiconductor−metal interface, which limits carrier injection in the low-bias regime. The transition between Ohmic-like and Schottky-like contacts can be attributed to the bottom-gated configuration, where the band bending in WS_2 reduces the width of potential barrier at high V_{GS}. At 78 K, $I_{D(SAT)}$ is further improved to 386 $\mu A/\mu m$ (Figure 3c). However, as shown in Figure 3d, the device exhibits Schottky-like contacts at 78 K, even at V_{GS} = +20 V. The drive current improvement can be attributed to reduced electron−phonon scattering at low temperature, leading to an increase in mobility.[27,28] The slight decrease of the drain current with an increasing V_{DS} at V_{GS} = +20 V could be a result of self-heating effects.

It is suspected that 2L-WS_2 can contribute to both reduced contact resistance and improved carrier mobility in the channel, leading to improved $I_{D(SAT)}$. To investigate the

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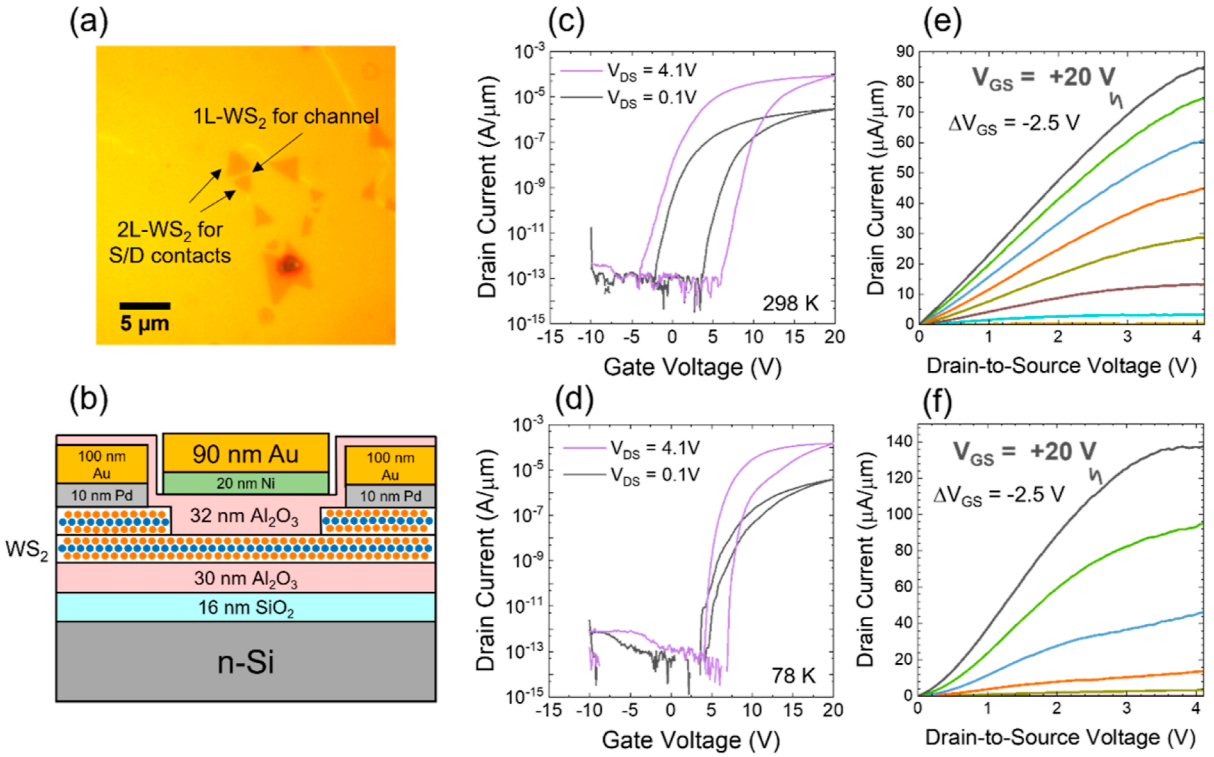

Figure 4. Electrical characterization of a dual-gated MOSFET with an 1L-WS_2 channel and 2L-WS_2 contacts. (a) Optical micrograph of two WS_2 flakes grown closely on the 1L-WS_2 film. A MOSFET would be fabricated where source and drain Pd/Au (10/100 nm) contacts were deposited on adjacent 2L-WS_2 flakes and the channel consists of 1L-WS_2 between the two WS_2 flakes. (b) Cross-sectional schematic of a dual-gated MOSFET with a 1L-WS_2 channel and 2L-WS_2 contacts fabricated on the two adjacent 2L-WS_2 flakes in (a). Here, the source-drain spacing, L_{DS} = 1.7 μm, is defined by the Pd/Au contact spacing and the gate length, L_G = 1.0 μm, is defined by the Ni/Au top gate dimensions. The channel width W_{ch} is 1.5 μm. (c,d) Transfer characteristics at (c) RT and (d) 78 K. In both plots, the hysteresis is clockwise. (e,f) Output characteristics at (e) RT and (f) 78 K.

specific contribution of 2L-WS_2 contacts to this improvement, we also fabricated dual-gated MOSFETs (EOT = 10.3 nm) using two adjacent 2L-WS_2 flakes, as depicted in Figure 4a. In these devices, the source and drain contact electrodes were made into two different 2L-WS_2 flakes, where a distinct region of 1L-WS_2 remained between the flakes. The fabrication process was the same as that described previously, except that an additional top gate was formed on top of 32 nm Al_2O_3 (EOT = 15.6 nm) by patterning the top gate (L_G = 1.0 μm) through EBL, followed by metallization with Ni/Au (20 nm/90 nm). As shown in Figure 4b, the Pd source/drain contacts were deposited on 2L-WS_2, but the channel comprises only 1L-WS_2 because the separate 2L-WS_2 flakes are not coalesced. Using this technique, a MOSFET with L_{DS} = 1.7 μm was formed, where L_{DS} was defined as the distance between the Pd/Au electrodes. The L_{DS} is larger compared to the 2L-WS_2 device since it is constrained by the distance between the two adjacent 2L-WS_2 flakes. The MOSFET was measured in dual-gated mode, where top and bottom gates were tied together. Transfer characteristics of the n-MOSFET at RT and 78 K are shown in Figure 4c,d, respectively, and show devices with I_{ON}/I_{OFF} of 10^8 similar to the results in Figure 3, where 2L-WS_2 was continuous throughout the channel region. The reduction of hysteresis in the MOSFET at 78 K is noticeable owing to the reduced thermally activated charge injection into trap sites in the gate dielectric. An extracted maximum g_m of 6.8 μS/μm and a μ_{FE} of 8.5 $cm^2/(V\ s)$ are obtained from Figure 4c. The μ_{FE} value is roughly one-third of the 2L-WS_2, showing degraded transport when only 1L-WS_2 is present in the channel (Figure S5). As shown in Figure 4e,f, the drain current of the MOSFET reaches 85 μA/μm at RT and 138 μA/μm at 78 K, respectively, at V_{GS} = +20 V and V_{DS} = +4.1 V. It should be noted that the current in the device in Figure 4 with the 1L-WS_2 channel and 2L-WS_2 contacts has a longer L_{DS} value than the all-2L-WS_2 device in Figure 3, and once this difference is accounted for, the performance of the two devices is comparable. The device in Figure 4 also demonstrated Ohmic contacts at V_{GS} = +20 V at RT and more Schottky-like contacts under the same bias conditions at 78 K, similar to the device in Figure 3.

Given the limited number of available devices with various channel lengths, the traditional transfer length measurement could not be used to provide a quantitative value for the contact resistance. This limitation arises due to the challenge of growing two sufficiently close 2L-WS_2 regions. Instead, to quantitatively compare the RT performance of devices with different channel lengths, we introduce a parameter, $I_D \times L_{DS}$, to scale the ON current by L_{DS}. These values are compared at V_{DS} = +0.1 V, and a sheet carrier concentration of n_S = 8.6 × 10^{12} cm^{-2}. The all-2L-WS_2 device exhibited $I_D \times L_{DS}$ of 5.4 μA, while the 1L-WS_2 device with 2L-WS_2 contacts exhibited $I_D \times L_{DS}$ of 2.4 μA. Additionally, a reference all-1L-WS_2 device was fabricated with direct Pd contacts to the 1L-WS_2 (Figure 5). That device, which had L_{DS} = 1.0 μm, displayed an $I_D \times L_{DS}$ of only 0.13 μA at V_{DS} = +0.1 V, over an order of magnitude lower compared to MOSFETs with 2L-WS_2 in the contact regions. In addition, the all-1L-WS_2 device exhibits a total resistance, R_{tot}, of 0.77 × 10^6 Ω−μm, which is approximately

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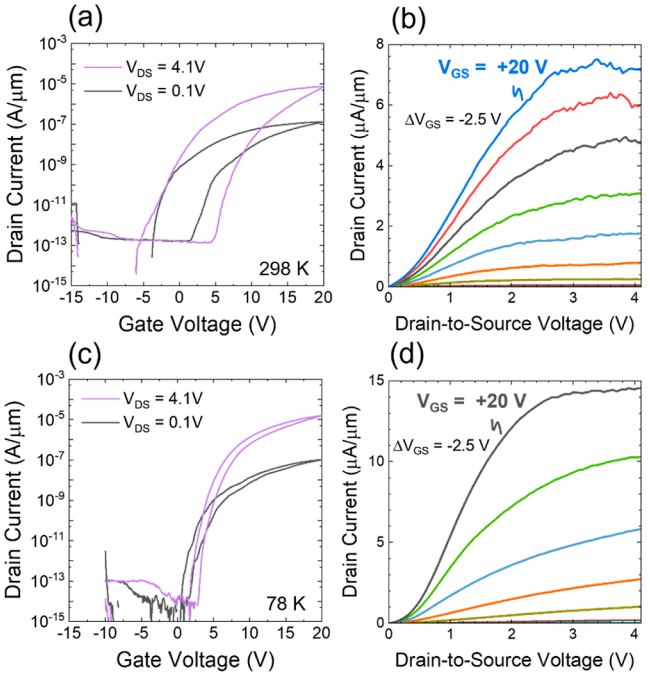

Figure 5. (a,b) RT characteristics for a bottom-gated 1L-WS_2 MOSFET (EOT = 30.6 nm) with Pd/Au (10/100 nm) contacts and L_{DS} = 1.0 μm, W_{ch} = 10 μm. (a) Linear and saturation transfer characteristics and (b) output characteristics using pulsed-mode sweep where I_D is measured using 0.5 ms pulses on V_{DS} with 5% duty cycle. (c,d) Measurements of the same device at 78 K, measured under the same conditions as in (a,b). In both (a,c), the hysteresis is clockwise.

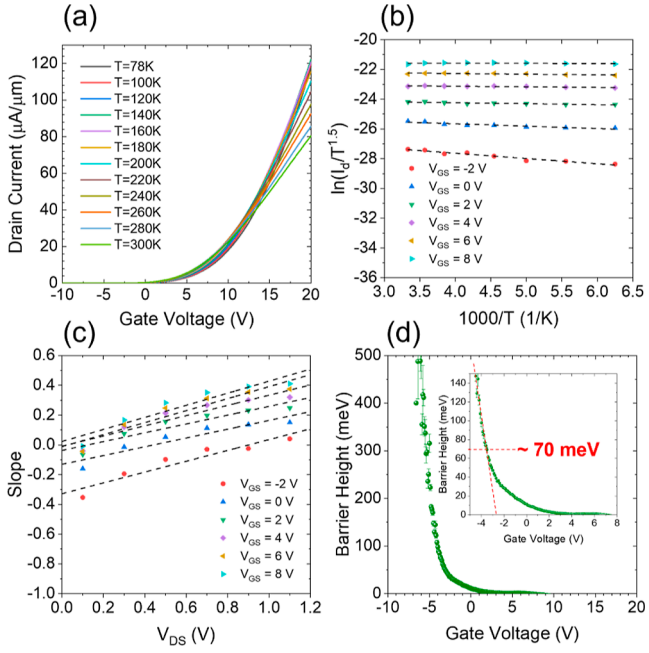

Figure 6. Temperature-dependent transfer characteristics of a bottom-gated 2L-WS_2 MOSFET with Pd/Au (10/100 nm) contacts with L_{DS} = 0.3 μm. (a) Drain current, I_D vs gate voltage, V_{GS}, is plotted at V_{DS} = 0.5 V covering a temperature range from 300 to 78 K. (b,c) Arrhenius analysis showing (b) temperature and (c) drain bias dependence. (d) Effective barrier height vs gate voltage. The flat band barrier height was estimated from point where the decreasing barrier height deviates from the linear fit (red dashed line).

20 times larger than that of the 1L-WS_2 MOSFET with 2L-WS_2 in the contact regions, despite having a shorter L_{DS} of 1.0 μm. These results suggest that the primary reason for the enhanced performance of the 2L-WS_2 devices is improved contact quality. Additional results on similar Pd-contacted 1L-WS_2 devices are provided in Figure S6, showing similar on-state resistance. To further assess 2L-WS_2 contact quality, we compared the 1L-WS_2 device shown in Figure 4e with our previously reported Bi-contacted 1L-WS_2 MOSFET.[8] Both devices have the same dual-gated configuration (EOT = 10.3 nm) and a comparable L_{DS} of 1.7 μm. At V_{DS} = 1 V, the 2L-WS_2-contacted MOSFET reached 23 μA/μm compared to 13 μA/μm in the Bi-contacted 1L-WS_2 MOSFET (Figure S7). In contrast, the all-1L-WS_2 MOSFET with Pd contacts only achieves 2.5 μA/μm even with a shorter L_{DS} of 1 μm.

In order to investigate the energy barrier at the 2L-WS_2/Pd interfaces, temperature-dependent transfer characteristics were measured on the MOSFET from Figure 3. As shown in Figure 6a, a crossover was observed in the transfer characteristics with increasing gate voltage, implying that charge carrier injection at the 2L-WS_2/Pd interfaces transits from thermionic-limited to band-like transport regimes. The effective Schottky barrier height was extracted using the thermionic emission equation

$$I_D = A^{**}T^{1.5}\exp\left[-\frac{1}{k_BT}(\Phi_{SB} - qV_{DS})\right] \quad (1)$$

where A^{**} is the Richardson constant for a 2D system, T is the temperature and the exponent of 1.5 applies for 2D semiconductors, k_B is Boltzmann's constant, Φ_{SB} is the effective Schottky barrier height, and qV_{DS} is the product of the electronic charge and drain-to-source voltage.

Figure 6b shows an Arrhenius plot, where $\ln(I_D/T^{1.5})$ is plotted against $1000/T$, spanning temperatures from 160 to 300 K at various gate voltages and V_{DS} = +0.1 V. The linear fit of $\ln(I_D/T^{1.5})$ vs $1000/T$ provides slopes corresponding to the barrier height at each V_{GS} and V_{DS} condition. The slopes are expressed as $-(1000/k_B)(\Phi_{SB} - qV_{DS})$. The determined barrier heights are further analyzed by extracting the slopes from the linear fits in Figure 6b, and a drain-bias-dependent Arrhenius plot was constructed, representing slope vs V_{DS}, as shown in Figure 6c. Finally, to obtain the effective barrier height vs V_{GS}, linear fits from Figure 6c are extrapolated to V_{DS} = 0 V. The results, barrier height vs gate voltage, are shown in Figure 6d. The effective flat-band barrier height of ~70 meV is estimated from the energy barrier value where the barrier height vs gate voltage starts deviating from the linear fit. Although a barrier height exists at the contact interface, consistent with the results observed in Figure 3d, the effective barrier height can be easily modulated by the gate voltage and quickly drops to 0 at V_{GS} = +2 V. The observation is consistent with the thermionic-field-emission model. Following the same procedure, the effective flat-band barrier heights of the 1L-WS_2 MOSFET with 2L-WS_2 contact and the all-1L-WS_2 MOSFET are extracted as 80 and 110 meV, respectively (Figure S8). The results align with the observation of enhanced contact quality for the 2L-WS_2 contacts.

The temperature-dependent field-effect mobility, μ_{FE}, is extracted from the peak linear transconductance (Figure S9). In the case of the 2L-WS_2 MOSFET, the mobility increases from 36.9 $cm^2/(V\ s)$ at T = 300 K to 52.5 $cm^2/(V\ s)$ at T = 200 K following an approximate temperature dependence of

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mobility $T^{-1.3}$, consistent with phonon-limited transport. Similarly, a temperature dependence of mobility proportional to $T^{-1.5}$ is observed in the 1L-WS_2 MOSFET with 2L-WS_2 contacts. However, the all-1L-WS_2 MOSFET exhibits a more temperature-independent mobility, likely limited by the contact quality. Additional temperature-dependent and comparison results for the devices in Figures 3−5 are provided in Figures S10 and S11.

The reproducibility of high-performance WS_2 MOSFETs was investigated on another distinct batch of 2L-WS_2 grown via the two-step CVD process described above. The composition of this sample was likewise assessed through cross-sectional TEM and EDX. The results similarly demonstrated the presence of a 2L-WS_2 with prominent signals for W and S (Figure S12). A bottom-gated device (EOT = 30.6 nm and L_{DS} = 0.4 μm) was fabricated using the method described in the experimental section but using Ni/Au (10/100 nm) for the source/drain electrodes. Transfer and output characteristics of the device at RT are shown in Figure S13. The device demonstrated a high drive current of 240 μA/μm at V_{GS} = +20 V and V_{DS} = +3.1 V, which is comparable to the device shown in Figure 3. Furthermore, the devices displayed excellent stability over time. The device shown in Figure 3 was measured after 13 months of storage in air (Figure S15), and it maintained an $I_{D(SAT)}$ of 274 μA/μm at V_{DS} = +3.1 V, V_{GS} = +20 V, and RT, which is close to the initial measurement of 280 μA/μm.

The reason for the improved contacts using 2L-WS_2 is expected given the narrower band gap and higher electron affinity compared to 1L-WS_2 (Figure S16), which should reduce the potential barrier at the metal−WS_2 interface.[14,29,30] The presence of the second layer of WS_2 also serves to protect the underlying WS_2 and prevents the introduction of inevitable defects during device fabrication and metallization. Our contacts are also gated by the substrate gate, and electrostatic gating underneath the contacts is expected to be more effective in the 2L-WS_2 sample since the lower layer is less influenced by MIGS. We believe that these combined effects allow the 2L-WS_2 regions to have lower contact resistance compared to 1L-WS_2.

CONCLUSIONS

In conclusion, we have presented an innovative two-step CVD approach for improving the performance of WS_2 MOSFETs. The devices fabricated on 2L-WS_2 and 1L-WS_2 with 2L-WS_2 contacts exhibit high-performance characteristics even with traditional directly deposited metallic contacts. The best-performing 2L-WS_2 device displayed an I_{ON}/I_{OFF} ratio of 10^8 and a saturated drive current of 280 μA/μm at RT and 386 μA/μm at 78 K, over an order of magnitude higher compared to devices fabricated on 1L-WS_2. These results underscore the crucial role of 2L-WS_2 beneath the contacts in achieving an exceptional device performance. The devices also exhibited performance comparable to previously reported devices with semimetallic Bi contacts but at the same time overcoming the thermal stability concerns associated with semimetallic Bi contacts and exhibiting exceptional long-term stability. This contact strategy employing 2L-WS_2 grown through a two-step CVD process presents an alternative approach for achieving high-performance TMDC-based MOSFETs that are highly compatible with the existing semiconductor manufacturing industry.

METHODS

CVD of 1L-WS_2 on Sapphire. Monolayer WS_2 was synthesized on a *c*-plane sapphire substrate in a two-zone 3 in. tube furnace (planarTECH). The sapphire substrate was cleaned in Piranha solution (concentrated H_2SO_4/30 wt % H_2O_2 = 3:1) for 12 h, then rinsed with isopropyl alcohol, and dried by N_2. The sapphire substrate was placed on an alumina crucible with the growth side face-up. The crucible was positioned in the middle of the downstream furnace. An alumina crucible (50 × 20 × 20 mm) containing 1.0 g of WO_3 powder was placed in the middle of the upstream furnace. An alumina crucible containing 0.8 g of sulfur powder was placed upstream out of the furnace heating zone. A hot plate was set beneath the sulfur source with the heating surface in contact with the bottom tube. After loading, the tube was evacuated and purged by Ar gas, and then Ar and H_2 gases were supplied at rates of 120 and 10 sccm (standard cubic centimeters per minute), respectively. The pressure in the tube was stabilized at 6.0 Torr. The upstream furnace was ramped to 900 °C in 25 min, and the downstream furnace was ramped to 980 °C in 25 min. The sulfur source was heated to 150 °C after both furnaces reached set temperatures. Sulfur powder melted in 15 min. The reaction was held for 180 min. Then, the heat components of both furnaces were turned off, and the furnaces were slowly cooled below ∼850 °C. The tube furnace was then rapidly cooled down to RT by turning off the hot plate and opening both furnace lids.

CVD of the Second Layer TMDC on 1L-WS_2. The second layer TMDC was synthesized on the 1L-WS_2 grown on *c*-plane sapphire from the previous step in a separate 2 in. tube furnace (ThermoFisher Blue M). 200 mg of Nb_2O_5 powder and 20 mg of NaCl were mixed in an alumina crucible. The 1L-WS_2 sample was placed on the crucible with the 1L-WS_2 side facing downward and positioned in the middle of the furnace. Another alumina crucible containing 800 mg of sulfur pieces was placed upstream out of the furnace heating zone. The tube where the sulfur source was located was wrapped by heating tape. Prior to the reaction, the tube was evacuated and purged by Ar gas. Then, Ar gas was supplied to the tube, until the pressure in the tube reached atmospheric pressure. Ar and H_2 gases were adjusted to 120 and 2 sccm, respectively. The tube furnace was ramped up to 790 °C in 42 min. The sulfur source was heated to 200 °C when the temperature in the tube furnace reached 790 °C and sulfur pieces melted in 5 min. The reaction was held for 15 min and terminated by turning off heating components of the furnace and heating tape. Ar gas flow rate was increased to 150 sccm, and the lid of the furnace was opened to cool the tube furnace to room temperature rapidly. While the addition of Nb_2O_5 during growth was originally intended to promote the formation of NbS_2 as the second TMDC layer, it was observed that only WS_2 was grown, and that no Nb could be observed above the detection limit of the EDX system. We suspect that residual WO_x from the first growth of WS_2 on the substrate might have served as the source of W for the growth of the second-layer WS_2, and this could be the reason why only a few small islands of WS_2 were regrown.

Transfer of Multilayer WS_2 Film. The sapphire substrate with the multilayer WS_2 film was spin-coated with PMMA and then baked at 180 °C for 90 s. The edges of the sample were scratched using a razor blade and immersed in a 90 °C, 25% KOH solution for 20 min to initiate separation of the PMMA/

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WS_2 stack from the sapphire substrate. Then, the sample was transferred and rinsed in DI water. DI water was used to complete the separation of the PMMA/WS_2 stack from the substrate through the surface tension of water. The PMMA/WS_2 stack was rinsed in DI water tree times and transferred onto the target substrate [Al_2O_3(30 nm)/SiO_2 (16 nm)/Si] and baked at 50 and 120 °C for 20 min each to remove moisture and enhance the adhesion of WS_2 to the substrate. The transfer was completed by immersing the sample in acetone for 6 h to remove PMMA.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.4c04431.

Summary of high-performance CVD 1L- and 2L-WS_2 MOSFETs; calculation of EOT of bottom-gated and dual-gated devices; Raman analysis of 1L-WS_2 and 2L-WS_2; AFM measurement of 1L-WS_2 film; cross-sectional TEM characterization of 2L-WS_2 MOSFETs with Pd and Ni electrodes; transconductance and field-effect mobility comparison; output characteristics of 1L-WS_2 devices with 2L-WS_2 contacts vs. Bi contacts; barrier height measurements and temperature-dependent field-effect mobility; on-current comparison; additional data on 1L- and 2L-WS_2 MOSFETs with Ni and Pd contacts; long-term stability measurements; band diagram explanation of contact difference (PDF)

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Notes

The authors declare no competing financial interest.

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