

The planar anodic Al₂O₃-ZrO₂ nanocomposite capacitor dielectrics for advanced passive device integration

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ABSTRACT

The need for integrated passive devices (IPDs) emerges from the increasing consumer demand for electronic product miniaturization. Metal-insulator-metal (MIM) capacitors are vital components of IPD systems. Developing new materials and technologies is essential for advancing capacitor characteristics and co-integrating with other electronic passives. Here we present an innovative electrochemical technology joined with the sputter-deposition of Al and Zr layers to synthesize novel planar nanocomposite metal-oxide dielectrics consisting of ZrO₂ nanorods self-embedded into the nanoporous Al₂O₃ matrix such that its pores are entirely filled with zirconium oxide. The technology is utilized in MIM capacitors characterized by modern surface and interface analysis techniques and electrical measurements. In the 95–480 nm thickness range, the best-achieved MIM device characteristics are the one-layer capacitance density of 112 nF·cm⁻², the loss tangent of 4·10⁻³ at frequencies up to 1 MHz, the leakage current density of 40 pA·cm⁻², the breakdown field strength of up to 10 MV·cm⁻¹, the energy density of 100 J·cm⁻³, the quadratic voltage coefficient of capacitance of 4 ppm·V⁻², and the temperature coefficient of capacitance of 480 ppm·K⁻¹ at 293–423 K at 1 MHz. The outstanding performance, stability, and tunable capacitors' characteristics allow for their application in low-pass filters, coupling/decoupling/bypass circuits, RC oscillators, energy-storage devices, ultrafast charge/discharge units, or high-precision analog-to-digital converters. The capacitor technology based on the non-porous planar anodic-oxide dielectrics complements the electrochemical conception of IPDs that combined, until now, the anodized aluminum interconnection, microresistors, and microinductors, all correlated in one system for use in portable electronic devices.

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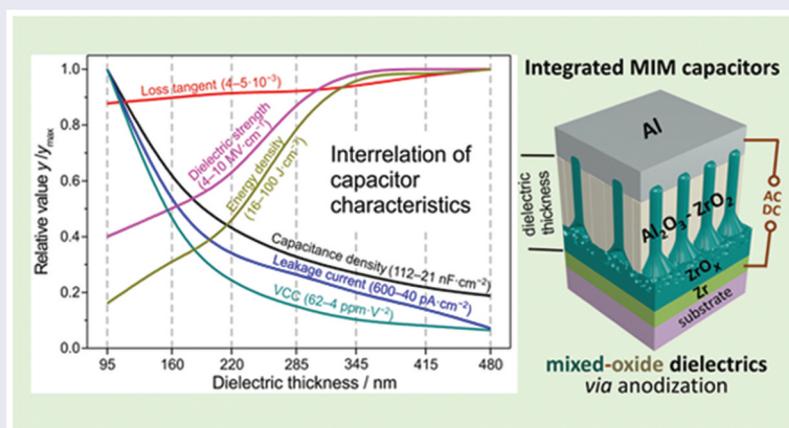
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Advanced technology for novel nanocomposite metal-oxide dielectrics utilized in integrated MIM capacitors with cutting-edge performances for multipurpose applications

1. Introduction

Modern portable electronic devices (PEDs) such as smart wearable gadgets, personal digital assistants, multi-media and biomedical appliances, various automotive and aerospace devices, or unmanned aerial vehicles still consist of many discrete passive components: resistors (R), inductors (L), capacitors (C), or modules [1,2]. Those components may occupy up to 40% of the surface of a second-level package substrate, such as a printed circuit board (PCB) or a multichip module (MCM) [3]. To reduce the number of discrete passives and make PEDs substantially smaller and lighter, the concept of *Integrated Passive Devices* (IPDs) has been implemented [3–5]. In this concept, all R , C , and L components, interconnection, or their combinations are integrated into a single layer or incorporated in a multilayer structure assembled on top of a bare chip or a substrate with active integrated circuits (PCB, MCM, hybrid integrated circuits, or chiplet modules) [6–8]. IPDs can potentially fully substitute discrete-components-based solutions such as through-hole or surface-mount devices. The miniaturization of PEDs using IPDs improves the precision of passives, shortens and narrows interconnections, and contributes to smaller tolerances of elements' characteristics, thus making IPDs especially attractive for impedance matching, filtering, and coupling/decoupling circuits [6,7,9]. IPDs are also actively used in designs with high input/output pin count for achieving electromagnetic interference (EMI) filtering or electrostatic discharge (ESD) suppression [10].

The technology and fabrication sequence for all passives must allow their mutual compatibility for co-integration on various substrates such as ceramics, glass plates, silicon wafers, or even flexible polymer cards [8]. IPDs are generally produced using standard microfabrication technologies: physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), wet and dry chemical or plasma-chemical etching, and lithographic techniques [2,3,11]. Notably, these approaches require more complex efforts to planarize the layers and blend them in multilayer stacks [12,13].

Advancing the existing methodologies and developing new materials, technologies, and assembly techniques are vital enablers for IPDs. *Electrochemical anodizing* [14] is a versatile and cost-effective approach capable of challenging commonly used technologies. ALD, PVD, and CVD are typically power-consuming methods with complicated processing steps, requiring high vacuum and elevated temperatures, high-budget equipment, and non-eco-friendly precursors [3,15]. Contrarily, anodizing is a cost-effective, easy-to-implement, and eco-friendly method used at ambient conditions to produce oxide films with tunable properties [14,16]. *Selective anodizing* of

aluminum has been proposed to make self-planarized Al interconnection via the anodic oxidation of Al layers [17] and Al/Hf bilayers [18] on substrates. In both cases, the gaps between the Al lines were filled with porous anodic alumina (PAA) that served as a low- k planarizing dielectric. The approach was further advanced to create a two-layer Al interconnection package comprising the interlevel low- k dielectric fabricated entirely via the selective anodizing of Al layers [19] or Al/Ta metal stacks [20]. In pursuit of new applications, selective anodizing processes were developed for fabricating thin-film resistors [21,22], inductors [23], and low-value capacitors [23,24] from Al, Al-Si alloy, and Al/Ta bilayers on substrates. Although the proof-of-concept for utilizing the selective anodizing and PAA-based dielectrics for IPDs has experimentally been justified in the early works [17–24], a significant technology limitation for anodic fabrication of high- k PAA-based dielectrics is associated with their porous structure [24]. The presence of pores lessens the capacitance density, worsens the dielectric performance, and makes the nanofabrication of further layers over such surfaces challenging.

Capacitors are vital electronic components of RCL networks that serve as building blocks for high-frequency electronic devices such as oscillators, impedance matching circuits, passive filters (high-pass, low-pass, band-pass, band-stop, or all-pass), couplers and baluns, power combiners/dividers, EMI/ESD components, and resonant circuits [1–3]. It is essential to develop state-of-the-art anodizing technologies for metal-oxide dielectrics incorporated into planar metal-insulator-metal (MIM) capacitors to complement the existing anodizing technologies for IPDs. High-permittivity metal oxides (Nb_2O_5 , TiO_2 , Ta_2O_5 , HfO_2 , and ZrO_2) have long been considered prospective candidates for building thin-film high- k capacitor dielectrics [25,26]. It has been a challenge to fabricate PAA-embedded, self-planarized, and *entirely non-porous* dielectrics based on these high- k metal oxides and co-integrate them with other anodized passives and interconnection in multilayers onto package substrates. Developing the anodizing technology to produce such planar nanocomposite dielectrics is anticipated to result in materials with a rare combination of essential properties like high capacitance and energy density, improved dielectric strength, non-dispersive, low-loss, low-leakage-current characteristics, high electrical and thermal stability, accuracy, and tunability of properties to meet the requirements for advanced PED applications.

In the present work, we have developed an electrochemistry-based technology to synthesize non-porous nanocomposite films consisting of ZrO_2 nanostructures self-incorporated into the PAA layers such that the alumina nanopores are filled with zirconium oxide to form fully planar Al_2O_3 - ZrO_2 mixed-oxide films. For

the first time, the films have been integrated as the high- k nanocomposite dielectric in on-chip MIM microdevices. The choice of material was motivated by the generally attractive dielectric properties of both ZrO_2 and Al_2O_3 , complemented by the enhanced properties of the Al_2O_3 - ZrO_2 dielectrics utilized in an experimental electrolytic capacitor design [27]. The anodic films and test MIM devices have been examined by scanning electron microscopy (SEM), X-ray photoelectron spectroscopy (XPS), X-ray microdiffraction (XRD), electrochemical impedance spectroscopy, and electrical/dielectric measurements in a frequency range of 10^{-2} – 10^6 Hz at temperatures ranging 293–523 K. An array of integral capacitors utilizing the new dielectrics has been modeled in pursuit of creating the missing technology to complement the anodizing conception of passive device integration for PEDs.

2. Methods

2.1. Anodic-film fabrication

A standard one-side polished 4" Si wafer covered with a thermally grown 380 nm-thick SiO_2 layer was used as the starting substrate. The magnetron sputtering of Zr (99.95%) and Al (99.999%) targets was carried out to subsequently deposit a 160 nm-thick zirconium layer followed by a 500 nm-thick aluminum layer (hereafter the Al/Zr bilayer). The wafer with the deposited Al/Zr bilayer was cut into ca. 2 cm \times 2 cm pieces, which were individually anodized in a cylindrical polytetrafluoroethylene two-electrode bath with a circular working area of 1.8 cm² (1.5 cm in diameter). Additional details on the anodizing setup are described elsewhere [28]. An aqueous 0.6 M solution of oxalic acid ($\text{H}_2\text{C}_2\text{O}_4$) was used as the anodizing and re-anodizing electrolyte. The *anodizing* was carried out at room temperature (295 K) by potentiodynamic polarization from 0 to 40 V with a rate of 0.5 V s⁻¹, followed by potentiostatic polarization at 40 V for 5 min. Immediately following the anodizing, the *re-anodizing* was carried out via a high-speed potentiodynamic polarization (10 V s⁻¹) to a higher voltage selected from a range of 80–320 V. Upon attaining the desired voltage value, the voltage was stabilized for 5 min to ensure uniform oxide growth across the whole sample surface. This combination of electrical and electrolytic conditions for processing the Al/Zr bilayer was justified in the previous work [27]. The samples were then thoroughly washed with Milli-Q® ultrapure water, dried in a cool nitrogen stream, and placed in an oven preheated to 393 K for 1 h to fully desorb the moisture from the alumina nanopores. The samples were then immersed in 1 wt.% NaOH solution at 295 K for 5 minutes to dissolve the empty (not filled with zirconium oxide) pores. Finally, the samples were thoroughly washed and dried, as mentioned above.

2.2. MIM device fabrication

Test MIM capacitors were assembled using lift-off photolithography and the magnetron sputter-deposition of aluminum to form top electrodes. Image reversal photoresist AZ5214E (MicroChemicals GmbH, Germany) was spin-coated onto the samples and exposed through a photomask, which resulted in a \sim 1.5 μm -thick patterned photoresist layer over the planar film surface. A layer of aluminum was deposited using DC magnetron sputtering system. The photoresist lift-off process was performed in dimethyl sulfoxide at 333 K, enhanced by ultrasonic vibration. In the assembly, the unoxidized zirconium metal layer that remains between the substrate and the anodic film served as the bottom electrode.

2.3. SEM analysis

The morphologies of the anodic films and MIM capacitors were examined in a MIRA II (TESCAN) scanning electron microscope operated at 30 kV. Cross-sections of the anodic films and assembled capacitors were observed in a Verios 460L (Thermo Fisher Scientific) instrument operated at 15 kV. Both instruments were equipped with an InBeam detector for secondary electrons, so charge-reducing conducting layers were not deposited before the observation.

2.4. XRD analysis

Diffraction patterns of the anodic films were taken from a Bruker-AXS D8-Discover diffractometer, equipped with a parallel incident beam (Göbel mirror), a vertical θ - θ goniometer, an XYZ motorized stage, and a General Area Diffraction System (GADDS). The samples were analyzed in the reflection mode, and the area of interest was selected with a video-laser-focusing system. An X-ray collimator of a 500 μm system allowed the analysis of a mean area represented by an ellipsoid with a constant short axis of 500 μm and a variable long axis of 600–1500 μm . The diffractometer was operated at 40 kV and 40 mA to generate CuK α radiation. The VÅNTEC-500 detector (silicon strip technology, active area of 30 cm \times 30 cm, frame size of 2048 pixels \times 2048 pixels) was placed at a 15-cm distance from the sample. Sixteen frames were collected in reflection mode covering 26–38° 2θ with a step size of 0.8° to obtain a conventional 2D diffractogram suitable for Rietveld analysis [29]. The exposure time was 300 s per frame, and it was γ -integrated to generate the 2θ vs. intensity diffractogram. The experimental diffractograms were fitted with the crystal structure [30] for the phases identified with the aid of TOPAS 6.0 software (Bruker AXS GmbH, 2017) [31]. The wt.% of the phases involved was estimated by refining the Rietveld scale factor and applying the corresponding formulas [32].

2.5. XPS analysis

The chemical composition of the selected anodic films was analyzed by XPS in a Kratos Axis Ultra DLD spectrometer employing a monochromatic Al K α source. Typical operating pressures were less than $1.3 \cdot 10^{-9}$ mbar. The emitted electrons were detected by a hemispherical analyzer at fixed pass energies of 160 and 20 eV for the survey and high-resolution spectra, respectively. CasaXPS software version 2.3.24PR1.0 was used for spectra analysis. Before recording XPS spectra, the samples were heated in the XPS chamber at 423 K to desorb water molecules from the sample surface. Further details are reported elsewhere [33].

2.6. Electrical characterization

Electrical characterization of test MIM capacitors was performed using a Cascade Microtech MPS 150 probe station. Room-temperature measurements were performed in a 10^2 – 10^6 Hz frequency range using an Agilent Technologies Precision LCR Meter E4980A. A custom-made heating platform was employed for electrical measurements in the 293–523 K temperature range. Selected MIM capacitors were tested in an extended frequency range of 10^{-2} – 10^6 Hz using an impedance analyzer Metrohm Autolab PGSTAT204 equipped with the AG FRA32 M module and a Faraday cage. The breakdown voltage was measured using a Keithley 2410 SourceMeter Instrument at room temperature. The DC conductivity, current-voltage (J – V) curves, and capacitance-voltage (C – V) curves were recorded using a Keithley 4200A-SCS Parameter Analyzer supporting the automated real-time parameter extraction, data graphing, and analysis functions. All electrical testing was carried out using the Al top metal as a cathode.

3. Results and discussion

3.1. Device modeling and assembling

The general approach for forming nanostructured metal oxides via the anodizing of a layer of Al superimposed on a layer of a different valve metal, the so-called PAA-assisted anodization, has been pioneered and advanced by some of the present authors in a series of previous works [33–37], including the recent and most challenging case of the Al/Zr bilayer [38]. A PAA film is first formed by anodizing the upper Al layer. The pore pattern may then affect the anodization of the underlying metal under appropriate electrical and electrolytic conditions. An array of metal-oxide nanostructures may grow under the alumina barrier layer, simultaneously pushing their way outward, partly filling the pores proportionally to the applied voltage until a dielectric breakdown occurs.

Typically, the PAA-assisted anodic-oxide nanostructures are deep-located inside the pores, such that the upper volume of pores remains free from the underlying metal oxide [35]. Some deep-located oxides (Ta $_2$ O $_5$ [39], HfO $_2$ [40], and ZrO $_2$ [27]) behave as nearly ideal dielectrics when measured by electrochemical impedance spectroscopy in solution. Such PAA-inbuilt films are advantageous for electrolytic capacitors as the empty pores above the oxide nanocolumns serve as a spacer and collector for a liquid or gel-like electrolyte [27,40]. However, a planar non-porous anodic oxide film is required for MIM capacitor fabrication. In a planar film, anodic zirconium oxide should completely fill the alumina nanopores up to the general surface of the PAA layer, leaving no empty pores at the air/film interface. The difficulties with the fabrication of such a film arise because the surface of a PAA film has a disordered porous structure owing to the irregular pore formation at the commencement of anodic film growth. About half of the surface pores stop growing before a steady-state pore-formation regime is established [14,41]. The terminated pores cannot be filled with oxide of the underlying metal and, therefore, will remain empty during re-anodizing. For achieving a higher degree of pore self-ordering, a two-step anodizing process [42] or a set of specific electrical and electrolytic conditions [43] may theoretically be tried. However, neither of the above approaches would be effective with the limited thicknesses of the magnetron sputter-deposited Al films and the resultant PAA layers. In the case of the Al/Zr bilayer, the formation of a planar anodic film is even more challenging since the PAA overlayer is a key enabler for the upward growth of ZrO $_2$ nanorods: the Zr $^{4+}$ transport number becomes abnormally high (~ 0.26) due to the location of the oxide inside the pores and the suppression of oxide crystallization inside the pores, as was explained in detail elsewhere [38]. Preliminary experiments have shown that the PAA-assisted zirconium-oxide nanorods stop growing within the pores before they reach the alumina surface. Consequently, the formation of the planar anodic film via directly re-anodizing the Al/Zr bilayer is practically impossible. Therefore, we have developed an alternative, facile, and highly reproducible approach for forming a planar PAA-inbuilt dielectric integrated into a MIM capacitor, outlined in a series of computer-aided 3D (upper row) and corresponding 2D images in Figure 1.

The initial film formation steps include the sputter-deposition, aluminum anodizing, and anodic processing of the Zr underlayer (Figure 1(a–d)), generally following the procedure developed in our previous work [27]. Briefly, the Al layer is first converted into a PAA film; this is immediately followed by the local oxidation of the Zr underlayer through the alumina

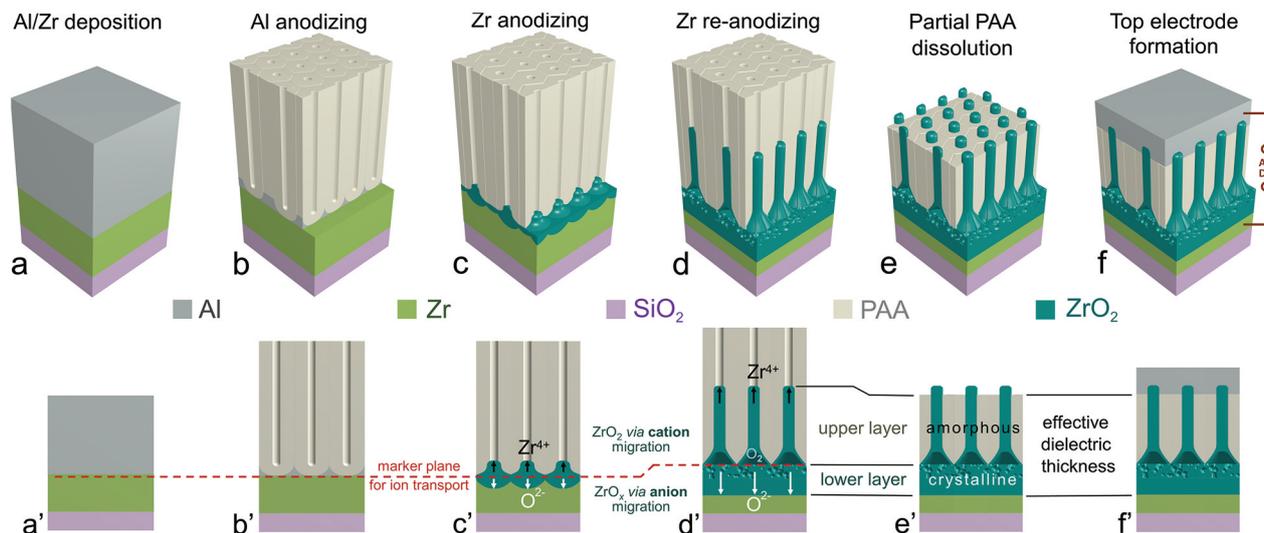


Figure 1. Modeling the growth of a planar nanocomposite dielectric and its incorporation into a test MIM device: (a) the sputter-deposition of an Al/Zr bilayer, (b) the anodizing of the Al layer to form a PAA layer, (c) the PAA-assisted *anodizing* of the Zr underlayer to grow zirconium-oxide nanohillocks, (d) the PAA-assisted *re-anodizing* of the Zr underlayer to transform the hillocks into the nanorods and form a lower oxide layer, (e) partial PAA dissolution in a selective etchant to planarize the film, (f) the formation of a top Al electrode. Images in the lower row (a'–f') show 2D sections of the anodic film at the different stages for forming the dielectric and assembling the MIM device.

barrier layer resulting in an array of ZrO_2 nanohillocks that grow within the alumina barrier layer (Figure 1(c)). To make the oxide develop further inside the pores, re-anodizing is carried out to a higher voltage relative to that used for forming the PAA layer. During the voltage rise, the Zr layer is further oxidized, and new amorphous anodic oxide continuously forms and fills the pores due to the outward migration of Zr^{4+} ions (Figure 1(d)). This process competes with the widening of the nanorod bases (nanocrystalline zirconium oxide) beneath the marker plane due to the inward migration of O^{2-} ions. The position of the marker plane was justified in previous works on anodizing/re-anodizing valve-metal bilayers, including the Al/Zr couple [33,37–39]. The bases gradually merge since more zirconium is exposed to oxidation under the plane. After holding the voltage at the designated value for a while, the zirconium-oxide protrusions become well interconnected and buffered from the remaining Zr metal by a thin and relatively uniform zirconium-oxide lower layer, whose thickness is determined by the re-anodizing voltage. Further details of the zirconium-oxide nanorod formation mechanism and interrelation between the film layers are presented elsewhere [27,38,44].

Next, a novel approach is introduced to planarize the anodic film. The empty (unfilled with the zirconium oxide) pores are chemically dissolved in 1 wt.% NaOH aqueous solution until the tops of the zirconium-oxide nanorods slightly protrude over the surface of the remaining alumina layer (Figure 1(e)). In such a film, the lower layer, which forms under the pores due to the inward migration of O^{2-} ions, is crystalline zirconium oxide. The upper layer, which grows due to the outward

migration of Zr^{4+} cations, is composed of rod-like protrusions of amorphous zirconium oxide fully filling the pores. The presence of O_2 -filled voids in the nanorod bases is associated with the oxidation of the migrating O^{2-} ions on the ZrO_2 nanocrystallites beneath the alumina barrier layer, generation of O_2 gas, and partial dissociation of the Al–O bonds under the high electric field as described in detail in previous works on anodizing of Al/Si [45], TiNb [46], or TiN [47] substrates. The formation of a sponge-like bottom sublayer that thickens proportionally to re-anodizing voltage is another feature revealed in this work during the anodizing/re-anodizing of the Al/Zr metal layers. The cavities in the sponge are likely to be filled with oxygen gas because they are most probably generated due to the oxygen evolution on the zirconium-oxide crystallites composing the bottom sublayer of the lower film layer [27]. Obviously, the formation of voids and cavities within the oxide nanorods and the lower oxide layer influence the cation and anion transport numbers during the re-anodizing. Moreover, the transport numbers likely depend on the re-anodizing voltage because the size of the O_2 -filled voids increases with increasing re-anodizing voltage. Detailed consideration of the impact of the anodizing/re-anodizing conditions on the ionic transport in the zirconium-oxide nanorods relevant to the present case is presented elsewhere [27,38].

After the sputter-deposition of a top aluminum electrode (Figure 1(f)), the upper parts of the rods, protruding from the surface of the remaining alumina, become short-circuited by the upper metal. The effective dielectric thickness and the electrical metal/oxide interface are defined as marked in Figure 1(f).

Notably, regardless of the re-anodizing voltage, the same pore-dissolution treatment is applied to all the films. No matter how long the rods grow, the same dissolution conditions are needed to dissolve the empty part of the pores. Therefore, there is no need to adjust the thickness of the initial Al layer to achieve a particular thickness of the anodic-oxide dielectric. This feature significantly simplifies the technology and guarantees the result.

Selected on-chip capacitors were examined by SEM. Figure 2(a) shows a panoramic top SEM view of a representative sample designed to be diced in 4 identical chips comprising an assembly of MIM capacitors having the same bottom electrode (non-anodized Zr metal) and separated top electrodes (Al metal) of various areas fabricated by the sputter-deposition and lift-off photolithography. Figure 2(b) shows a top electrode, 0.8 mm² in size. The electrode has well-defined edges at the micro- and nanoscale, as seen in detailed views of Figure 2(c,d). Figure 2(e,f) demonstrates examples of panoramic cross-sectional views of typical fragments of the electrode-free and electrode-covered areas of a MIM capacitor. The anodic film is of a uniform thickness and has a microscopically flat surface without defects or physical imperfections. The sputter-deposited Al layer looks uniform across the fragment's

surface and is ~200 nm thick, measuring out of the level of the alumina surface, as was expected from the magnetron sputtering setup. No hillocks are observed over the Al surface, which makes the film stack perfectly suitable for forming further layers on top of it if necessary. The upper and lower film layers and the underlying Zr layer, as marked in the schematic of Figure 1, are well identified in the high-resolution images in Figure 2(h,i). The surface views of Figure 2(e,g) confirm that the rods reside inside the hexagonal alumina cells. One may see that the alumina cells are sufficiently self-organized, and all the pores are filled with anodic zirconium oxide. From Figure 2(i), the rod tops are covered by aluminum such that the metal is in direct physical contact with the alumina surface surrounding the rods. The aluminum metal conformally covers the surface of the anodic film so that the size of the Al grains fits the size of the horizontal projections of the PAA cells (Figure 2(g,j)). Therefore, the approach for forming the planar nanostructured mixed-oxide anodic films incorporated in a MIM microdevice is experimentally justified.

3.2. Dielectric's structure and composition

As shown in the previous study [27], the lower film layer has a complex structure comprising a nanosponge-like

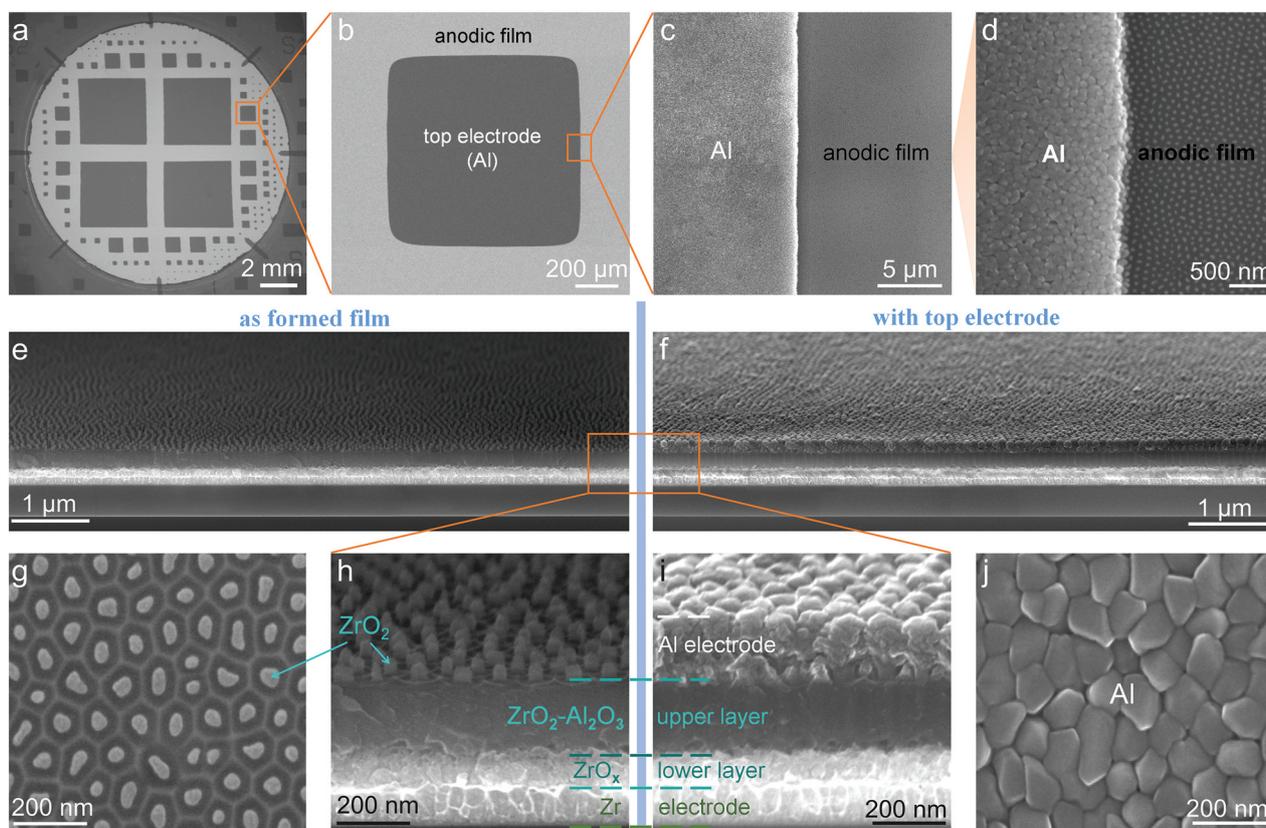


Figure 2. SEM views of MIM microdevices utilizing a planar Al₂O₃-ZrO_x nanocomposite film: (a) panoramic top-view of a four-chip assembly of test devices within a circle of 1.5 cm in diameter made by combining the sputter-deposition on a SiO₂/Si wafer, anodizing (40 V), re-anodizing (200 V), and lift-off photolithographic techniques, (b) zoomed-in image of an individual capacitor, which is further elaborated in panels (c) and (d). Cross-sectional and surface views of fragments of the anodic-oxide dielectric between and under a top electrode are shown in (e-h) and (f-j), respectively.

sublayer laminated with a solid continuous anodic zirconium oxide which is in contact with the remaining zirconium metal. Although it was revealed by TEM analysis that the upper layer consists of fully amorphous anodic oxides and the lower layer comprises nanocrystallites and non-stoichiometric oxide [27], the exact crystal phases and bonding states in the zirconium oxides were not identified and, therefore, became the subject of the present study. Figure 3(a,b) shows the experimental and curve-fitted narrow-scan Zr 3d and O 1s XP spectra collected at the surface of a representative anodic film made by re-anodizing to 240 V, after the PAA layer was selectively and fully dissolved away, as shown in the inserted sketch. The absence of the PAA matrix enabled the analysis of the chemical composition and bonding states of zirconium oxide in the nanorods and partly in the sponge-like lower layer. The C 1s surface spectrum (not shown) was charge-corrected to give the adventitious C 1s spectral component (C–C, C–H) binding energy of 285.0 eV. The peak-fitting of the C 1s spectrum was performed as described elsewhere [33] to disclose the features of atmospheric surface contamination and possibly identify the presence of electrolyte-derived species such as oxalate ions from the anodizing electrolyte [44]. The Zr 3d_{3/2} peak for each species was constrained at a fixed energy increment of 2.40 eV above the Zr 3d_{5/2} peak with a fixed intensity ratio of 3:2 [48]; further details of Zr 3d spectra analysis are reported elsewhere [38].

The Zr 3d surface spectrum in Figure 3(a) is perfectly fitted with two spin-orbit doublets (Zr 3d_{5/2} and Zr 3d_{3/2}). The higher-energy dominating doublet of symmetric lineshapes (Zr 3d_{5/2} at 182.80 eV) is assigned to the Zr⁴⁺ oxidation state in ZrO₂ (~86 at.%) [49]. The second doublet, shifted to –1.30 eV from the higher-energy component, indicates the formation of zirconium suboxide, which may be referred to as ZrO_x (1.5 < x < 2). Following the previous interpretations of Zr 3d peaks [38], Zr³⁺ may be assigned for the lower limit of x (Zr₂O₃). Alternatively or additionally, the

manifestation of the lower-energy peak may be associated with oxygen vacancies in ZrO₂.

The presence of oxygen vacancies in zirconium dioxide is also assumed from the analysis of the O 1s spectrum (Figure 3(b)). The main component at 530.80 eV is associated with O^{2–} in the lattice of ZrO₂ [38]. The highest-energy peak at 532.50 eV, shifted to +1.70 eV from the main component, may be attributed to oxygen vacancies in ZrO₂ because, as suggested elsewhere [50], the kinetic energy of an oxygen atom adjacent to an oxygen vacancy is different from that of an oxygen atom in a stoichiometric compound. Assuming the absence of adsorbed water molecules and a negligible amount of hydroxyl groups in the oxide, the feature at 532.50 eV may be assigned to O^{2–} ions located near oxygen vacancy sites (up to 34 at.%), in agreement with the conclusions of Holgado et al [51,52]. The lowest-energy peak in the O 1s spectrum (529.10 eV, 5.5 at.%) is associated with O^{2–} coordinated in negatively charged oxalate ions C₂O₄^{2–} incorporated into oxide composition during the anodizing/re-anodizing [53].

Figure 3(c) shows the observed, calculated, and difference diffractograms in the range of 26–39° 2θ angles of a planar anodic film grown via the PAA-assisted anodizing as outlined in inserted sketch and modeled in Figure 1(e). The diffractogram is best interpreted with the presence of metallic α-Zr (P6₃/mmc space group) in a dominating amount of 52.9 wt.% and two oxide phases: monoclinic ZrO₂ (P2₁/c space group) and orthorhombic ZrO₂ (Pnam space group) in the amount of 21.3 and 25.8 wt.%, respectively. The 2D diffractogram (inset in Figure 3(c)) revealed that at least α-Zr and orthorhombic ZrO₂ phases are oriented as the intensities of their Debye rings are not constant along the γ angle. Although it is not straightforward to judge on the orientation of the monoclinic ZrO₂ phase, all the phases were corrected with the March-Dollase model for preferred orientations in the following directions: α-Zr – <001>, monoclinic ZrO₂ – <011>, and orthorhombic ZrO₂ – <11–1>. The

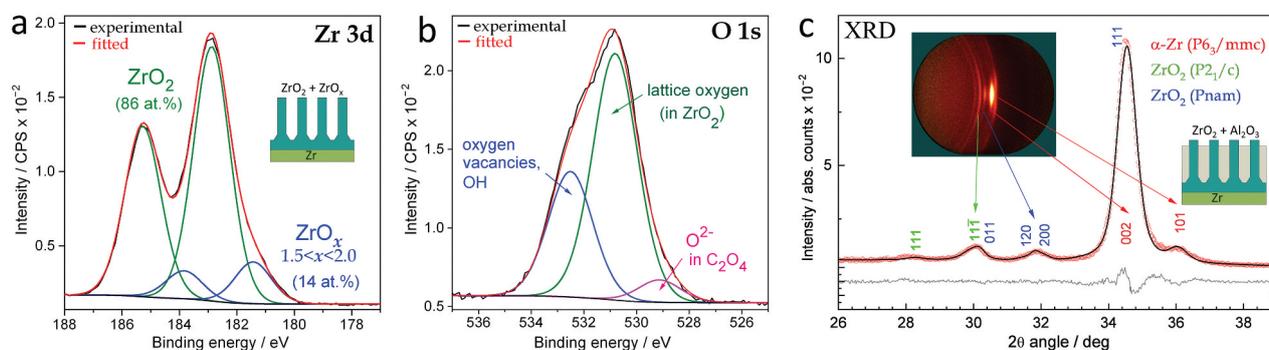


Figure 3. Experimental and curve-fitted (a) Zr 3d and (b) O 1s narrow-scan XP spectra of anodic zirconium-oxide nanorods recorded after dissolving the PAA layer from an anodic film prepared by 40 V anodizing and 240 V re-anodizing, as outlined in the inserted schematic. (c) Experimental (red circles), calculated (black lines), and difference (grey lines) X-ray diffractograms of the same sample analyzed before the dissolution of the PAA layer, as outlined in the inserted schematic. The arrows relate the observed Debye rings of the 2D diffractogram (inserted image) with the corresponding peaks of the conventional diffractogram.

microstructure of metallic α -Zr was estimated from peak broadening by considering only the influence of the crystallite size with a value of 12.7 ± 0.4 nm. The crystallite sizes for the monoclinic ZrO_2 and orthorhombic ZrO_2 were estimated to be 9 ± 1 and 19 ± 2 nm, respectively. The alumina matrix appeared to be fully amorphous since no crystal phases of Al_2O_3 were revealed by XRD (at the available detection limit).

Conclusively, while the α -Zr phase is associated with a layer of initially sputter-deposited zirconium metal that remains unoxidized, the two ZrO_2 phases grow due to the anodic oxidation. Comparing the sizes of the ZrO_2 nanocrystallites with the film morphology and architecture features, we assume that the monoclinic and orthorhombic ZrO_2 nanocrystallites reside in the compact sublayer of the lower film layer, which buffers the sponge-like sublayer from the bottom metallic electrode (Figures 1(e') and 2(h)). The PAA-inbuilt nanorods comprise the stoichiometric (dominating amount) and substoichiometric (having oxygen vacancies) amorphous ZrO_2 .

3.3. Device performance at room temperature

3.3.1. Impedance analysis

By raising the re-anodizing voltage from 80 to 320 V in 40 V steps, seven options of the anodic-oxide dielectrics having similar surface morphologies and progressively increasing thicknesses were synthesized from the same Al/Zr bilayer precursor. Critical factors that characterize the performance of MIM devices are the capacitance density, dielectric loss, breakdown field strength, and leakage current density in relation to dielectric thickness, applied voltage, frequency, and operating temperature [54]. The impact of the film thickness on the electrical behavior of the MIM devices is demonstrated in Figure 4. The Bode plots recorded in a 10^2 – 10^6 Hz frequency range at room temperature are shown in Figure 4(a). The impedance modulus linearly decreases with a slope of -1 with frequency increasing, indicating the capacitive behavior of the anodic oxide. Further, the impedance value increases with dielectric thickness. The phase shift for all films is almost frequency independent, closely approaching -90° , which indicates a nearly ideal dielectric behavior of all the films.

3.3.2. Capacitance – losses – thickness relationship

The capacitance density of the MIM devices, C , and the relative permittivity, ϵ_r , of the anodic-oxide films in relation to film thickness, h , are shown in Figure 4(b). First, C declines with increasing h . Specifically, the thinnest ($h = 95$ nm) dielectric results in the highest C (112 nF·cm $^{-2}$), while the thickest anodic film ($h = 480$ nm) gives the lowest C (21 nF·cm $^{-2}$). The apparent relative permittivity of

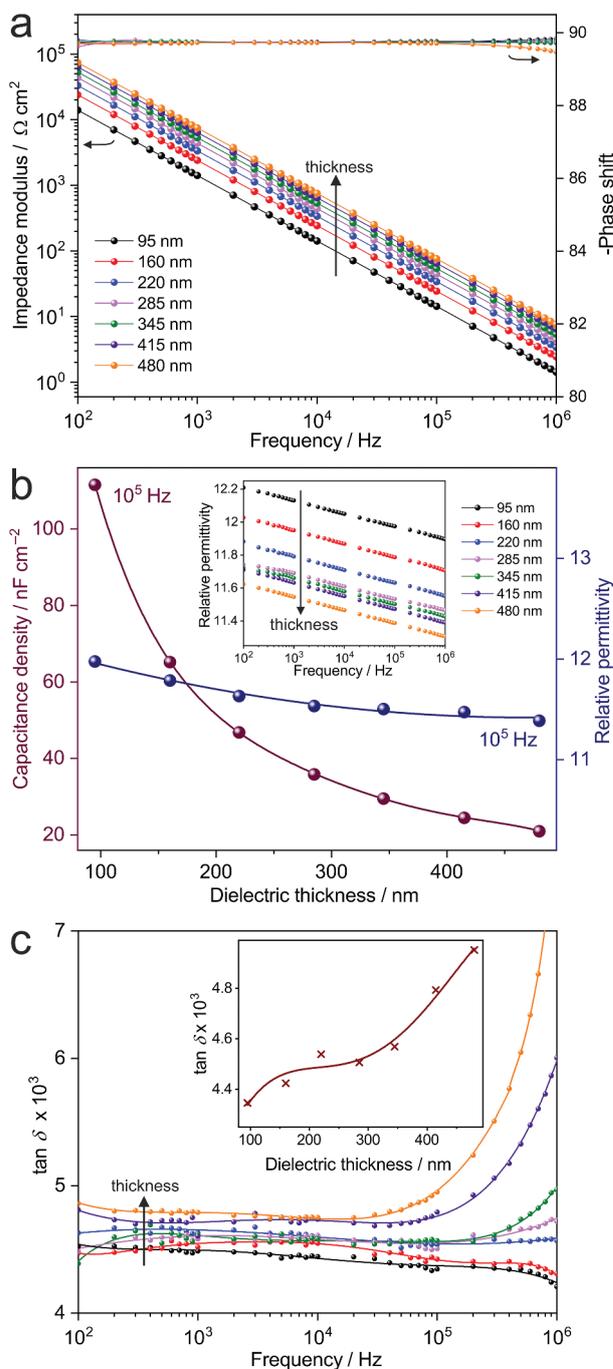


Figure 4. (a) Room-temperature characterization of MIM devices based on the planar nanocomposite dielectrics of various thicknesses: (a) Bode plots – modulus of impedance and phase shift vs. frequency, (b) variation in capacitance density and relative permittivity with dielectric thickness at 10^5 Hz (the inset shows the relative permittivity vs. frequency), and (c) variation of $\tan \delta$ with frequency (the inset shows $\tan \delta$ vs. dielectric thickness at 10^5 Hz).

the anodic-oxide dielectrics can be calculated as $\epsilon_r = hC/\epsilon_0$, where ϵ_0 is the vacuum permittivity. When measuring at 10^5 Hz, the apparent ϵ_r gradually declines from 12.0 ($h = 95$ nm) with increasing h and then stabilizes around 11.5 ($h \geq 285$ nm). The average ϵ_r -value of the anodic films prepared in this study is ~ 11.5 , which differs from the known values for Al_2O_3 ($\epsilon_r = 9.0$) and ZrO_2 ($\epsilon_r = 22.0$) [55].

This difference arises due to the complex film composition and its layered architecture. It is assumed that the present films do not exhibit distinct electrical interfaces and can be viewed as a single dielectric [27]. The PAA matrix and ZrO₂ nanorods are electrically connected in parallel, both being connected to the lower layer in series. Therefore, the apparent ϵ_r is a combination of ϵ_r of the individual film components. The lack of zirconia stoichiometry and the oxygen-filled cavities ($\epsilon_r = 1.0$) decrease ϵ_r of the lower ZrO_x layer. In the upper layer, the ZrO₂ nanorods occupy only ~17 vol.% of the layer volume, while the rest is Al₂O₃. Additionally, the ZrO₂ nanorods contain oxygen-filled voids ($\epsilon_r = 1.0$) within their bases [27]. All these factors limit the impact of ZrO₂ on the apparent ϵ_r and emphasize the role of the alumina matrix.

The apparent ϵ_r of the planar anodic films (11.5) appears slightly higher than that of the ZrO₂-Al₂O₃ dielectrics deeply incorporated in the PAA layer (11.0) [27]. The increase may be due to the PAA-dissolution-induced disproportionality between the thickness of the upper Al₂O₃-ZrO₂ layer, h_{up} , and the thickness of the lower ZrO_x layer, h_{low} . The effective dielectric thickness is $h = h_{up} + h_{low}$ (Figure 1(e)). As previously reported, during the PAA-assisted re-anodizing of the Al/Zr bilayer in 0.6 M H₂C₂O₄ solution, both layers thicken simultaneously and proportionally to re-anodizing voltage with a constant h_{up}/h_{low} ratio of 2.5 [27]. This feature results in a constant ϵ_r -value of ~11.0 for the anodic films regardless of re-anodizing voltage and h [27]. However, the pore-dissolution procedure employed to planarize the anodic films makes the upper Al₂O₃-ZrO₂ medium- ϵ_r layer thinner by ~40 nm equally for all the films, irrespective of their h . This alters the relative contributions of the upper and lower film layers to the apparent ϵ_r . The pore-dissolution procedure reduces h_{up} and, consequently, decreases the contribution of the upper Al₂O₃-ZrO₂ medium- ϵ_r layer to the apparent ϵ_r . At the same time, as h_{low} is not affected by the pore dissolution, the relative contribution of the high- ϵ_r ZrO_x lower layer to the apparent ϵ_r increases. This effect makes the apparent ϵ_r of the planarized films designed for MIM capacitors higher than ϵ_r of the as-formed anodic films intended for electrolytic capacitors [27]. The pore-dissolution procedure affects the apparent ϵ_r of the thinner films ($h \leq 285$ nm) disproportionately stronger as they have relatively thinner Al₂O₃-ZrO₂ upper layers. The apparent ϵ_r of the thicker films ($h \geq 285$ nm) is less affected because of the thicker Al₂O₃-ZrO₂ upper layers. Therefore, ϵ_r almost stops decreasing with the thickening of the films over 285 nm and stabilizes around 11.5. Schematic diagrams depicting the impact of the pore-dissolution procedure on ϵ_r , a graph showing the variability of h_{up}/h_{low} ratio with film thickness, and fitting of the apparent ϵ_r with

a model function are presented in the Supplementary Information (SI) file.

The inset in Figure 4(b) shows that ϵ_r decreases with frequency, f , regardless of h . Such behavior is typical for dielectrics and is attributed to a lag of interfacial dipole orientation in the direction of an alternating electric field as f increases [56]. Figure 4(c) shows loss tangent, $\tan \delta$, as a function of f . In the 10²-10⁵ Hz range, $\tan \delta$ is small and almost f -independent, slightly increasing from 4.3·10⁻³ to 4.8·10⁻³ with increasing h . However, above 10⁵ Hz, the behavior becomes more thickness-affected. For the 95 and 160 nm-thick dielectrics, $\tan \delta$ slightly declines in the 10⁵-10⁶ Hz range. The 220 nm-thick dielectric exhibits stable behavior up to 10⁶ Hz. The loss tangent gradually increases beyond 10⁵ Hz in the 285 and 345 nm-thick dielectrics, with the tendency to exaggerate in the thickest 415 and 480 nm dielectrics.

The inset in Figure 4c presents the behavior of $\tan \delta$ with respect to h measured at 10⁵ Hz. A minor rise of $\tan \delta$ is noted as h increases from 95 to 220 nm, followed by a period of stability up to 345 nm and finishing with a second rise of $\tan \delta$ for the thickest films. The losses may be caused by chemical composition, impurities, physical imperfections, or crystallite grain boundaries in the dielectric [56]. Since the upper film layers are amorphous Al₂O₃ and ZrO₂, the loss tangent may rise due to crystallographic imperfections in the lower crystalline zirconium-oxide layer. The thickening of the lower layer with re-anodizing voltage most likely results in the formation of relatively bigger ZrO₂ nanocrystallites. This feature can potentially result in an increased energy dissipation over the grain boundaries alongside a rise in dielectric losses at higher frequencies as the films thicken. However, the low- and middle-frequency losses achieved for the planar Al₂O₃-ZrO₂ nanocomposite dielectrics appear to be almost two orders of magnitude lower than in the Al₂O₃-ZrO₂ mixed-oxide layers prepared by other methods [57]. Moreover, the losses achieved here are one to two orders of magnitude lower than in one-component Al₂O₃ and ZrO₂ films deposited by ALD [58,59].

3.3.3. Voltage linearity, DC stability, and energy density

Capacitance change by applied DC voltage (voltage linearity) is one of the vital capacitor characteristics. The voltage linearity is most often characterized by the quadratic voltage coefficient of capacitance (VCC), α , derived from the C - V curves [60] as $\Delta C/C_0 = \alpha V^2 + \beta V$, where C_0 is the zero-bias capacitance, $\Delta C = C(V) - C_0$ is the increase in the capacitance with applied voltage V , and β is the linear VCC. Figure 5(a) depicts the change in C , $\Delta C/C_0$, with V at 10⁵ Hz in relation to h . C as a function of V at 10⁵ Hz is shown in the inset of Figure 5(a). The observed growth

of C with the bias voltage is typical for high- ϵ_r metal oxides [61] and follows a quadratic function. With increasing h , the fitting curves flatten, indicating the lowering of α from 62 to less than 5 ppm·V⁻². The decrease in α with increasing h correlates well with previous reports, where α was almost inversely proportional to the capacitor dielectric thickness [62]. As h increases, electric field across the film decreases, resulting in lower α . The low value of α may be explained by the charge accumulation at the interfaces between the dielectric anodic film and the conducting electrodes [63]. Notably, the MIM devices fabricated in the present work exhibit a lower α than the capacitors based on ALD-deposited Al₂O₃ films of similar thickness [58].

Figure 5(b) shows changes in the leakage current density, J , measured at a 5 V bias voltage and the breakdown field strength, E_b , with increasing h . The highest 560 pA·cm⁻² J is measured through the thinnest 95 nm dielectric. The leakage current decreases to 40 pA·cm⁻² as h increases to 480 nm. Such low leakage-current densities may be explained by the

nanostructured composition of the composite films and the layered film architecture. This suggestion is backed by other studies where the fabrication of Al₂O₃-ZrO₂ nanolaminates or mixtures was noted as a practical approach for lowering leakage current in the dielectric [64,65].

The E_b rises sharply with increasing h up to 285 nm (Figure 5(b)). Then the increase rate retards until E_b attains a relatively stable value of about 10 MV cm⁻¹ for $h \geq 345$ nm. The increase in E_b with increasing h may be explained by a more pronounced impact of the pore dissolution during the planarization procedure on the upper layer of thinner films, as described in the SI file. The lowest 4.0 MV cm⁻¹ E_b is attributed to the thinnest 95 nm dielectric with the highest ZrO_x lower-layer contribution to film composition. This E_b -value is close to those reported for pure ZrO₂ (2–6 MV cm⁻¹) [66]. With increasing h , the impact of the planarization procedure on the Al₂O₃-ZrO₂ upper-layer thickness becomes less pronounced. The higher h decreases the contribution of the ZrO_x lower layer and increases the contribution of the Al₂O₃-ZrO₂ upper layer to the film composition. Due to this feature, ϵ_r decreases slightly, but E_b increases noticeably. The high thickness of Al₂O₃-rich Al₂O₃-ZrO₂ upper layer seems to be a key to achieving the high E_b as the 10 MV cm⁻¹ value is a theoretical maximum for Al₂O₃ [67]. The E_b value achieved in the present work surpasses the values reported for Al₂O₃-ZrO₂ mixed oxides synthesized via other methods [57,68]. Moreover, E_b of the Al₂O₃-ZrO₂ mixed-oxide films prepared via the PAA-assisted anodizing exceeds the values for one-component Al₂O₃ films (4–7 MV cm⁻¹) prepared by ALD and ZrO₂ films (2–4 MV cm⁻¹) prepared by ALD or sol-gel deposition [69–73]. The ability of the Al₂O₃-ZrO₂ nanocomposite dielectrics synthesized here to withstand the field of up to 10 MV·cm⁻¹ while having a higher permittivity ($\epsilon_r = 11.5$) relative to pure Al₂O₃ ($\epsilon_r = 9.0$) is a tremendous improvement of the essential capacitor characteristic.

The relatively high ϵ_r and E_b values revealed in the anodic Al₂O₃-ZrO₂ composite dielectrics can be potent for energy-storage capacitor applications since the device's maximum energy density, U , is proportional to ϵ_r and E_b per equation $U = \epsilon_r \epsilon_0 E_b^2 / 2$. An inset of Figure 5(b) shows how U changes with h . Initially, U rapidly rises but stabilizes at about 100 J·cm⁻³ for $h \geq 345$ nm. U grows mainly due to the rise of E_b with increasing h since ϵ_r slightly declines for films with high h . The technology developed in this study is advantageous for forming dielectric films with highly competitive energy density. The U value achieved here surpasses the energy density of Al₂O₃-ZrO₂ mixtures or nanolaminates (~10–40 J cm⁻³), pure Al₂O₃ (~5–20 J cm⁻³), and pure ZrO₂ (~20 J cm⁻³) reported elsewhere [57,68,74,75].

The summary of all relevant MIM capacitor characteristics measured at 10⁵ Hz frequency and room temperature is presented in Table 1.

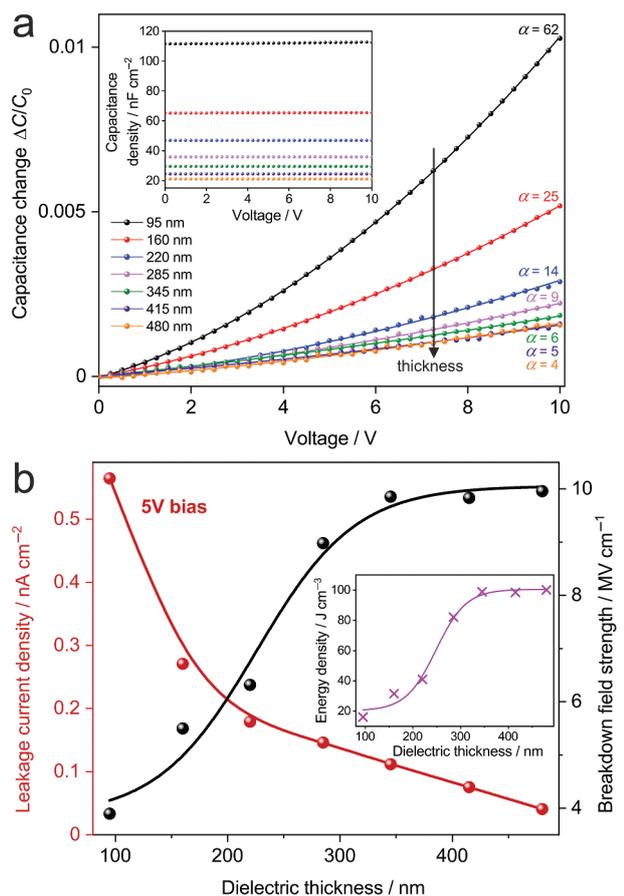


Figure 5. Room-temperature-measured (a) relative change in capacitance density under DC bias voltage for MIM devices utilizing the nanocomposite dielectrics of various thicknesses (inset: capacitance density vs. DC bias voltage in relation to dielectric thickness) and (b) leakage current density and breakdown field strength vs. dielectric thickness (inset: capacitor energy density vs. dielectric thickness). The measurements were performed at 10⁵ Hz.

Table 1. Characteristics of MIM capacitors utilizing the planar Al₂O₃-ZrO₂ nanocomposite dielectrics, measured at 10⁵ Hz and room temperature.

Re-anodizing voltage, V	Dielectric thickness, nm	Capacitance density, nF·cm ⁻²	ϵ_r	$\tan \delta \times 10^3$	Leakage current, nA·cm ⁻²	Breakdown voltage, V	Breakdown field strength, MV·cm ⁻¹	Quadratic VCC (a), ppm·V ⁻²	Energy density, J·cm ⁻³
80	95	112	12.0	4.3	0.56	40	4	62	16
120	160	65	11.8	4.4	0.27	90	5	25	32
160	220	47	11.6	4.5	0.18	140	6	14	41
200	285	36	11.5	4.5	0.15	260	9	9	82
240	345	30	11.5	4.6	0.11	340	10	6	99
280	415	24	11.5	4.8	0.08	410	10	5	98
320	480	21	11.4	4.9	0.04	480	10	4	100

3.4. MIM device performance at elevated temperatures

3.4.1. Conduction mechanism

If not stated otherwise, all experiments described in the following sections were conducted with an array of on-chip MIM devices utilizing a 345 nm-thick planar anodic-oxide dielectric. This thickness was chosen based on the graphs in Figures 4 and 5 and the data summarized in Table 1. The moderate C-value and stable static characteristics provided by such a dielectric were thought to be a logical choice for performing dynamic measurements with varied bias voltage, frequency, and operating temperature.

Figure 6(a) shows the dependency of *J* on the applied electric field, *E*, and the *I*-*V* curve in the inset. Under relatively weak *E*, up to about 2.0 MV cm⁻¹, *J* remains very low and is practically independent of *E*. Such behavior conforms with Ohm's law, meaning that bulk-limited conduction is a dominant contribution to the leakage current [76], which is of great practical importance. The *J*-*E* dependence exhibits a knee at a higher field, beyond which *J* increases notably (from 2.0 to 2.7 MV cm⁻¹). This behavior indicates the initiation of space-charge-limited currents or/and the beginning of a transition to injection-limited conduction [76]. The *I*-*V* curve recorded in the range of -25 to 25V demonstrates low currents in the device, well

below 1 nA·cm⁻² even at -25/25 V. A minor asymmetry under the negative and positive polarization likely reflects the differences between the upper (Al/Al₂O₃-ZrO₂) and bottom (Zr/ZrO_x) electrical interfaces [77]. The Al₂O₃-ZrO₂ anodic-oxide capacitor assembled in this work revealed a 2 nA cm⁻² *J* at 2.0 MV·cm⁻¹, which is lower than leakage currents reported in single-component MIM devices based on ALD-deposited Al₂O₃ (~100 nA·cm⁻²) and ZrO₂ (~1 μA·cm⁻²) layers measured at a similar field [78,79]. Further, the leakage current in our capacitor is lower than in capacitors based on sol-gel deposited Al₂O₃-ZrO₂ nanocomposites (~1 μA·cm⁻² at 2.0 MV·cm⁻¹) [57].

Figure 6(b) shows the impact of temperature, *T*, on *J* at 5 V bias voltage. Three distinct regions are noted. *J* increases slowly from 0.1 to 0.2 nA·cm⁻² in the low-*T* region (293–363 K). Then, *J* increases more rapidly, up to 2.4 nA·cm⁻² in the mid-*T* region (363–433 K), followed by a relatively faster rise up to 640 nA·cm⁻² in the high-*T* region (433–523 K). The low values of leakage currents at temperatures up to 423 K are highly competitive in the niche of high-temperature capacitors [80].

For a better understanding of the DC conduction mechanism in the mixed-anodic-oxide dielectrics, the logarithm of the conductivity is plotted against reciprocal temperature in Figure 6(c). Three conductivity

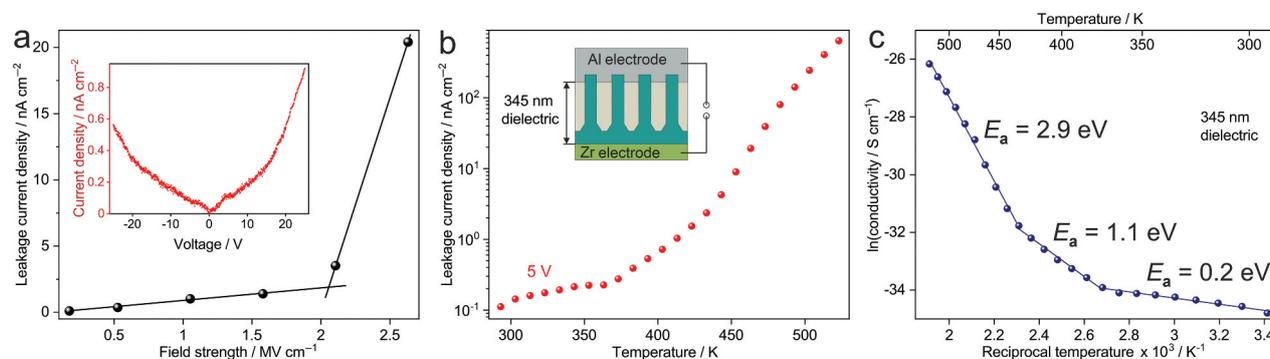


Figure 6. Leakage current density (a) as a function of applied electric field strength at room temperature and (b) vs. operating temperature in a MIM device utilizing a 345 nm-thick Al₂O₃-ZrO₂ planar anodic-oxide dielectric (hereafter the 'MIM-345 device') measured at 5 V DC bias voltage. The inset in (a) shows the *I*-*V* characteristic under positive and negative polarization up to 25 V. (c) Natural logarithm of DC conductivity measured at 5 V vs. temperature and reciprocal temperature (the Arrhenius plot) of the MIM-345 device in a temperature range of 298–523 K.

regions are distinguished and fitted with a linear function that follows the Arrhenius equation. The activation energy, E_a , of each region can be derived from the equation $E_a = -2.3k(\Delta \ln \sigma / \Delta(1/T))$, where σ is the conductivity and k is the Boltzmann constant. The following E_a values are calculated from the Arrhenius plot: 0.2 eV for the low- T region, 1.1 eV for the mid- T region, and 2.9 eV for the high- T region. As follows from Figure 6(a), the electron conductance in the Al_2O_3 - ZrO_2 anodic-oxide dielectrics can be neglected at a field of $0.17 \text{ MV}\cdot\text{cm}^{-1}$. Therefore, the increase in σ with increasing T can be explained by lowering the potential energy of traps and increasing the ion mobility in the oxide [81]. A low 0.2 eV E_a in the low- T region may be explained by the current governed by the impurities and singly-ionized oxygen vacancies in the anodic zirconium oxide [82]. In the mid- T region, σ increases noticeably faster, and a higher 1.1 eV E_a may be related to the conductance through doubly-ionized oxygen vacancies [82]. Singly and doubly ionized oxygen vacancies are readily associated with the substoichiometry of the anodic zirconium oxide, as revealed by the XPS analysis (Figure 3(a,b)). In the high- T region, characterized by the fastest increase in σ , a 2.9 eV E_a can be related to an intrinsic conductivity in the anodic-oxide dielectric as the value fits theoretical activation energies for amorphous ZrO_2 [83].

3.4.2. Frequency-dependent characteristics

The graphs in Figure 7 demonstrate the influence of operating temperature on the frequency-dependent characteristics. Figure 7(a) shows the Bode diagrams recorded over an extended f range of 10^{-2} – 10^6 Hz at T ranging from 298 to 523 K. The f -dependent behavior of impedance modulus and phase shift confirms that the device performs as an ideal capacitor and retains its dielectric properties at elevated temperatures. The impedance lines systematically shift toward lower values with raising T , meaning an increase in device's capacitance is likely related to the T -induced change in ϵ_r . The low- f operating range progressively narrows with growing T , as one may expect due to increasing temperature-induced conductance [76,81].

The C - f curves at various temperatures are shown in Figure 7(b). It is first noted that C rises with increasing T . In the 298–348 K range, C weakly and monotonically decreases with f . In the 373–398 K range, a weak low- f capacitance dispersion occurs but weakens as f increases. The capacitance dispersion becomes more pronounced in the low- and middle- f ranges starting from 423 K and shifts toward higher f with further heating. Such behavior can potentially be associated with the thermal activation of charge carriers responsible for the net increase of dipoles at the metal/oxide interfaces. However, with increasing frequency, the capacitance stabilizes as the contribution of thermally activated charge carriers weakens, and the charge buildup at the electrode/film inferences does not occur [84].

The temperature-affected behavior of the $\tan \delta$ - f curves is shown in Figure 7(c). The losses systematically increase with heating. The curves attain a more parabolic shape when T is raised to 398 K. A broad peak appears on the $\tan \delta$ - f curve in the low- f range at 398 K. The peak slightly grows and systematically moves toward higher f with further heating. The T -induced broad peaks on the $\tan \delta$ - f curves arise due to the relaxation effects in the dielectric polarization of the anodic-oxide films. However, due to the long relaxation times, the polarization is substantially slower than the field reversals, and relaxation maximums do not appear yet at temperatures below 398 K. The absence of relaxation peaks in the whole frequency range at temperatures up to 373 K is of immense practical importance.

Figure 8(a) shows how $\tan \delta$ changes with T at several fixed f . The relaxation peaks shift to higher temperatures, and their intensities rise with frequency. The behavior confirms that the relaxation process is T -dependent. The relaxation effects are commonly enhanced in dielectrics when the hopping frequency of charge carriers matches the frequency of the electric field. The temperatures at which the peaks manifest (≥ 398 K) assume the accumulation of thermally activated delocalized charge carriers at the electrode/oxide

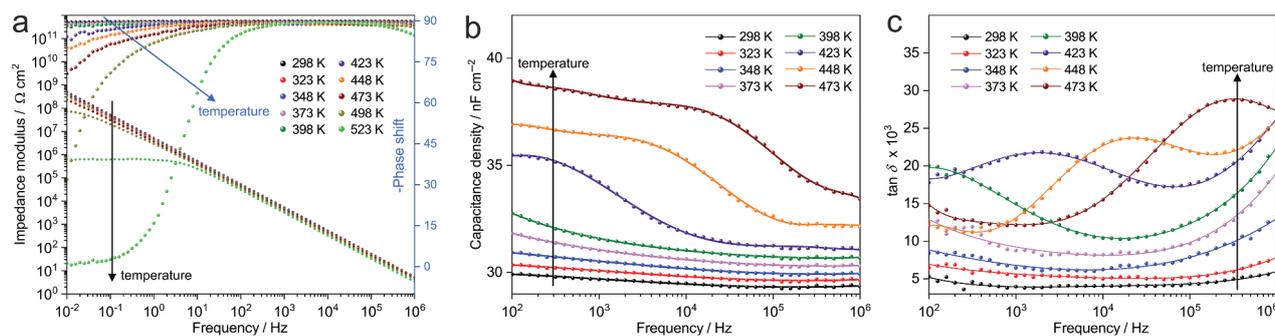


Figure 7. Frequency dependencies in relation to operating temperatures of (a) modulus of impedance and phase shift (Bode diagrams), (b) capacitance density, and (c) loss tangent. The measurements were performed with the MIM-345 device.

interfaces. The T -induced shift of the peaks with rising temperature may be associated with the increased hopping frequency of thermally activated charge carriers [85].

Figure 8(b) shows C - T curves recorded at several characteristic f . The temperature coefficient of capacitance (TCC) can be calculated per equation $TCC = \Delta C / (C_i \Delta T)$, where C_i is the initial capacitance density at 298 K, ΔT is the temperature change, and ΔC is the change in capacitance density over the temperature range. Each graph can be divided into two parts: a slow linear C rise in the low- T region (low-TCC) and a substantially faster C rise at higher temperatures (high-TCC). At frequencies above 10^3 Hz, the low-TCC region propagates further and extends up to 423 K. The slopes of the lines in the low-TCC regions become systematically smaller with rising f , meaning a drop in TCC from 960 ppm·K⁻¹ at 10^2 Hz to 480 ppm·K⁻¹ at 10^6 Hz. The substantial reduction in TCC and the extension of the low-TCC region up to 423 K with increasing f is an asset for the particular application of the capacitors in high-

frequency circuits operating at harsh temperature conditions.

3.5. Relevance and application perspectives

The electrochemistry-based technology for the planar dielectrics developed here enables the highly competitive characteristics in the niche of ceramic (metal-oxide) thin-film capacitors. This makes the results attractive for potential multipurpose applications. The capacitance density can be pre-selected from 112 to 21 nF·cm⁻² by choosing the dielectric thickness from 95 to 480 nm. The loss tangent remains low (0.004–0.005) for the 95–345 nm-thick dielectrics at frequencies up to 10^6 Hz and temperatures up to 373 K. The leakage-current density lowers from 600 to 40 pA·cm⁻², the breakdown field further improves from 4.0 to 10 MV·cm⁻¹ (breakdown voltage rises respectively from 40 to 480 V), the maximum energy density attains 100 J·cm⁻³, and the quadratic VCC decreases from 62 to 4 ppm·V⁻² with thickening the dielectric from 95 to 480 nm. The TCC lowers from ~635 to 480 ppm·K⁻¹ with increasing frequency from 10^3 to 10^6 Hz at temperatures up to 423 K. A graph showing the interrelation between the thicknesses of the anodic-oxide dielectrics, the re-anodizing voltages to form the dielectrics, and the relative changes of major capacitor characteristics is presented in Figure 9(a) and complemented by a bar-chart presentation in the SI file. The low-value equivalent series resistance (ESR) of 0.6 Ohm is estimated at 10^6 Hz and 293 K for a practical 1 nF MIM microcapacitor fabricated in this work. This value is comparable to the ESR of commercial ceramic 1 nF capacitors based on X7R dielectrics measured at the same frequency and temperature [86]. The electrical and thermal stabilities of our capacitors are relatively superior, up to about 398 K. Further details about the ESR estimation are available in the SI file.

Regarding earlier attempts to employ the PAA films with open pores as a capacitor dielectric [24], it is obvious that the non-porous planar Al₂O₃-ZrO₂ nanostructured composites developed in the present work substantially improve major capacitor characteristics such as capacitance density, energy density, leakage currents, and voltage sustainability, also minimizing the capacitance dispersion and energy dissipation at frequencies up to the 10^6 Hz and temperatures up to 398 K due to the long relaxation times for dielectric polarization and lessening the charge buildup at the electrode/film interfaces [24].

From the viewpoint of achieved characteristics, the application areas for the capacitors described here include EMI/EDS filters, coupling/decoupling/bypass circuits, low-pass filters, RC oscillators, energy storage, ultrafast charge/discharge devices, or high-precision analog-to-digital and digital-to-analog converters, especially when improved thermal stability is

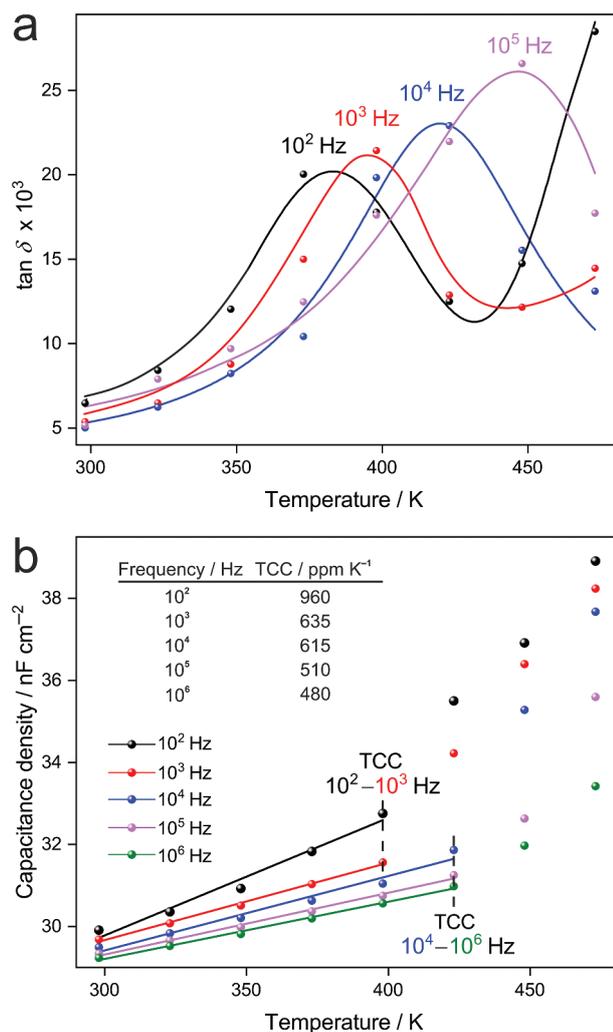


Figure 8. (a) Loss tangent and (b) capacitance density as a function of operating temperature at various fixed frequencies measured for the MIM-345 device.

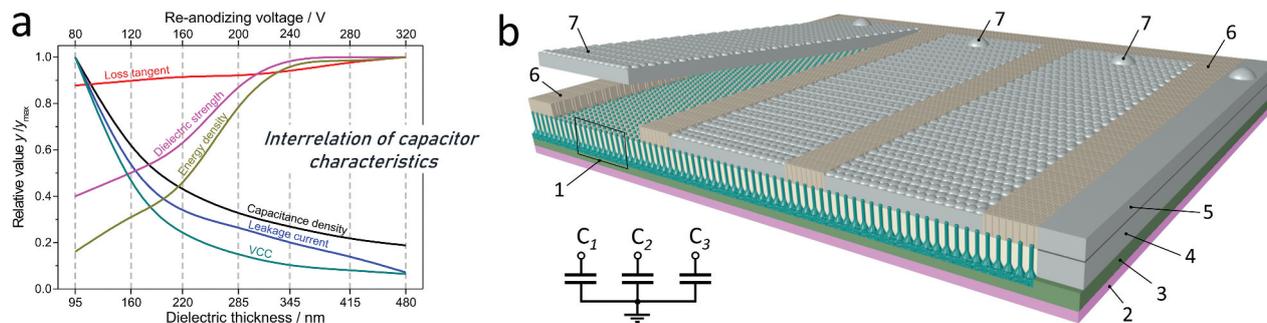


Figure 9. (a) Interrelation between the thicknesses of the planar composite dielectrics, the re-anodizing voltages to form the dielectrics, and the relative changes of major capacitor characteristics. (b) Computer-aided 3D model of an array of MIM capacitors based on the sputter-deposition, selective anodizing, and planarization technologies: (1) the planar nanostructured $Al_2O_3-ZrO_2$ composite dielectric; (2) a substrate; (3) the bottom capacitor plate (Zr); (4, 5) the electrical contact to the bottom plate (Al); (6) a low- k PAA dielectric planarizing the top capacitor plates; (7) the top capacitor plates (Al).

required. Detailed consideration of the suitability of the $Al_2O_3-ZrO_2$ -based MIM capacitors for particular electronic devices is available in the SI file.

From the technological viewpoint, to demonstrate the potential of the fabrication and assembly techniques for passive device integration, an array of planar thin-film MIM capacitors was designed based on combining selective anodizing with standard microfabrication technologies. Figure 9(b) shows a 3D view of the computer-aided package comprising three micro-devices sharing the bottom electrode and having separated top electrodes. The design is reasonably simplified to provide a general understanding of the packaging approach. The capacitor dielectric (1) is made via the anodizing/re-anodizing of an Al/Zr bilayer sputter-deposited on a substrate (2), followed by the partial PAA dissolution to planarize the film surface as outlined in detail in Figure 1(a–e). A portion of the Zr layer that remains unoxidized (3) serves as the bottom capacitor plate, common for all devices in the assembly. An array of top capacitor electrodes (7) is made by the sputter-deposition of Al over the planar anodic film, followed by its selective anodizing. Such anodizing is to be carried out in an acid electrolyte that transforms the Al film into a low- k PAA layer (6), having relatively smaller pores to minimize parasitic capacitances between the electrodes and avoid difficulties in making further layers over this package if necessary. A low- k PAA layer serves simultaneously as the electrode-separating and planarizing dielectric for the top level of capacitor assembly. The stacked Al strips (4 and 5) are made during the selective anodizing for the 1st and 2nd layers and provide an electrical connection to the bottom electrode.

The electrochemistry-based technology for integrated capacitors may potentially be combined with the processes for the anodic formation of planar thin-film aluminum interconnection, nanostructured micro-resistors, thermistors, and micro-inductors [17,19,20,23]. Therefore, further progress with the fabrication and assembly techniques developed in

our work is associated with moving toward a universal technology for the whole range of electronic passives co-integrated within the same package on a chip module or stacked in multilayers on a microelectronic substrate. This will be the subject of future works.

4. Conclusion

An electrochemistry-based technology was developed for forming the non-porous nanostructured anodic-oxide composite films of tunable thicknesses and planar surfaces from an Al/Zr bilayer sputter-deposited on a substrate. The films were utilized as novel dielectrics for MIM microcapacitors. From the performance viewpoint, the devices revealed outstanding electrical/dielectric characteristics that may be tuned on demand by simply adjusting the dielectric thickness to meet the requirements for particular applications. The best-achieved capacitor characteristics are the one-layer capacitance density of $112 \text{ nF}\cdot\text{cm}^{-2}$ (which can potentially be doubled in a two-layer architecture), the low loss tangent of $4\cdot 10^{-3}$ at frequencies up to 10^6 Hz and temperatures up to 373 K, the low leakage current density of $40 \text{ pA}\cdot\text{cm}^{-2}$, the excellent breakdown field strength of $10 \text{ MV}\cdot\text{cm}^{-1}$, the extraordinary small quadratic VCC of $4 \text{ ppm}\cdot\text{V}^{-2}$, the low TCC of $480 \text{ ppm}\cdot\text{K}^{-1}$ at 293–423 K, and the high energy density of $100 \text{ J}\cdot\text{cm}^{-3}$. Due to the voltage, frequency, and temperature stabilities, the capacitors meet the requirements for multipurpose applications. The extremely low RC time constants make the capacitors the logical choice for most high-speed circuits. Being inherently more stable at high frequencies than the electrolytic capacitors, the electrostatic capacitors fabricated here may notably improve the performance and reliability of the output filter sections.

From the technological viewpoint, the approach for fabricating on-chip MIM microcapacitors utilizing the planar $Al_2O_3-ZrO_2$ nanocomposite dielectrics complements the emerging anodizing conception of IPDs

all correlated in one system and may inspire their application in future PEDs.

Disclosure statement

No potential conflict of interest was reported by the authors.

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