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Hardware Article

BIMMS: A versatile and portable system for biological tissue and electrode-tissue interface electrical characterization

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ABSTRACT

The presented design is a low-cost, compact, and open-source USB-controlled platform for biological tissue and electrode-tissue interface electrical measurements, capable of potentiostatic and galvanostatic electrical impedance spectroscopy up to 10 MHz and cyclic voltammetry with voltage compliance of +−8 V and up to 2.4 mA while ensuring tissue-safety conditions. The data acquisition and generation are based on an Analog Discovery 2 platform (Digilent, USA). We provide accuracy analysis and comparisons with a commercially available calibrated impedance analyzer. Impedance measurements are demonstrated on implanted electrodes for neural stimulation and on an isolated ex-vivo calf brain as an example use case of the presented design.

Specifications table

Hardware name	*BIMMS: Bio-Impedance Measurement System*
Subject area	Bio-engineering
Hardware type	Electrical engineering and computer science
Open Source License	*CC BY 4.0*
Cost of Hardware	*$650 ($530 with academic pricing on the Analog Discovery 2 platform).*
Source File Repository	https://doi.org/10.5281/zenodo.7148811

Hardware in context

The miniaturization capabilities of electronic components have enabled to produce complex healthcare implanted systems (neurostimulators such as deep brain stimulators [1] or for rehabilitation purposes [2], cardiac pacemakers [3] for instance) compatible with implantation closer to the target organ. However, although the microelectronic integration tech-

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niques allow to consider the production of ever smaller, energy-efficient, and reliable systems for therapeutic or diagnostic applications, the need for accurate characterization of the electrode-tissue interface and tissue electrical characteristics appears to be crucial for both designing [4] and post-implantation performances [5–7] or characterize tissue safety [8].

Tissue properties are usually monitored using Electrode Impedance Spectroscopy (EIS) over a given bandwidth, and for a specified set of discrete frequencies [9]. A voltage or current is applied to the sample under test (SUT) and impedance is sensed using simple techniques such as the I/V method (Fig. 1(a)) for low frequencies (up to 100 MHz) and network analysis or RF I/V methods are the most appropriate methods for higher frequencies [10]. Various waveshapes have been used such as the conventional swept-sine, chirps [11], multisine [12], and more complex waveforms [13]. Choosing the adequate broadband signal depends on the application and the optimal choice will differ according to the criterion chosen: accuracy, configurability, measurement speed, design complexity, etc. For example, a multisine-waveform offers accurate results while being highly configurable [14], however generating such a waveform is not a trivial task for low-power small-size systems such as implantable devices. In such applications, multisine-waveform can be swapped with much simpler broadband binary or ternary sequences at the cost of a slight decrease in accuracy and signal-to-noise ratio [15].

EIS can be performed using 2 or 4 points configurations (Fig. 2). In the 4-points configuration, also referred to as tetrapolar configuration, the stimulus injection and the voltage readout are split in two ways. By using high input impedance voltage readout circuit, the current flowing through the sensing electrode is negligible, resulting in a close to zero voltage drop across it. Thus, only the impedance of the SUT is being measured [16]. The 2-point configuration is suitable when information on the electrode-tissue interface is needed [17]. When only the tissue's electrical properties are considered, a tetrapolar configuration is required [18].

Electrode-tissue interface properties and more specifically non-linearities are measured using electrochemical methods such as Cyclic Voltammetry (CV) [19]. In CV, the voltage potential at an electrode is ramped linearly versus time, and the resulting current is measured. These techniques rely mostly on 3 points configurations, with working- counter- and reference-electrodes. (Fig. 3). A potentiostat feedback circuit is used to maintain the potential of a working electrode (WE) equal to the potential of a reference electrode (RE) while forcing the current going from the working electrode to the counter electrode (CE). This electrode configuration allows to maintain RE at known pseudo-equilibrium during measurements and not being influenced by any current passing through. Measurement circuits are limited to low-frequency domains and are well-identified [20].

For both EIS and CV, the voltage potential at the SUT is measured, as well as the current via a sense resistor. In the auto-balancing configuration (Fig. 1(b)), the sense resistor is replaced with a trans-Impedance Amplifier (TIA). The TIA connects the SUT to a virtual ground, greatly reducing the parasitic of the feedback resistor. The auto-balancing configuration extends the measurement bandwidth above 10 MHz. In EIS measurement, the excitation source can either be a controlled voltage source or a controlled current source. Those two methods are respectively referred to as potentiostatic EIS and galvanostatic EIS. A voltage source has the advantage of being simpler to design and usually offers better performance at higher frequencies. However, for EIS on bio-sample, a controlled current source remains popular for its ability to ensure that the injected current is lower than the medical safety limits [21]. The injected current with a voltage source is determined by the interface impedance between the electrode and the SUT. This impedance can vary over time or with electrode displacement, thus it is difficult to accurately predict injected current. Current sources also provide additional insurance to maintain the amount of injected charges in the SUT balanced. The current-voltage relationship in bio-electronic interfaces tends to have a non-linear behavior [22], thus ensuring charge-balancing with a voltage source is problematic. However, designing a current source is challenging. High-frequency performances are mostly limited by its output impedance, degraded by stray capacitance. Various topologies of current source exist, such as the Howland pump and its improved version [23] or the current conveyor topology [24].

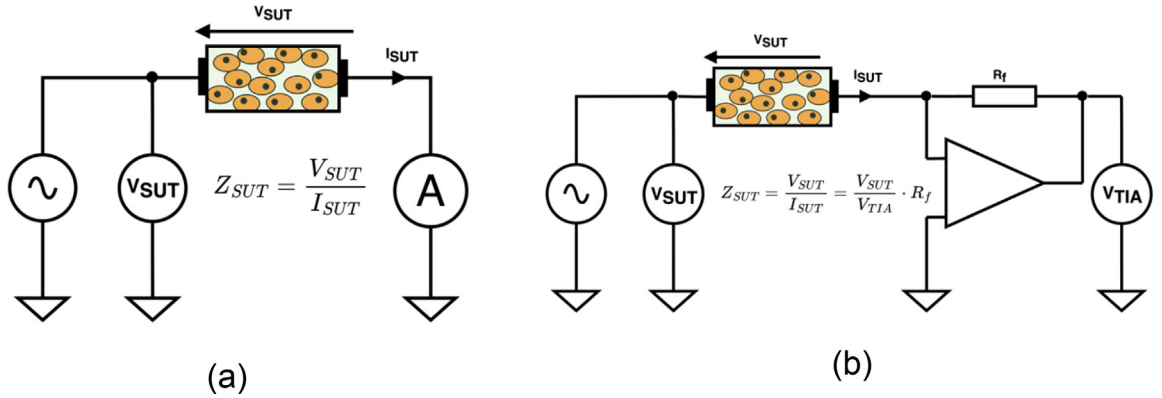

Fig. 1. Commonly used impedance measurement configuration under 100 MHz. (a) I/V configuration. (b) Auto-balancing bridge configuration.

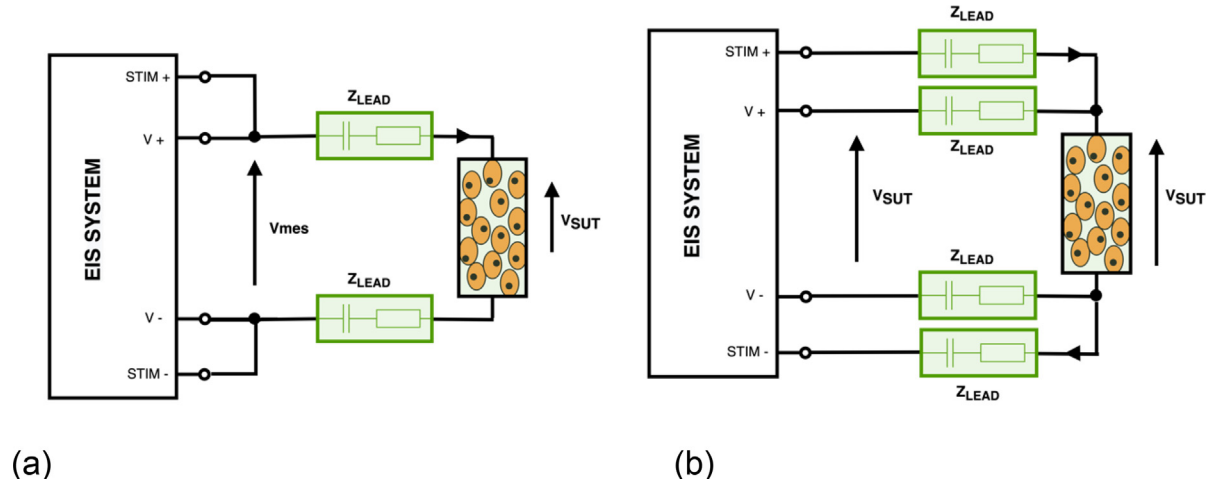

Fig. 2. Load connection methods. (a) 2-points configuration. (b) 4-points configuration.

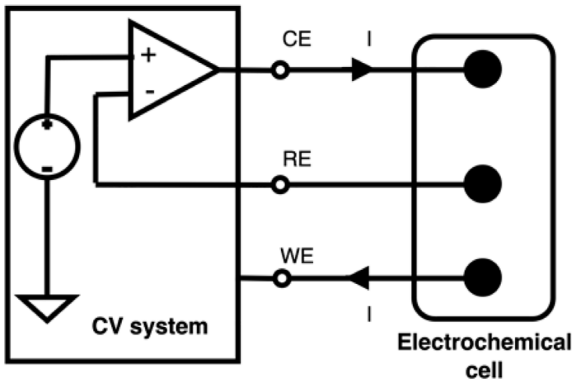

Fig. 3. Three-electrodes configuration with potentiostat feedback for cyclic voltammetry (CV). Electrode (electrochemical half-cell, or metal-electrolyte junction) under measurement is marked WE for Working Electrode, and two other contacts are used as a voltage reference, or Reference Electrode (RE), and a current return electrode, or Counter Electrode (CE).

Considering the need for measurements in various contexts, several impedance analyzer devices available on the market have been used for non-implanted experiments, such as the MFIA from Zurich Instruments, the 65120B from Wayne Kerr, or the 4294A from Keysight. Those devices offer a wide bandwidth (up to 120MHz for both the 65120B and the 4294A) on a wide range of loads, with excellent accuracy. However, those good performances come at a very expensive price (about $10,000 for the MFIA and more than $25,000 for the 65120B and 4294A), and large weight and dimensions. Those impedance analyzers are designed for electronic components characterization and are therefore not suited for measurement on implanted electrodes. Most benchtop commercially available impedance analyzers are not capable of tetrapolar measurement. An external front-end amplifier can be added to overcome this limitation [25]. The stimulus front end is also not adapted for the targeted application. For example, the MFIA can only do potentiostatic EIS. The 65120B and the 4294A can do both potentiostatic EIS and galvanostatic EIS. However, the minimum 200μA they can produce can be too high for measurement involving implantable electrodes, where it could be enough to trigger unwanted physiological responses [26]. Measurement time ranges from a few seconds to several minutes, which can also be problematic when measuring moving organs such as the lungs or heart [27].

Solutions have been proposed in the past years to perform EIS at a lower cost [28–30]. In Ref. [31], the authors propose a light battery-powered impedance analyzer. This device performs potentiostat EIS up to 10MHz with a 50mV excitation and is capable of both swept sine and multi-sine excitation. Similar performances are obtained with the FPGA-based galvanostatic EIS system presented in Ref. [32]. However, to the best of our knowledge, those designs are not fully reconfigurable, are not fully open-source, and are not easily replicable, and hardware and software can't be easily customized. On the other hand, there is a couple of open-design available for CV, such as the MYSTAT system [33]. However, this instrument is only capable of very low-frequency analysis and thus not capable of performing impedance spectroscopy. This paper addresses these issues and proposes an open-source design capable of both EIS and CV measurements on implanted dispositive. Our objec-

tive is to propose a measurement device capable of characterizing electrode tissues and tissue properties for the design of unconventional therapeutical interfaces [34] and in-vitro/in-vivo experiments (however non-chronic-implanted setup) aiming in investigating bioimpedance-based pathological markers [35,36].

Hardware description

The proposed system is depicted in Fig. 4 and comprises the following elements: i) a USB data acquisition and generation platform (Analog Discovery 2, Digilent, USA), in charge of the analog-to-digital and digital-to-analog conversions and digital processing; ii) an analog differential excitation front end, capable of applying a current-controlled waveform or a voltage-controlled waveform to the SUT, as well as potentiostat feedback for the CV measurement; iii) an analog differential current and voltage readout front end; iv) a reconfigurable SUT connection circuitry, in charge of the setting the connection mode to the load (2 wires or 4 wires), the coupling (AC or DC) and selecting the desired stimulus source (current controlled or voltage controlled); v) an STM32 microcontroller (ST microelectronics, Italy/France) to configure the system as defined by the user; vi) a power supply section to generate the multiple supply rails required.

Power supply

The analog excitation and readout front end are powered with a symmetrical ±12V supply generated with an isolated symmetrical DC/DC converter (TDN 5-0923WI, TracoPower, Switzerland), Fig. 5(a). This module accepts a wide input DC range, from 4.5V to 13.2V, and offers various protection such as overcurrent protection and reversed polarity while being compact (1.23 cm^3) and capable of outputting up to ±168mA. Galvanic isolation allows a floating system and thus improves safety. Galvanic isolation in a clinical environment is required by the IEC 60601-1 standard.

Three pairs of linear low dropout regulators (LDOs) are used to provide a clean, low noise, and stable ±11V3 (Fig. 5(b)). One pair is used for the excitation front end, one pair is used for the voltage readout front end, and the last one is for the current readout front end. Positive rail LDOs use LT1962, and negative rails are based on the LT1964, both manufactured by Linear Technology (USA). Using multiple pairs of LDOs reduces thermal stress for the components as well as crosstalk between sub-systems.

The digital part is powered with a second isolated DC/DC converter (TEC-3-0911, TracoPower, Switzerland), generating 5V (Fig. 5(c)). Using a separated and galvanically isolated supply for the digital part reduces the digital pollution on the analog circuitry. The 5V is lowered to 3 V3 required for the digital circuitry via a dedicated LDO (TLV702-33, Texas Instrument, USA).

The board can be powered either from a DC jack barrel connector, with an input range of 5V–12V, or from a dedicated USB-C connector. The input power selection between the jack barrel and USB-C connector is handled via a power path selector integrated circuit (LTC4416, Linear Technology, USA), Fig. 5(d). When both connectors are plugged to power, the highest input voltage is selected to power the system, via two low R_{DSon} PMOS (PMT200EPEX, Nexperia, Nederland).

Signal processing module

The signal processing part is built around the Analog Discovery 2 (AD2), a multifunction FPGA-based platform developed by Digilent (USA) and Analog Devices (USA). This low-cost, compact, and USB-powered platform is equipped with a 2-channels oscilloscope, a 2-channel arbitrary waveform generator (AWG), and digital I/Os to perform different operations

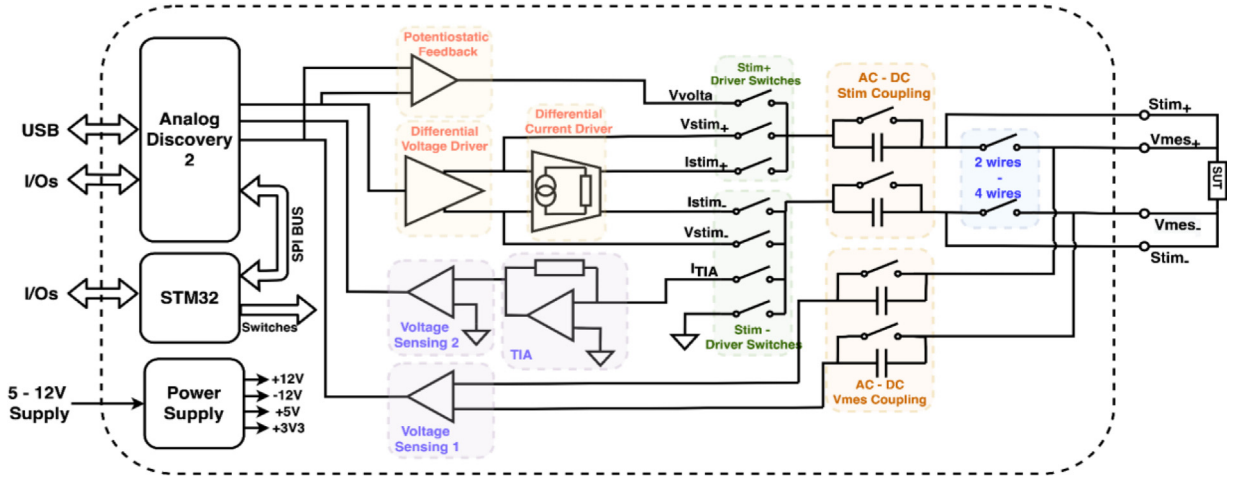

Fig. 4. Functional schematic of the proposed EIS system.

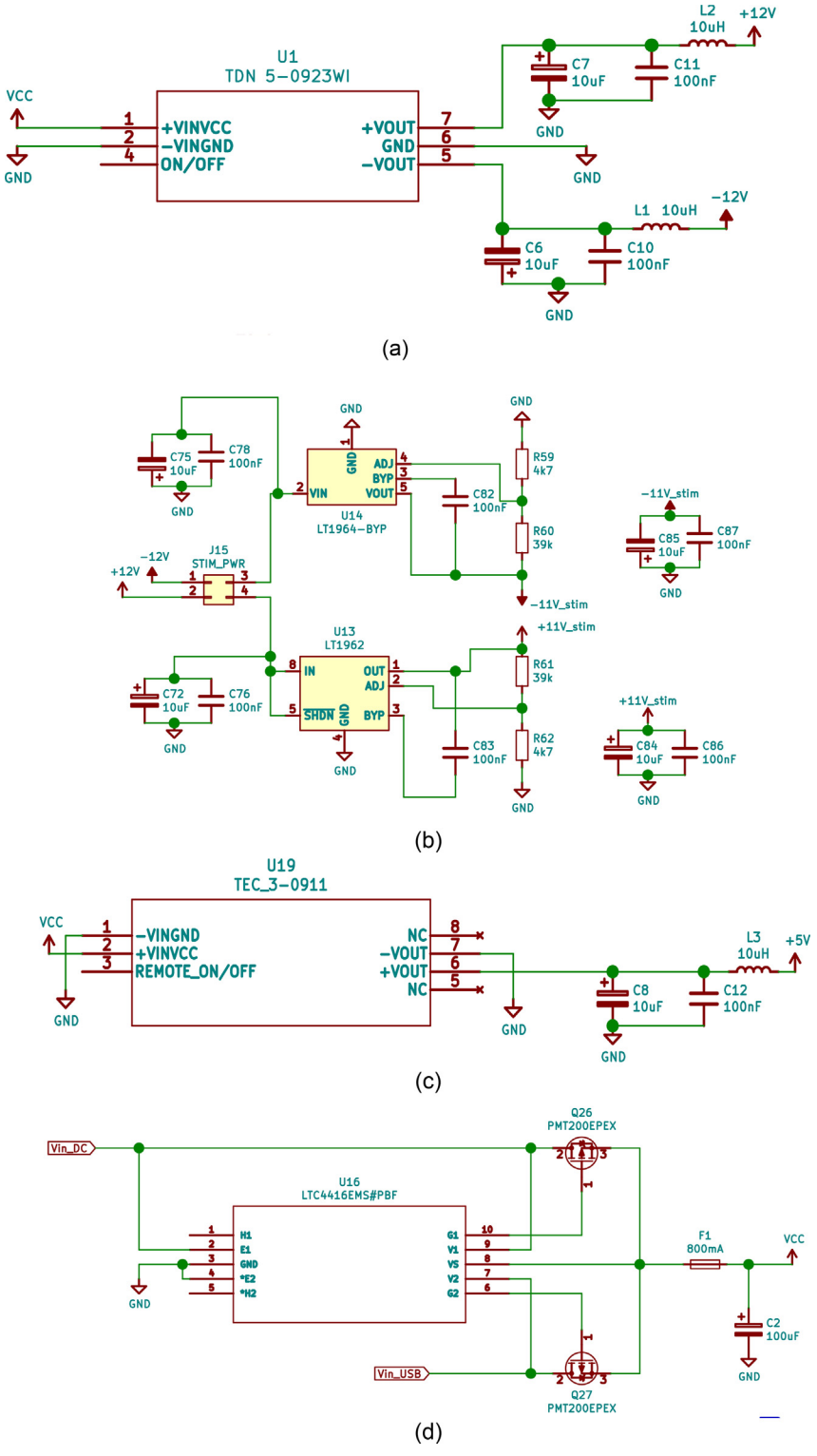

Fig. 5. Schematic of the power supply section. (a) U1 generates the ±12V rails from a single supply. C6, C7, C10, and C11 provide output decoupling. L1 and L2 provide additional current filtering. (b) U13 and U14 provide a clean and stable ±11 V3. Both rails are decoupled via C84 and C86, C85 and C87. Feedback resistor values (R61 and R62, R59 and R60) set the output value of the LDOs. (c) 5V Digital Supply is generated via U19 and is decoupled via C8 and C12. Additional filtering is provided via the inductor L3. (d) The power input path selection is handled by U16. Q26 and Q27 are capable of up to 2.4A continuous drain current.

(logic analyzer, pattern logger, etc.). The internal structure of the AD2 platform is shown in Fig. 6. On the analog acquisition side, the AD2 is equipped with a two-channel differential ADC (AD9648, Analog Devices, USA), capable of synchronous conversion at up to 100MS/s, with 14-bit resolution. Including the signal conditioning path, the acquisition side has about 30 MHz of bandwidth, with a 1MΩ input impedance and a ±25V input voltage compliance. The FPGA internal memory buffer allows it to store up to 16,384 samples per channel. The acquisition can be manually triggered from software, from an internal trigger, or from an external trigger. On the analog waveform generation path, the AD2 module is equipped with a 2-channel DAC (AD5643, Analog Devices, USA), generating arbitrary waveforms at a sample rate up to 100MS/s, and with a 14-bit resolution. Both channels can generate signals with a 12MHz bandwidth and ±5V voltage range. A buffer of 16,384 samples per channel is dedicated to storing custom arbitrary waveforms. Analog specifications are summarized in Table 1.

Choosing the AD2 platform over a custom solution has been dictated by several aspects. The data rate and memory requirement for both the waveform generation and acquisition, as well as the need for parallelism and accurate timing, make microcontrollers not relevant for the application. A dedicated FPGA with external ADC and DAC is an interesting alternative to the AD2 but requires advanced hardware and software design. Coastwise, a custom solution would also lead to higher prices as expensive parts and advanced manufacturing capabilities would have been required.

Differential voltage driver

The voltage driver is built in a 2-stages arrangement (Fig. 7). The first stage buffers the AWG output of the AD2 and amplifies the signal to match the maximum output swing possible of about ±10V. It is built around a wideband, high-slew rate FET-input op-amp (THS4631, Texas Instrument, USA). This op-amp is configured in a non-inverting amplifier topology with a gain of 2.2V/V. Its output is filtered with a simple RC filter cutting around 19MHz, to remove sampling noise from the AD2 DAC. The signal is converted to a differential signal with a 150MHz differential amplifier (THS4151, Texas Instrument, USA) capable of delivering up to 150mA to the load. Gain is set to unity via feedback resistors. Feedback capacitors are added in parallel to prevent oscillation.

Series resistors are added in the differential output path to avoid ringing or oscillations when driving capacitive loads, such as implantable electrodes [ref bioelectricity]. The maximum output swing is output ±10V on V_{in+} and V_{in-}, thus about ±20V on the load. Specifications are summarized in Table 2.

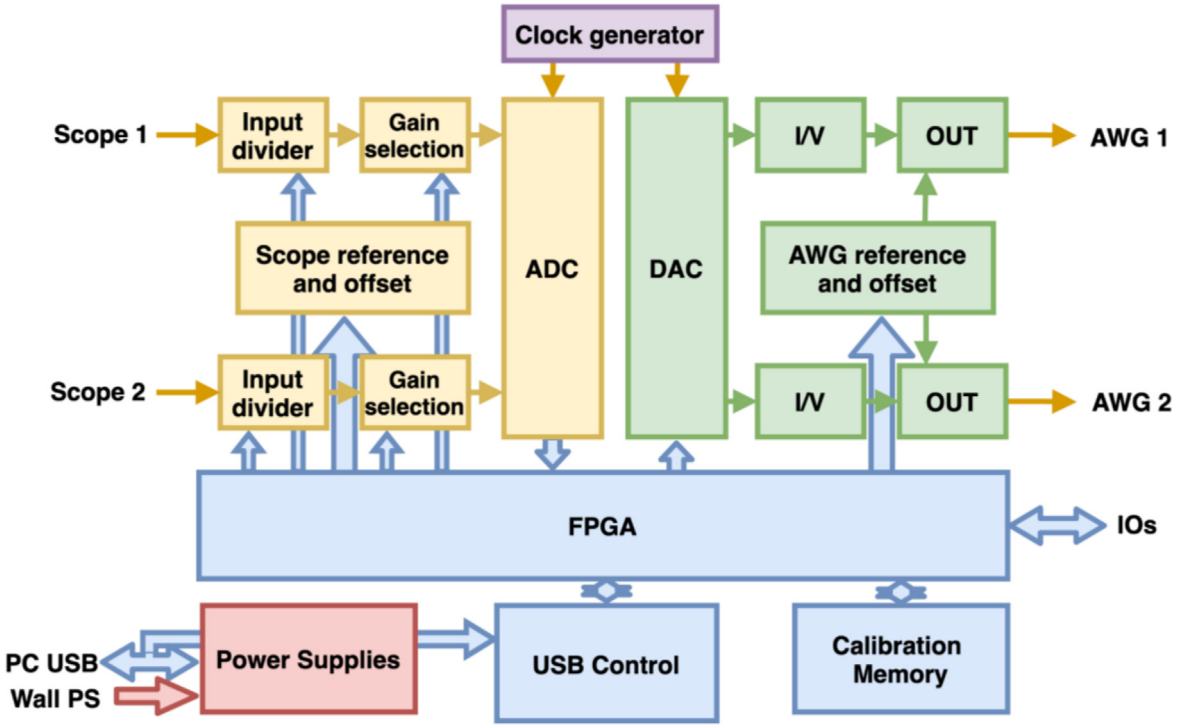

Fig. 6. Architecture of the Analog Discovery platform. Inspired by the AD2 reference manual.

Table 1
Analog capabilities of the Analog Discovery 2 platform. [1]Vertical scale is lesser than 0.5 V/div. [2]Vertical scale is greater than 0.5 V/div. [3] Voltage output is lesser than 1 V. [4]Voltage output is greater than 1 V.

Analog Inputs							
Resolution	Absolute Resolution[1]	Absolute Resolution[2]	Sample Rate	Input Impedance	Input Range	Bandwidth (−3dB)	Buffer Size
14-bit	0.32 mV	3.58 mV	100MS/s	1MΩ||24pF	±25 V	30 MHz	16 k samples
Analog Output							
Resolution	Absolute Resolution[3]	Absolution Resolution[4]	Sample Rate	AC amplitude	DC offset	Bandwidth (−3dB)	Buffer Size
14-bit	166 µV	665 µV	100MS/s	±5V	±5V	12 MHz	16 k samples

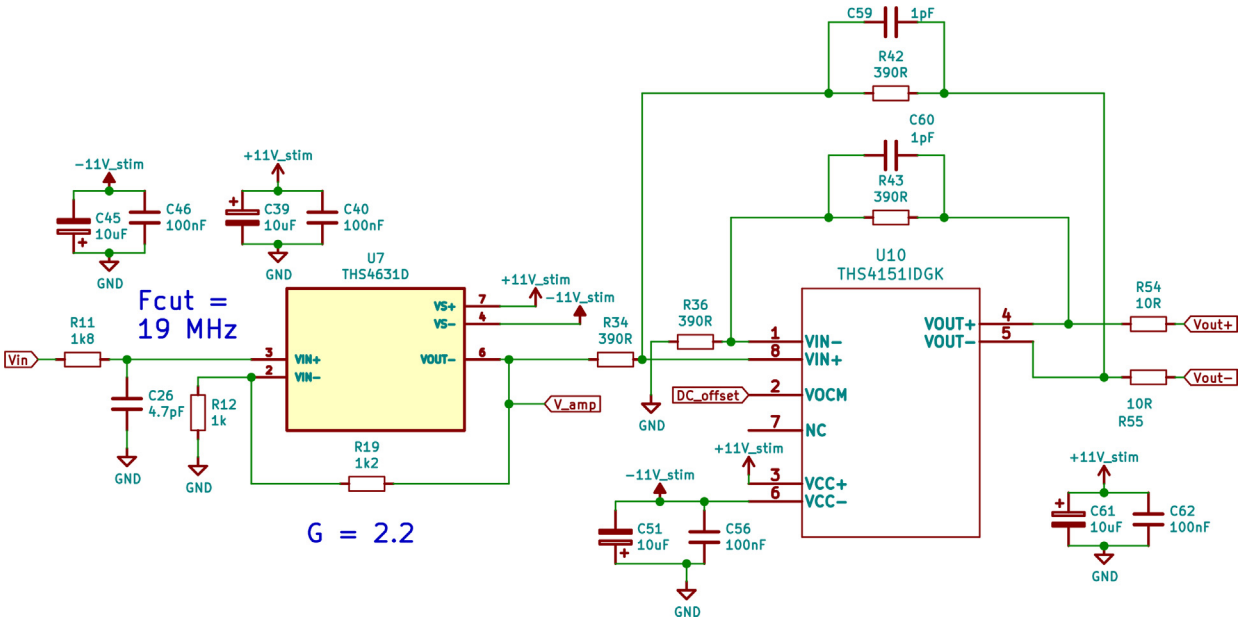

Fig. 7. AWG output is buffered and amplified with U7. Input is filtered with R11 and C26. A gain of 2.2 is set by R12 and R19. C39, C40, C45, and C46 are used for power supply decoupling. Single-ended to differential conversion is provided by U10. Conversion gain is set to one with R34, R36, R42, and R43. Stability is increased with C59 and C60, and R54 and R55 limit inrush current when driving capacitive loads. Power supply is decoupled with C51, C56, C61, and C62.

Table 2
Specifications of the differential voltage driver. [1]In the single-ended configuration. [2]In the differential configuration. [3]Slew-rate of the THS4631D differential driver.

Differential Voltage Driver						
Input Range	Output Range[1]	Output Range[2]	Output Current	Input filtering frequency	Input Bias Current	Slew Rate[3]
±5 V	±10 V	±20 V	150 mA	19 MHz	100 pA	650 V/µs

Differential current driver

A differential current-controlled source is also preferable to better reject common-mode voltage and increase dynamic range. Designing a differential current driver is challenging: a mismatch between the source and sink results in a parasitic current flowing to the ground through the large output resistor of the current source and creating a large common-mode voltage [37]. A differential current source with common-mode feedback (CMFB) has been developed to address this situation. In Ref. [38] the current course is split into two parts: a master source driver and a slave current sink (Fig. 8). The master driver is built around a current feedback topology, where the transconductance gain is set via the feedback resistor: $G = \frac{1}{R_f}$. On the over end, the slave driver is simply an inverting buffer. It senses the voltage at the source input and applies the inverted voltage to the sink input, thus sinking the same, but opposite sign, amount of current that is sourced by the master.

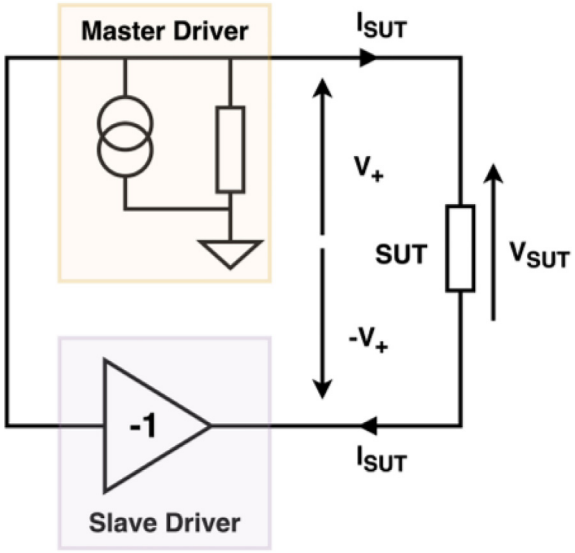

Fig. 8. Simplified schematic of the differential current driver with common-mode feedback.

The discrete implementation of the differential current driver with CMFB is built with two high-speed difference amplifiers (AD830, Analog Devices, USA), similar to the presented current driver in Ref. [39] (Fig. 9). Two transconductance gains can be selected via a dedicated relay and two resistors in the feedback loop. For each gain, an additional trimmer is added to

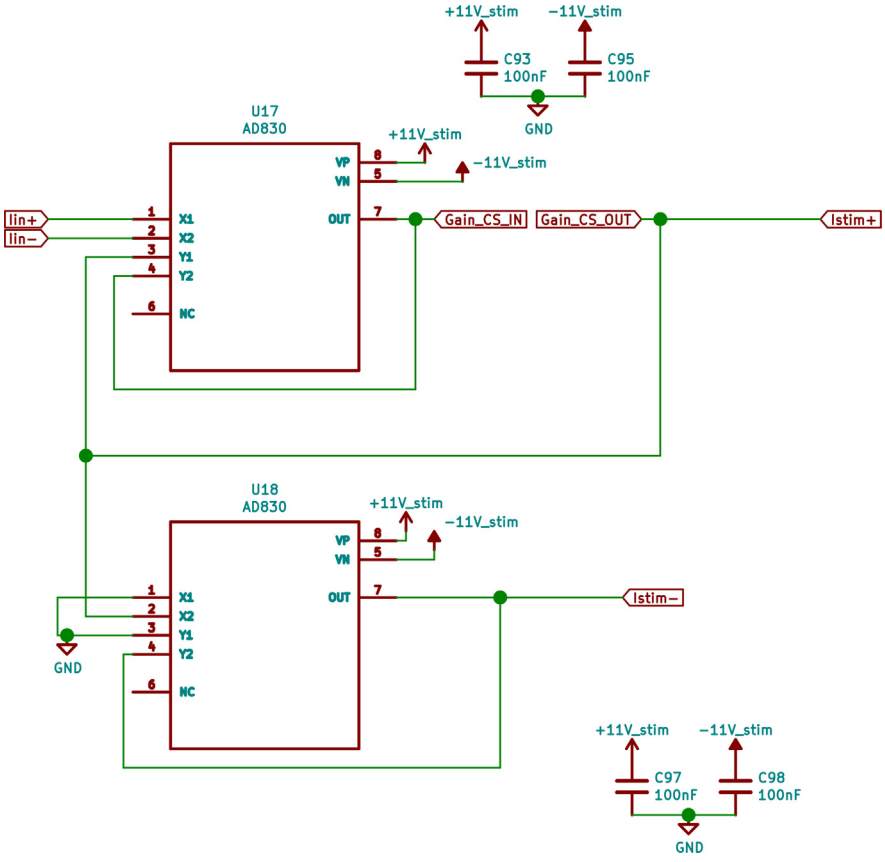

Fig. 9. Schematic of the differential current driver. U17 is the master current sourcing driver and U18 is the slave current sinking driver used for the CMFB topology. C93, C95, C97, and C98 are used for power supply decoupling. A relay connects 'Gain_CS_IN' and 'Gain_CS_OUT' via a resistor to set the desired driver's gain (High or Low).

adjust the gain to the desired value. With the current implementation, the low gain can be adjusted from 11μA/V to 21μA/V and the high gain can be tuned from 91μA/V to 1mA/V. AD830 inputs are clamped internally to 2.4V, thus the maximum current possible is 51μA in the low gain mode and 2.4mA in the high gain mode. Specifications are summarized in Table 3.

Differential transimpedance amplifier

In the auto-balancing bridge configuration, the current flowing through the load is sensed via a trans-impedance amplifier (TIA). In its standard configurations (Fig. 10(a) and (b)) the current I_{SUT} flowing through the load goes through the feedback resistor R_f. The very high differential gain of the op-amp forces that $V_{in+} = V_{in-} = 0V$. Thus, TIA virtually connects the load to the ground, and the op-amp output becomes $V_{TIA} = R_f \hat{A} \cdot I_{SUT}$.

To drive the load with a differential voltage driver while measuring the current flowing through it via the TIA, we propose to connect the inverting output of the voltage source V_- to the non-inverting input of the TIA op-amp V_{in+} (Fig. 10(c)). Because $V_+ = V_-$, the TIA virtually connects the load to V_-, maintaining the differential voltage across the load. The TIA's output voltage becomes $V_{TIA} = R_f \hat{A} \cdot I_{SUT} + V_-$. By measuring the potential $V_{TIA} - V_-$, the image of the current flowing through the load can be measured. The same principle can be applied to the differential current driver presented previously (Fig. 10 (d)). The potential generated by the current-sinking slave is applied to the non-inverting input of the TIA. This potential is duplicated at the inverting input of the TIA, virtually connecting the load to the current-sinking path.

Fig. 11 presents the schematic used in the presented system. The TIA is built around the THS4631 op-amp (Texas Instrument, USA). It is stable at unity gain which is a primary requirement for an op-amp used as a TIA. This op-amp also offers a large bandwidth of 325MHz and a high slew rate of about900V/μs. Its FET inputs make its input current negligible. A 1kΩ feedback resistor sets the TIA gain to 1V/mA. An expensive precision resistor is avoided by characterizing the TIA gain with software calibration. A 0.5pF capacitor is added in parallel to the feedback resistor to stabilize the TIA and avoid instabilities at high frequencies.

The non-inverting input can be connected either to the negative output of the voltage source, the negative output of the current source, or grounded. This selection is made via two relays. The input of the TIA can also be AC coupled via a pair of 1μF coupling capacitors. Those capacitors can be shunted to DC couple the TIA's inputs, via a relay. Specifications of the differential TIA are summarized in Table 4.

Voltage readout

Two identical voltage readout elements are used in the system. The first one is used to measure the voltage across the SUT during measurement. The second channel is connected to the TIA's output, as shown in Fig. 10. Because those two channels have identical bandwidths, high-frequency attenuation is compensated when the voltage over current ratio is computed for impedance estimation. Voltage readout is realized with two 10MHz programmable gain instrumentation amplifiers (AD8250, Analog Devices, USA) (Fig. 12). The gain for both instrumentation amplifiers can be digitally selected between 1, 2, 5, and 10V/V via a 2-bits word. Gain can be automatically adjusted to optimize the dynamic range and thus the signal-to-noise ratio (SNR). Splitting the total gain between two stages increases the gain-bandwidth product. A 16MHz RC low pass filter is added between the two stages to remove high-frequency noise from the recorded voltage. Voltage readout inputs can be AC-coupled if needed, via a pair of 1μF coupling capacitors. Specifications are summarized in Table 5.

Potentiostat feedback

The potentiostat feedback schematic is inspired by Ref. [33]. Fig. 13 shows the potentiostat feedback realized with an OPA192 op-amp (Texas Instrument, USA). The OPAx192 op-amp family are high-precision, low offset voltage, and rail-to-rail op-amps. Those good DC performances are crucial in this application. The desired voltage applied to the op-amp non-inverting input is compared to the potential of the reference electrode (RE). The op-amp output current is injected into the counter electrode (CE) and is adjusted until the reference electrode potential equals RE potential voltage.

Digital control

The analog excitation and readout front ends are configured and connected via electromechanical relays. Relays are cheap, reliable, and easy to drive. They also have fewer ON resistor in comparison to solid-state switches, as well as much less crosstalk. They also provide galvanic isolation between the digital driving path and the analog circuitry. A microcontroller is dedicated to control relays (STM32F103, STMicroelectronics, Italy/France). Each relay of the system is driven by the STM32 via an NMOS and is equipped with a flywheel diode to eliminate flyback due to the inductive coil of the relay. STM32 microcontrollers require only a couple of decoupling capacitors to be functional (Fig. 14). An external 16MHz crystal is used for its internal clock and is translated to 72 MHz via an internal PLL to run the CPU core. A 1.27 mm 10 pins serial wire debugging (SWD) connector is used for programming. Two LEDs can be directly controlled by the microcontroller.

Table 3
Specification of the differential current driver with CMFB. (1)Low gain mode. (2)High gain mode.

Differential Current Driver						
Input Range	Gain(1)	Gain(2)	Max current(1)	Max current(2)	Input Bias Current	Output Voltage Swing
±2.4 V	11µA/V–21µA/V	91µA/V–1mA/V	51µA	2.4mA	10µA	±3.5 V

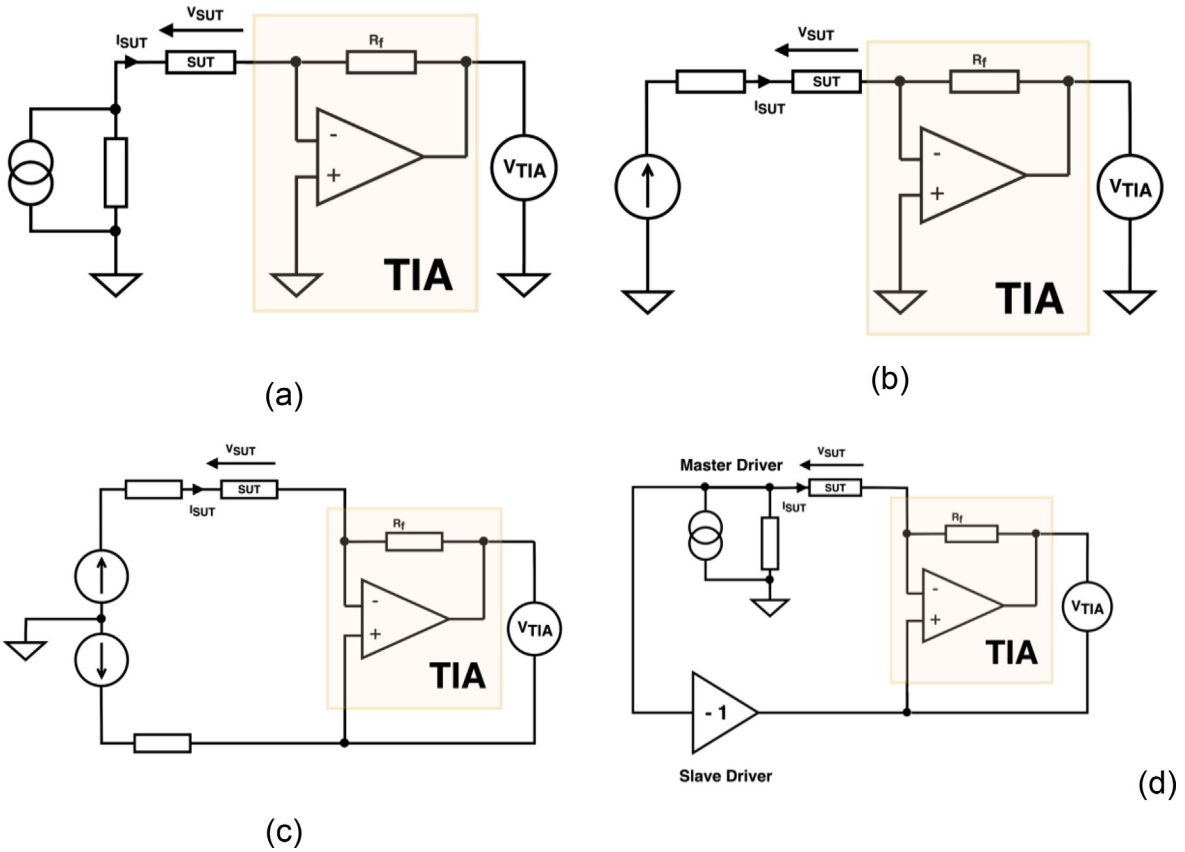

Fig. 10. Connection to the trans-impedance amplifier – TIA. (a) To a single-ended current source. (b) To a single-ended voltage source. (c) To a differential voltage source. (d) To a differential CMFB current source.

Two tactile switches can be used for various purposes, such as manually setting a specific configuration. A full-duplex SPI bus connects the microcontroller to the AD2, where the AD2 is the SPI master and the STM32 a slave. The AD2 is used as a bridge to control the STM32 via a computer interface.

PCB layout

The layout is made using a 4-layer stack. The top layer is privileged for analog signals, inner layers are mainly used as a continuous ground plane for the analog parts and for some digital routing. The bottom layer is used for power routing. A ground plane is used on the four layers. Short and direct connections are privileged, and analog parts routing is done with extra care. Decoupling capacitors are placed as close as possible to the ICs. Digital circuits and switched-mode converters are placed away from the sensitive analog parts. LDOs are close to their target analog block to keep analog supply rails away from the digital circuitry. The AD2 PCB can be placed on top of the digital circuitry and secured with spacers.

STM32 software

The STM32 microcontroller is programmed in C++ language using the MBED framework. The communication between the microcontroller and the AD2 is realized over a full-duplex 10 Mb/s 32-bit Serial Protocol Interface (SPI) bus. A simple

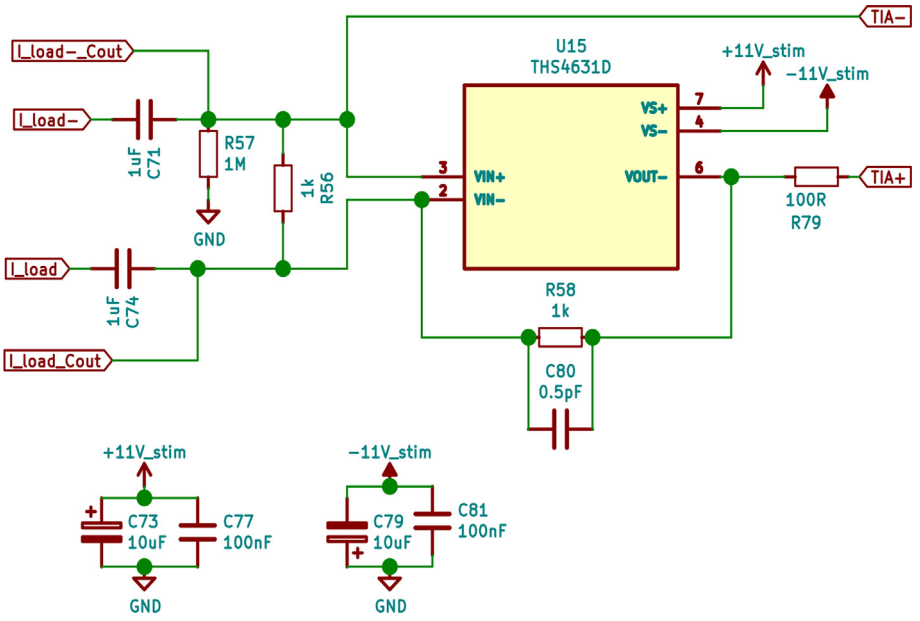

Fig. 11. Schematic of the differential transimpedance amplifier. U15 is decoupled on both supply rails via C73, C77, C79, and C81. C71 and C74 are for AC coupling of the input path and are shorted via a relay when input coupling is DC. R58 sets the gain of the TIA to 1 mA/V, and C80 limits its bandwidth to stabilize it.

Table 4
Specifications of the differential transimpedance amplifier. [(1)]In differential mode.

Differential Transimpedance Amplifier					
Gain	Input Coupling	Max Current	Feedback Cut-off frequency	Maximum Input Voltage[(1)]	Input Bias Current
1 mA/V	*ACorDC*	±10mA	34MHz	±10V	100pA

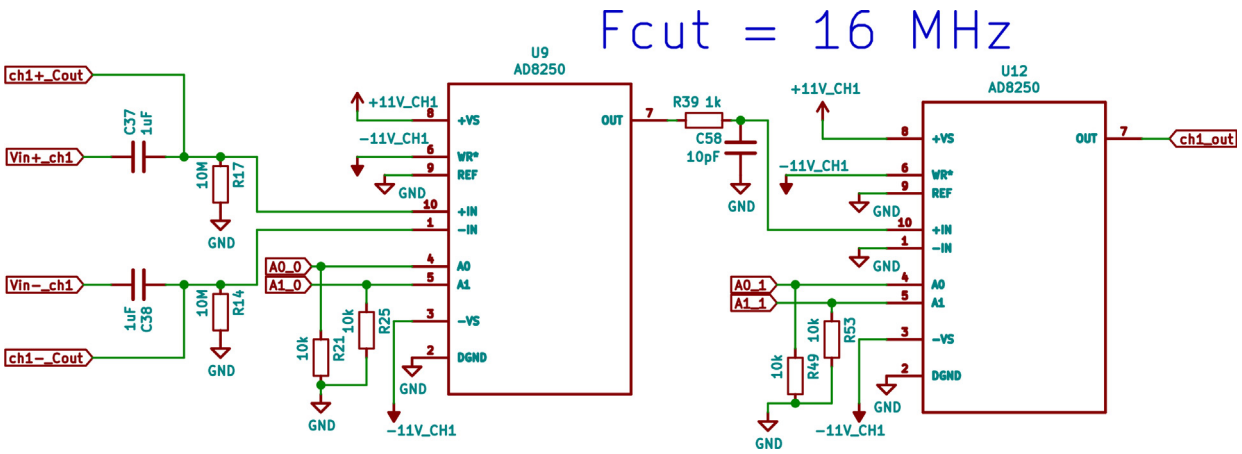

Fig. 12. Schematic of the differential voltage sensing circuit. R21, R25, R49, and R53 are pull-down resistors for the gain-setting pins of U9 and U12. C25, C28, C32, and C34 (not represented) are decoupling capacitors for U9. C64, C66, C69, and C70 (not represented) are decoupling capacitors for U12. C37 and C38 allow AC coupling if needed and are shorted with a relay when DC coupling is needed. R14 and R17 provide a path for the U9 biasing current when AC coupling. R39 and C58 form a 19 MHz low pass RC filter to filter out-of-band noise.

communication protocol between the AD2 and the STM32 allows a flexible read-and-write register scheme. The data format is depicted in Table 6.

The first 4-bit refers to a command, while the 28 last bits are the associated data. The currently supported commands are presented in Table 7.

Table 5
Specification of the voltage readout. [1]Gain >10 V/V.

Voltage Readout					
Input Range	Gain	Output Range	Input Bias Current	Bandwidth (−3 dB)	Common-Mode Input voltage
±10 V	1, 2, 5, 10, 20, 50, 100V/V	±10 V	30nA	10MHz 3MHz[1]	±10 V

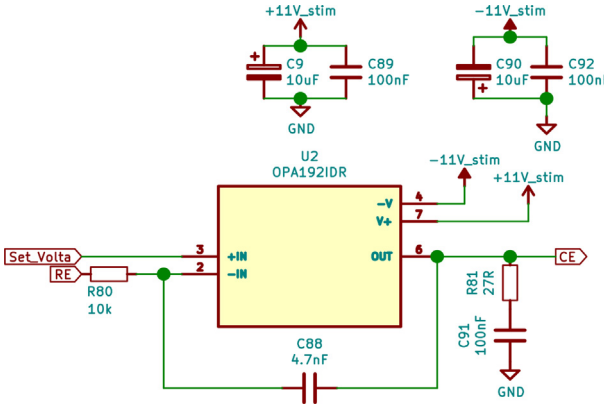

Fig. 13. Schematic of the potentiostat feedback circuit. U2 supply rails are decoupled via C9, C89, C90, and C92. R80 and C88 limit the feedback bandwidth to about 3kHz to prevent oscillation. R81 and C91 form a snubber-type network to increase stability when driving capacitive loads.

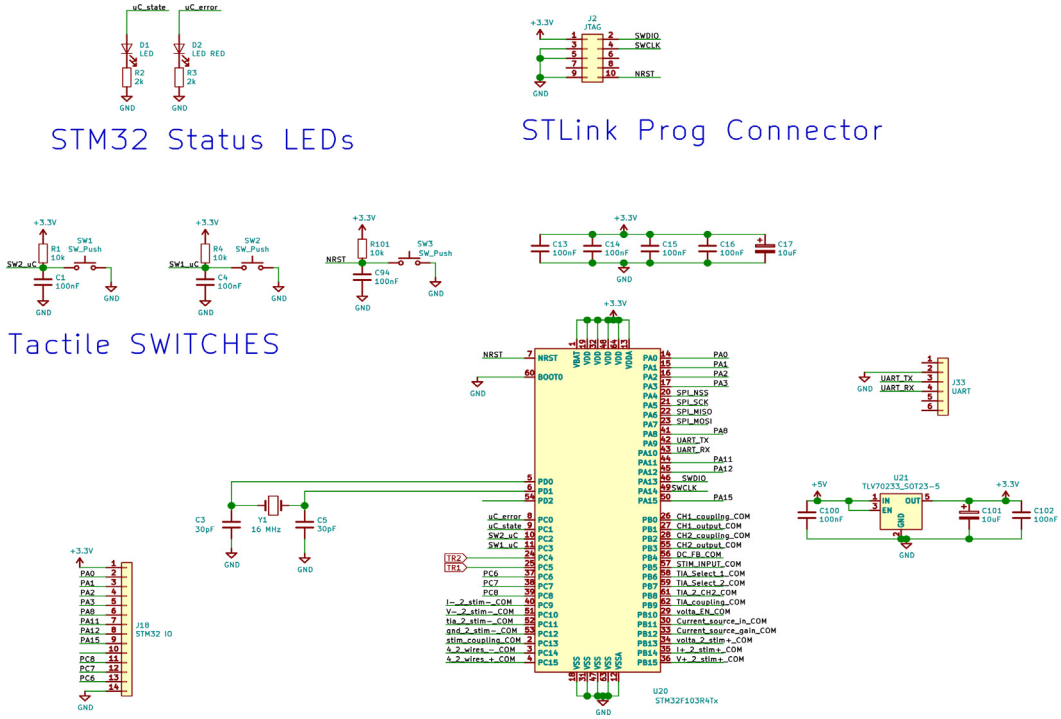

Fig. 14. Schematic of the digital control circuitry. C13–C17 are decoupling capacitors for the digital 3 V3 LDO U7. C3 and C5 are loading capacitance required by the 16 MHz crystal oscillator Y1. SW3 is a reset switch for the STM32. R1, C1, R4, C4, R101, and C94 are debouncing filters for SW1, SW2 and SW3. C100 to C102 are decoupling capacitors for U21. A UART interface can be used to bypass the AD2 to control the STM32 directly (J33). Non-utilized STM32 pins are deported to an external connector, facilitating connection to other hardware (J18).

Table 6
Data format of the 32-bit SPI communication between AD2 and STM32 microcontroller.

	MSB							LSB
Bits	31–28	27–24	23–20	19–16	15–12	11–8	7–4	3–0
Value	Command	← Data →						

Table 7
Register map.

Command	Description	Data
0x00	Do nothing	x
0x01	Set STM32 state	STM32 State
0x02	Set Relay state	Relay value
0x03	Read Register	Register address
0x04 to 0x0F	Not Used yet	x

Set STM32 state (0x01)

This command sets the internal state of the STM32. The *Off_state* (data = 0x00), relays on the board are set to their default value, and changing their status is not permitted. This mode is the default mode when the board is powered. In the *Idle_state* mode (data = 0x01), the configuration of the relay can be changed. This mode is utilized to set the board configuration. In the *Locked_state* (data = 0x02), relays are maintained in their current configuration but can't be changed. This mode is used to lock the current configuration during measurement. If any error occurs, the STM32 goes to the *Error_state*. Error can be cleared by setting the STM32 state to *Off_state*. This mode can also be set externally by setting data to 0x03.

Set relay state (0x02)

This command sets the state of the relays on the board. This command is only accessible in the *Idle_state*. Each bit of the Data value corresponds to the state of a specific relay. The corresponding table between bits and relays is presented in Table 8.

Read register (0x03)

After a Read Register command, the STM32 will load in the transmit SPI buffer the value of the requested register. The address of the register to be read is defined in the Data part. Currently, only two registers of the STM32 can be read: the board ID (address: 0x00) and the current state of the board (address: 0x01).

Board ID

Each board is individually named via a hardcoded ID in the STM32 memory. Its ID can be read at the 0x00 register address. This unique ID allows specific calibration data for each board.

Python library

We developed a Python3 library to enable simple and fast user-friendly scripting for measurements. The library is object-oriented and measurement boards are declared as unique boards, each one having a specific ID number. Boards are identified according to their Analog Discovery 2 ID and serial number. The global architecture of the library relies on two classes described in the UML class diagram provided in Fig. 15.

We developed a class dedicated to the Analog Discovery 2 hardware, overloading Digilent's existing code to get simple methods for generic signal generation and acquisition, as well as digital I/O communication to reach the embedded microcontrollers of our design. An instance of this class, Andi, is contained in the class to be instantiated by the final user, BIMMS. This class hosts attributes to store the relay states, gains, and calibration data and has top-level methods for rapid measurement with the board corresponding to the different experimental configurations.

Design files

Table 9 summarized the file provided to duplicate the presented system.

Bill of materials

The complete bill of material can be found on the Zenodo deposit. The excel document sheets include all required components, as well as the external power supply, cables, and accessories. The total cost is about $650, including the price of the AD2 ($399). The AD2 can be found at $279 with academic pricing, reducing the total cost to around $530.

Table 8
Corresponding table between relays and bits.

Bits	Relay Name	STM32 pin	Function	Default state
0	Ch1Coupling_rly	PB0	Channel 1 Coupling	DC coupled
1	Chan1Scope1_rly	PB1	Connect Channel 1 to scope 1	Unconnected
2	Ch2Coupling_rly	PB2	Channel 2 Coupling	DC coupled
3	Chan2Scope1_rly	PB3	Connect Channel 2 to scope 2	Unconnected
4	DCFeedback_rly	PB4	DC Feedback mode	GND
5	InternalAWG_rly	PB5	Select AWG1 or EXT_stim	AWG1
6	TIANegIn1_rly	PB6	TIA Negative Input Selection 1	GND
7	TIANegIn2_rly	PB7	TIA Negative Input Selection 2	Vout−
8	TIA2Chan2_rly	PB8	Connect TIA to Channel 2	Connected
9	TIACoupling_rly	PB9	TIA Input Coupling	DC Coupled
10	EnPotentiostat_rly	PB10	Enable potentiostat feedback	Grounded
11	EnCurrentSource_rly	PB11	Select current source input	Vout
12	GainCurrentSource_rly	PB12	Select Current Source Gain	Low Gain
13	Pot2StimPos_rly	PB13	Connect Potentiostat to Stim +	Unconnected
14	Ipos2StimPos_rly	PB14	Connect I+ to Stim+	Unconnected
15	VoutPos2StimPos_rly	PB15	Connect Vout+ to Stim+	Unconnected
16	Ineg2StimNeg_rly	PC9	Connect I− to Stim−	Unconnected
17	VoutNeg2StimNeg_rly	PC10	Connect Vout− to Stim−	Unconnected
18	TIA2StimNeg_rly	PC11	Connect TIA to Stim−	Unconnected
19	GND2StimNeg_rly	PC12	Connect GND to Stim−	Unconnected
20	StimCoupling_rly	PC13	Stimulation Coupling	AC Coupled
21	StimNeg2VNeg_ryl	PC14	Connect Stim− to V−	Unconnected
22	StimPos2VPos_rly	PC15	Connect Stim+ to V+	Unconnected

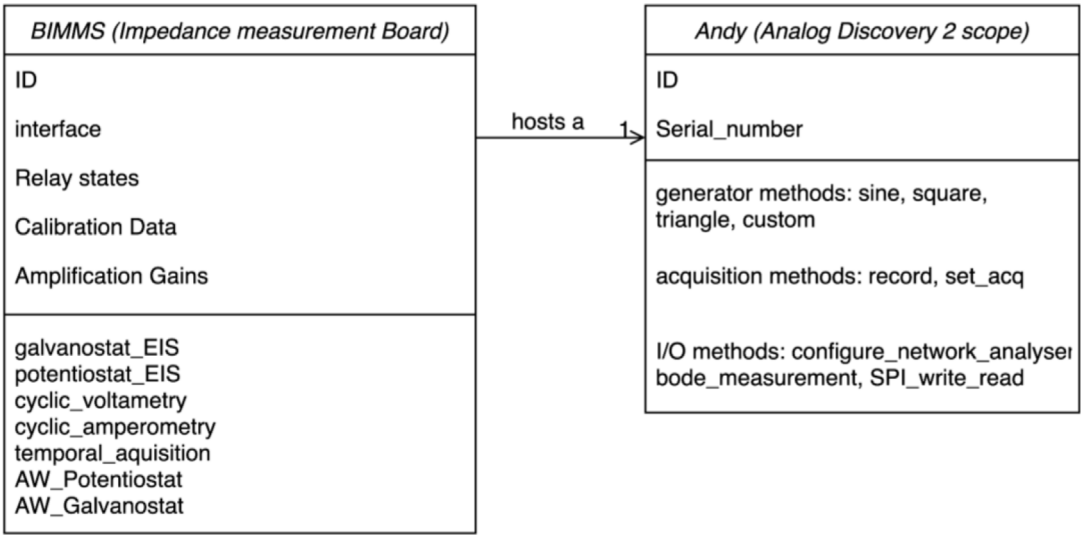

Fig. 15. Synthetic UML class diagram of the BIMMS Python3 library.

Table 9
Design files summary.

Design file name	File type	Open-Source license	Location of the file
schematic.pdf	*Electrical Schematic*	*CC BY 4.0*	https://doi.org/10.5281/zenodo.7148811
component_placement.pdf	PCB Component placement	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
layout.pdf	PCB layout	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
kicad.zip	KICAD Design files	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
gerber.zip	Gerber Files	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
BOM.zip	Bill of Materials	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
PCBWay.zip	Fabrication file required by PCBWAY.com	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
BIMMS_STM32_cubeIDE.zip	STM32 source code (Cube IDE)	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
BIMMS_STM32_V0.tgz	STM32 source code (MBED)	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
python.zip	Python API and examples.	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811
SuppMaterials.pdf	Supplementary materials	CC BY 4.0	https://doi.org/10.5281/zenodo.7148811

Build instructions

Procurement of parts

Any listed parts can be purchased from electronic retailers such as Mouser, Farnell, or Digikey. Passive components can be substituted with alternative parts. We recommend using at least 1% thin-film resistors, and 10% 25 V X7R or C0G ceramic capacitors when possible. Polarized tantalum can be used for large decoupling capacitors. We don't recommend substituting active parts such as op-amp. Although if you need to, one should be very careful to choose pin-to-pin compatible parts, and similar or higher voltage ratings. Surrounding passives might need to be tuned to accommodate alternative active components.

PCB fabrication

The board is a 4 layers PCB of 262 per 120 mm. We suggest using a prototyping PCB manufacturing service such as JLCPCB or PCBWAY.com. ENIG finish is suggested as it facilitates part placement. The cost of a PCB with ENIG finish is about $9 per board for a 10 PCBs order at JLCPCB.com, and $20 at PCBWAY.com.

Board assembly

Assembly can be manufactured by PCB prototyping companies such as JLCPCB or PCBWAY. A pick-and-place file needs to be generated for automatic assembly. The archive *PCBWay.zip* contains all the required files for PCB fabrication plus SMT part placements via PCBWAY services. The cost is about $300 per board for 8 boards. Purchase and manual assembly of through holes components will be required. JLCPCB offers cheap assembly but only for a limited number of references. Only passive components and a couple of active parts will be soldering. The remaining parts will need to be separately purchased and manually soldered.

In the case of a complete manual assembly of the board, we strongly suggest buying a stencil when fabricating the PCB. Then, solder paste can be easily applied to the solder pads, and SMT can be picked and placed on the board. Fine-tipped forceps or a vacuum pen can be used to facilitate the positioning of components on the board. Then, a reflow oven or vapor phase oven is needed to reflow the solder paste. Alternatively, a hot air soldering station can be used. However, this method does not allow the temperature to follow the recommended profile. We also suggest using it in combination with a hot plate station to harmonize the temperature on the board and thus limit thermal stress. We recommend using eutectic tin/lead solder to solder through-hole and remaining SMT parts. A thin and long solder tip is required to solder relays.

Initial electrical testing

After a careful inspection of all the soldering joints with binoculars or magnifying glasses, the board can be powered. Before applying any power to the board, we suggest unplugging everything, including the AD2 board. We also suggest disconnecting analog blocks by removing jumpers J5, J4, and J15 (Fig. 16). A benchtop power supply with current limiting capability is recommended for the first powering of the board. The voltage supply should be set between 5 V and 12 V. The current limit should be set to about 500–600 mA. Once powered, LEDs D3, D4, D5, and D28 should light up. We recommend checking various voltages with a multimeter. +12 V and −12 V power rails can be measured on connector J3. 3 V3 and 5 V rails can be measured on one edge of D5 and D28 respectively. Then, jumpers can be added on J5 to power channel 1. D10 and D13 should light up. The voltage across C19 should be about +11 V3 and the voltage across C21 should be about −11 V3. No excessive temperature should be observed on U4, U6, U9, or U12. Similar tests can be realized on channel 2, by adding jumpers on J4. Ultimately, jumpers need to be added to J15 to power the excitation analog block. D18 and D19 should light up. The voltage across C72 should be about +11 V3 and −11 V3 across C75. U10 and U15 tend to warm up a little bit, to about 50–55 °C. No excessive temperature should be observed on the other chips.

The next step is programming the STM32 microcontroller. Programming required the purchase of a low-cost programming device (ST-link V3 is recommended). An alternative option is to use the SWD connector on STM32 development boards such as Nucleo boards. For programming, two options are possible. Programming via the MBED Studio software, or just by copying the bin file into the USB device folder corresponding to the ST-link. MBED project and bin files are provided in the *BIMMS_STM32_V0.tgz* archive. Alternatively, CubeMx IDE from STMicroelectronics can be used, with the *BIMMS_STM32_cubeIDE.zip* archive. The board should be powered during the flashing of the microcontroller. Once programmed, D1 should start blinking at a rate of 1 Hz.

Ultimately, the system can be tested with a computer. The python API can be installed with the pip packet-management system. The Waveform software from Digilent needs to be installed separately. The board can be tested via test scripts available on the Zenodo depository. The *test_all.py* will call all the scripts located in the directory *unitary_test*. Each script tests a specific functionality of the board: communication with the AD2, communication between the STM32 and AD2, the output of channels 1 and 2, etc. Once all the tests are passed without any errors, the benchtop power supply can be swapped with a USB C power supply or DC jack barrel supply.

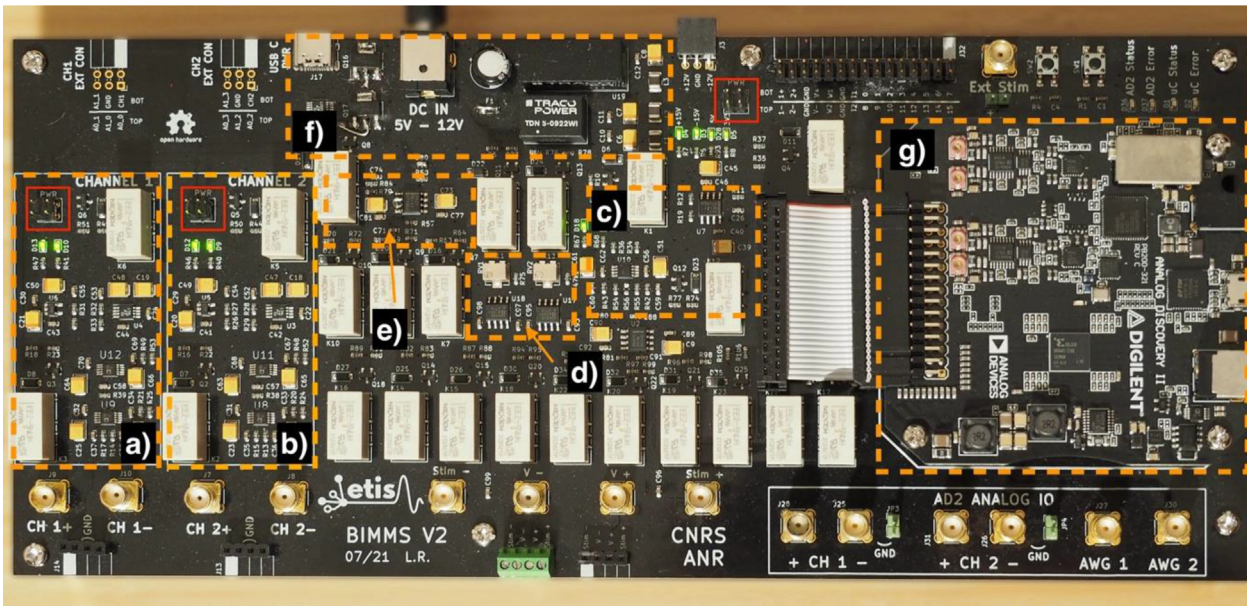

Fig. 16. Mains blocks of the system are highlighted in orange. a) and b) are respectively voltage readout channels 1 and 2; c) and d) are respectively the voltage stimulation circuit and the current source; e) the transimpedance amplifier; f) power supply section; g) Analog Discovery 2 PCB removed from its original enclosure and secured on top of the system. Jumpers on J4, J5, and J15 (in the red boxes) are removed before testing power supplies. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Operation instructions

The BIMMS platform is controlled from a computer via the AD2 USB connection. It is possible to run the BIMMS software on the Windows, Linux, or macOS operating systems. As no powerful computation is required, the system can be accessed from a cheap and compact microcomputer such as a Raspberry Pi 4. The system can be either controlled via python script with an object-oriented high-level API or via a dedicated minimalistic GUI.

Python API

The API handles the low-level communication with the BIMMS platform to configure the AD2 and the microcontroller. Basic methods allow to set the board state (idle, locked, off, error), setting the excitation front-end configuration (current or voltage mode, single-ended or differential, DC or AC coupling, etc.), and the readout front-end configuration (IAs gains, coupling, etc.). Higher-level methods are also provided to facilitate the usage of the board and to make its configuration transparent to the end user. High-level methods include a galvanostatic EIS measurement method, a potentiostatic EIS measurement method, and a cyclic voltammetry measurement method. The API facilitates scripting for automated measurement setups. Detailed examples are provided with the API.

The API is open source (under CeCILL license), referenced in Pypi (https://pypi.org/project/bimms/), and can therefore be automatically installed with all dependencies. The version corresponding to the results presented in this paper is 0.0.1.

Gui

A Graphical User Interface (GUI) application is provided to the user to easily perform EIS measurements. The GUI is based on the developed python API and uses the PyQt package for the graphical aspect. The PyQt package needs to be installed separately with the pip command for example. The GUI can be run on a Windows, macOS, or Linux computer. The GUI can be executed by running the script named *EIS_GUI.py* located in the *examples* folder of the python API. A window like the one in Fig. 17 should appear. The GUI allows the user to configure the system, run the measurement, plot the result, and save it in a CSV file.

Calibration

Two calibration procedures are provided to compensate for the resistors and capacitors' lack of precision and the influence of various parasitic: i) the DC calibration procedure (DCCalibration.py) estimates the gain of the TIA, of the current source and the voltage source, thus enabling accurate estimation of the measured current as well as the stimulation voltage

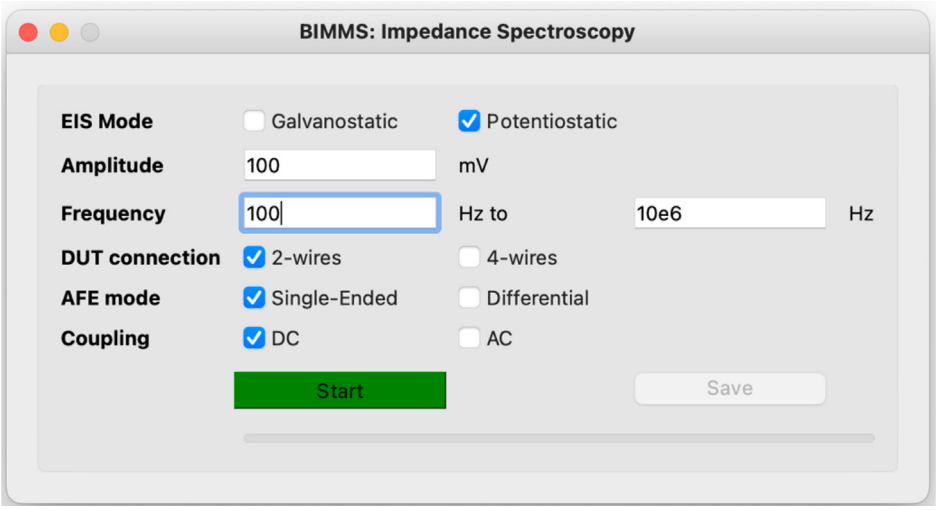

Fig. 17. Python GUI for EIS measurements.

or current. This first calibration method is convenient for quick analysis but lacks precision at high frequencies. This latter does not consider frequency dependent parasitic such as stray capacitance. ii) An Open-Short-Load calibration [40] procedure is provided (OSLCalibration.py) to improve the high-frequency measurement accuracy. Reference measurements are performed on an open load, a short load, and a reference load. The calibration is then applied to the measured unknown impedance using the following formula:

$$Z_{cal} = \frac{Z_r(Z_{uncal} - Z_{short})(Z_{open} - Z_{rm})}{(Z_{openl} - Z_{uncal})(Z_{zm} - Z_{short})}$$

where Z_{short} is the short load impedance Z_{open} is the open load impedance, Z_r is the known reference load impedance, Z_{rm} is the measured reference load impedance, Z_{uncal} is the un-calibrated measured load impedance and Z_{cal} is the calibrated measured load impedance.

Data are first filtered using a Savitzky-Golay filter and then fitted using polynomial equations. This strategy removes most of the noise of the calibration data and reduces the amount of data to be saved as only the coefficients of each polynomial equation must be stored. Using polynomial order between 4 and 8 allows limiting the fit error to under 0.01 %. Open-Short-Load calibration must be executed for each different measurement configuration as the introduction of different components on the signal path influences the high-frequency behavior.

Both DC calibration and Open-Short-Load calibration data are stored in specific data files using the *JSON* format. Those files are stored in the CalibrationData directory, located in the same directory as BIMMS.py. Those files are automatically loaded when calling the BIMMS object in the python library. Each file contains the ID of the board used during the calibration. During the loading of the files, the API checks that the ID in the files matches the ID of the board under use, ensuring consistency between the calibration files and the hardware.

Validation and performances

System characterization

The AD2, excitation front-end, and readout front-end have been characterized. Bandwidth, Total Harmonic Distortion plus Noise (THD + N), DC-offset, and power consumption are measured. Mismatch and crosstalk between the two inputs of the AD2 and the two-channel of the readout-front end are also evaluated. Output impedance is measured for the voltage source and the current source. All measurement plots are available in Supplementary Materials, in the document entitled *SuppMaterials.pdf*. This document is available on the Zenodo deposit. Results are summarized and discussed in this section.

The AD2 is measured using a loopback setup, i.e. the AD2 AWG output is connected to the AD2 scope inputs. Table 10 summarizes the measures. The −3dB bandwidth of the AD2 is above 10 MHz and high-frequency performances are mainly limited by the slew rate: the gain is about −1.8 dB at 10 MHz for 100 mVpp and 1 Vpp signals but drops at −2.5 dB when the AWG output signal is about 5Vpp. The slew-rate limitation is also noticeable on the THD + N at high-frequency. The mismatch between channel 1 and channel 2 of the AWG scope is negligible at low frequency and peaks at about 0.4 dB at 10 MHz. Crosstalk increases at higher frequencies and is due to capacitive coupling between channels. Regarding noise and harmonic distortion, 1 Vpp and 5Vpp input signals lead to similar THD + N results at low frequencies. The DC offset

Table 10
Measured performances of the AD2. [1]AWG output signal is 100 mVpp. [2]AWG output signal is 1 Vpp. [3]AWG output signal is 5 Vpp. [4]Unused channel is loaded with a 10 kΩ resistor.

Analog Discovery 2			
Bandwidth	Mismatch (1 kHz)	Mismatch (10 MHz)	Crosstalk[4] (1 kHz)
>10 MHz[1]	<0.05 dB[1]	0.4 dB[1]	−72 dB[1]
>10 MHz[2]	<0.05 dB[2]	0.4 dB[2]	−91 dB[2]
>10 MHz[3]	<0.05 dB[3]	0.4 dB[3]	−101 dB[3]
Crosstalk[4] (10 MHz)	THD + N (1 kHz)	THD + N (10 MHz)	DC Offset
−41 dB[1]	−38 dB[1]	−24 dB[1]	−4.3 mV[1]
−42 dB[2]	−55 dB[2]	−37 dB[2]	−4.5 mV[2]
−46 dB[3]	−58 dB[3]	−6dB[3]	−4.9 mV[3]

is measured between −4.0 and −5.0 mV. Additional measurements confirmed that the offset is being generated from the AWG part of the AD2. This offset can be easily canceled or reduced via software calibration.

Voltage readout measurements are summarized in Table 11. Measurements with various gain values and various input resistive loads are also available in Supplementary 2. A 10 MHz bandwidth is measured with a gain of up to 4 V/V (12 dB). The Gain-Bandwidth product limits the bandwidth under 10 MHz for higher gain: the bandwidth is about 5 MHz for a gain of 25 V/V (28 dB) and 2.2 MHz for a 100 V/V (40 dB) gain. One can note that the 2-stages topology improves the gain-bandwidth product in comparison to the 1-stage topology. Slew-rate limits the upper end of the bandwidth when the output voltage exceeds 1Vpp. Precision laser-trimmed resistors of the instrumentation amplifiers result in a mismatch under 0.08 dB at low frequencies. Mismatch increases with frequency due to parasitic capacitance. No significant differences are observed in crosstalk and THD + N in comparison with the AD2. The bias input current flowing into the input resistors generates a constant 1.2 mV input DC offset that can be canceled via software calibration. Power consumption is about 135mW per channel.

Transimpedance performances are summarized in Table 12. No stability issue is observed thanks to the compensation capacitor placed in the feedback loop of the TIA. High input loads limit the bandwidth as it forms an RC low pass filter with the input parasitic capacitance. Input current has no measurable effect on the bandwidth but improves the THD + N performances (Supplementary 3). These improvements on THD + N are neglectable at higher frequencies and are not impacted by the input load. In the differential configuration, the bandwidth is further reduced due to the additional parasitic capacitance brought by the symmetrical topology (Supplementary 3). THD + N and offset measured values are similar in both configurations. The power consumption of the TIA is about 110 mW.

The voltage driver is measured with a single-ended connection on an open load, on a 10kΩ load, and a 100Ω load. Results are summarized in Table 13 when the output voltage of the driver is set to 1 Vpp. Results for 100 mVpp and 5 Vpp output voltage are summarized in Supplementary 4. A gain of 0.8 dB (1.1 V/V) at 1 kHz is measured, as expected. The gain drops to −0.04 dB when the load is about 100Ω. This drop is due to the 10Ω output impedance of the voltage source, set by the output series resistors. Output impedance increases with frequency due to parasitic inductance. The measured impedance is about 26Ω at 10 MHz, thus has a moderate effect on impedance higher than 1kΩ. Bandwidth on an open load is about 7.9 MHz when the output is about 100 mVpp and is dropping to 7.5 MHz when the output is about 1 Vpp, and 7.3 MHz when the output is 5 Vpp (Supplementary 4). Those results suggest that the slew rate is limiting the high-frequency performances. Output load has a negligible influence on THD and THD + N. A large offset ranging between −31 mV and −36 mV is measured. This offset is likely to be caused by the unbalanced current flowing in the differential amplifier driver when connected to a load in a single-ended arrangement. This offset can be reduced via software calibration. In differential mode, the gain is measured at 6.8 dB (2.2 V/V). No significant differences are observed with the single-ended configuration regarding the bandwidth, THD + N, and power consumption (Supplementary 4). Output impedance is doubled due to the symmetrical topology. The measured DC offset is noticeably lower, being measured under 0.5 mV. Power consumption is about 253 mW.

Table 11
Measured performances of the Voltage Readout Channels. Gain is set to 1 V/V (0 dB). The unused channel is loaded with a 10 kΩ resistor. [1]IA output signal is 100 mVpp. [2]IA output signal is 1 Vpp. [3]IA output signal is 5 Vpp.

Voltage Readout			
Bandwidth	Mismatch (1 kHz)	Mismatch (10 MHz)	Crosstalk (1 kHz)
>10 MHz[1]	0.06 dB[1]	1.8 dB[1]	−65 dB[1]
>10 MHz[2]	0.05 dB[2]	1.6 dB[2]	−88 dB[2]
1.7 MHz[3]	0.07 dB[3]	0.75 dB[3]	−108 dB[3]
Crosstalk (10 MHz)	THD + N (1 kHz)	THD + N (10 MHz)	DC Offset
−42 dB[1]	−35 dB[1]	−17 dB[1]	1.2 mV[1]
−42 dB[2]	−54 dB[2]	−22 dB[2]	1.2 mV[1]
−38 dB[3]	−55 dB[3]	−22 dB[3]	1.3 mV[1]

Table 12
Measured performances of the TIA. Input current is 20 µApp. The input load is connected in a Single-Ended arrangement. (1)$R_L = 1k\Omega$. (2)$R_L = 10k\Omega$. (3)$R_L = 100k\Omega$.

Transimpedance Amplifier		
Bandwidth	Gain (1 kHz)	Gain (10 MHz)
>10 MHz(1)	40.0 dB(1)	39.9 dB(1)
3.0 MHz(2)	40.0 dB(2)	29.4 dB(2)
0.23 MHz(3)	40.0 dB(3)	10.2 dB(3)
THD + N (1 kHz)	THD + N (10 MHz)	DC Offset
−43 dB(1)	−23 dB(1)	2.1 mV(1)
−45 dB(2)	−34 dB(2)	1.9 mV(2)
−46 dB(3)	−37 dB(3)	2.0 mV(3)

Table 13
Measured performances of the Voltage Driver. The output voltage is set to 1Vpp and is connected to the load in a single-ended configuration. (1)Open load. (2)$R_L = 100\Omega$. (3)$R_L = 10k\Omega$.

Voltage Driver			
Bandwidth	Gain (1 kHz)	Gain (10 MHz)	Output Impedance (1 kHz)
7.5 MHz(1)	0.80 dB(1)	−6.4 dB(1)	10Ω
7.5 MHz(2)	0.80 dB(2)	−6.4 dB(2)	
7.2 MHz(3)	−0.04 dB(3)	−8.4 dB(3)	
Output Impedance (10 MHz)	THD + N (1 kHz)	THD + N (10 MHz)	DC Offset
26Ω	−63 dB(1)	−28 dB(1)	−33.4 mV(1)
	−63 dB(2)	−28 dB(2)	−32.4 mV(2)
	−63 dB(3)	−30 dB(3)	−32.1 mV(3)

Measurements of the current driver in a single-ended configuration with the low-gain gain setting are summarized in Table 14. The output impedance of the driver is notably affected by parasitic capacitances and thus is decreasing with frequency. Therefore, the bandwidth is limited in the high-frequency range with a higher load. This will result in a poorer SNR when performing wideband impedance spectroscopy on high load. About 10 % of bandwidth diminution is measured in the high-gain mode, but a smaller THD + N is measured due to the greater output current (Supplementary 5). In the differential configuration, a greater output impedance is measured, resulting in a bandwidth extension of about 50 % in comparison to the single-ended connection. Similar results are obtained regarding THD + N and offsets (Supplementary 5). The power consumption of the current source is about 341 mW.

Impedance spectroscopy accuracy on resistive loads

Four references 0.1 % precision resistors have been measured to test the accuracy of the device: 100Ω, 1kΩ, 10kΩ and 100kΩ. This range covers the impedance magnitude of the most implanted electrode categories [34]. Impedance is measured from 100Hz to 10MHz and in both galvanostatic configuration and in potentiostatic configuration. The excitation signal is about 100mVpp and 100µA in potentiostatic and galvanostatic configurations respectively. Both measurements use 32 sine periods per frequency point, with a 10ms settling time between each frequency step. The load is connected to the board in a DC-coupled 4-wires configuration. An Open-Short-Load calibration with a reference 1kΩ resistor is performed before the

Table 14
Measured performances of the Current Driver. Output current is set to 20 µApp. Gain is set in the lower range and load is connected in a single-ended arrangement. (1)$R_L = 100\Omega$, (3)$R_L = 1k\Omega$. (2)$R_L = 10k\Omega$.

Current Driver			
Bandwidth	Gain (1 kHz)	Gain (10 MHz)	Output Impedance (1 kHz)
>10 MHz(1)	−89.7 dB(1)	−90.9 dB(1)	> 1 MΩ
2 MHz(2)	−89.7 dB(2)	−104.3 dB(2)	
0.21 MHz(3)	−89.8 dB(3)	−120.0 dB(3)	
Output Impedance (10 MHz)	THD + N (1 kHz)	THD + N (10 MHz)	DC Offset
2.72**k**Ω	−23 dB(1)	−8dB(1)	0.21 µA(1)
	−41 dB(2)	−10 dB(2)	0.23 µA(2)
	−41 dB(3)	2 dB(3)	0.22 µA(3)

measurement. Un-calibrated results and calibrated results are compared to assess the performance of the calibration. Relative error (E_r) between the measured value (Z_{mes}) and the theoretical value (Z_{th}) is defined as follows [41]:

$$E_r = \frac{|Z_{th} - Z_{mes}|}{Z_{th}}.100$$

Data are plotted in Fig. 18.

As predicted by the characterization of the system, accuracy decreases with frequency (Fig. 18(a) and (b)). This decrease is further emphasized with a higher load. At 100kHz, the error is less than 1 % for the 100Ω, 1kΩ, and 10kΩ resistors, and about 5 % for the 100kΩ.

This error is about the same for both potentiostatic EIS and galvanostatic EIS. This error remains constant until 1MHz for both the 100Ω and the 1kΩ resistors. It reaches about 7 % for the 10kΩ in potentiostatic configuration and about 10% in the galvanostatic mode. At this frequency, the 100kΩ reference resistors measurement presents an unusable accuracy of about 70%. Accuracy at 10MHz is further degraded for every resistor.

Calibrated greatly improve accuracy and a better accuracy consistency through the entire measurement range (Fig. 18(c) and (d)). At 1MHz, the error remains under 2% for every resistor in both configurations, except for the 100kΩ resistor in the potentiostatic configuration reaching about 10 % error. At 10MHz, the error remains reasonably low for the 1kΩ and 10kΩ (<5 %), while reaching about 40 % for the 100Ω and about 50 % for the 100kΩ resistor in the potentiostatic mode and about 80 % for the galvanostatic EIS measurement.

Accuracy is greatly improved with a simple Open-Short-Load calibration, and the error is maintained low until 1MHz for each resistor, in both EIS configurations. Results are degraded at 10MHz, especially for the highest 100kΩ load. At this fre-

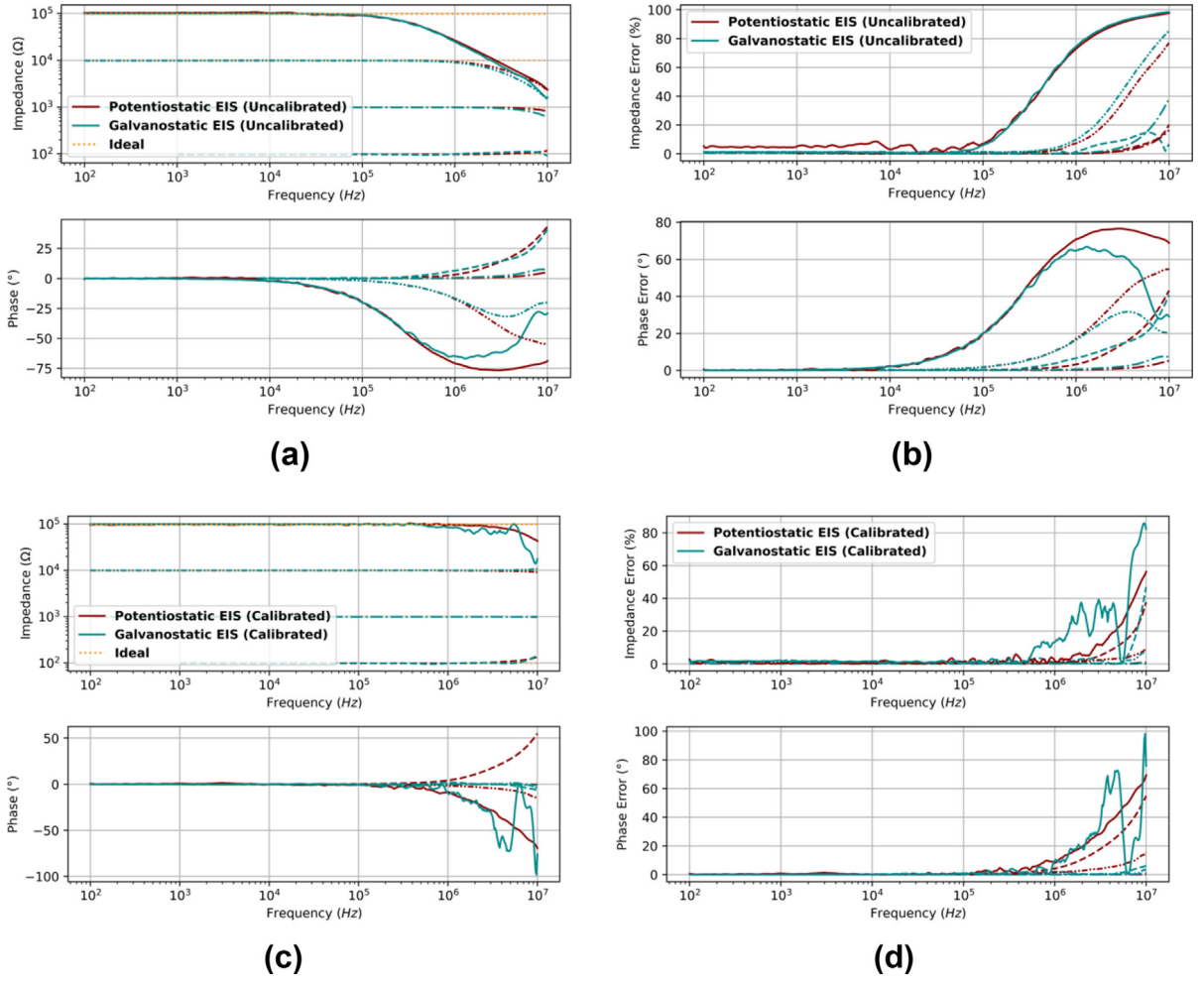

Fig. 18. Impedance measurement on reference resistors un-calibrated (a) with the associated error (b) and calibrated (c) with the associated error (d).

quency, the potentiostatic EIS is performing slightly better. It is worth noting that bio-impedance magnitude decreases with the frequency, and it is very unlikely to measure bio-impedance of this order of magnitude at this frequency [42]. It is also worth noting that we assumed that the used reference impedances are purely resistive, while they are also slightly capacitive and inductive.

Impedance spectroscopy SNR and sensitivity

Signal-to-Noise ratio of the impedance estimation is evaluated to assess the repeatability of the measurement. The methodology is based on the method described in [14]. A 0.1% 1kΩ resistor is used as a load. A 10µA current stimulus is applied in the galvanostatic EIS resulting in about 10mV across the load. A 10mV voltage stimulus is selected in the potentiostatic configuration for comparison between both EIS configurations. The influence of the IAs set gain is also assessed. Each SNR plot is evaluated from a set of 1000 measurements. Results are depicted in Fig. 19 for the galvanostatic EIS (a) and potentiostatic EIS (b). The galvanostatic configuration has an SNR of about 10 dB greater than the potentiostatic measurement. About 350mVpp is required from the AWG to set the output current to 10µA, in comparison to the 22mVpp required for an output of 10mV in the potentiostatic configuration. This order of magnitude is likely to explain the 10 dB difference between the two configurations. Adjusting the gain of the IAs has a considerable positive effect on the SNR. At 1kHz, more tham 20 dB of SNR improvement is measured in both configurations when the IAs gains are selected between 1 V/V and 50 V/V. As demonstrated previously, increasing the gain reduces the bandwidth and thus the SNR in the upper spectrum. Thus, at 10MHz the SNR improvement drops to about 10 dB for both potentiostatic EIS and galvanostatic EIS. A drop in SNR is observed near 1 MHz, caused by the switching frequency of the external power supply used. For very accurate

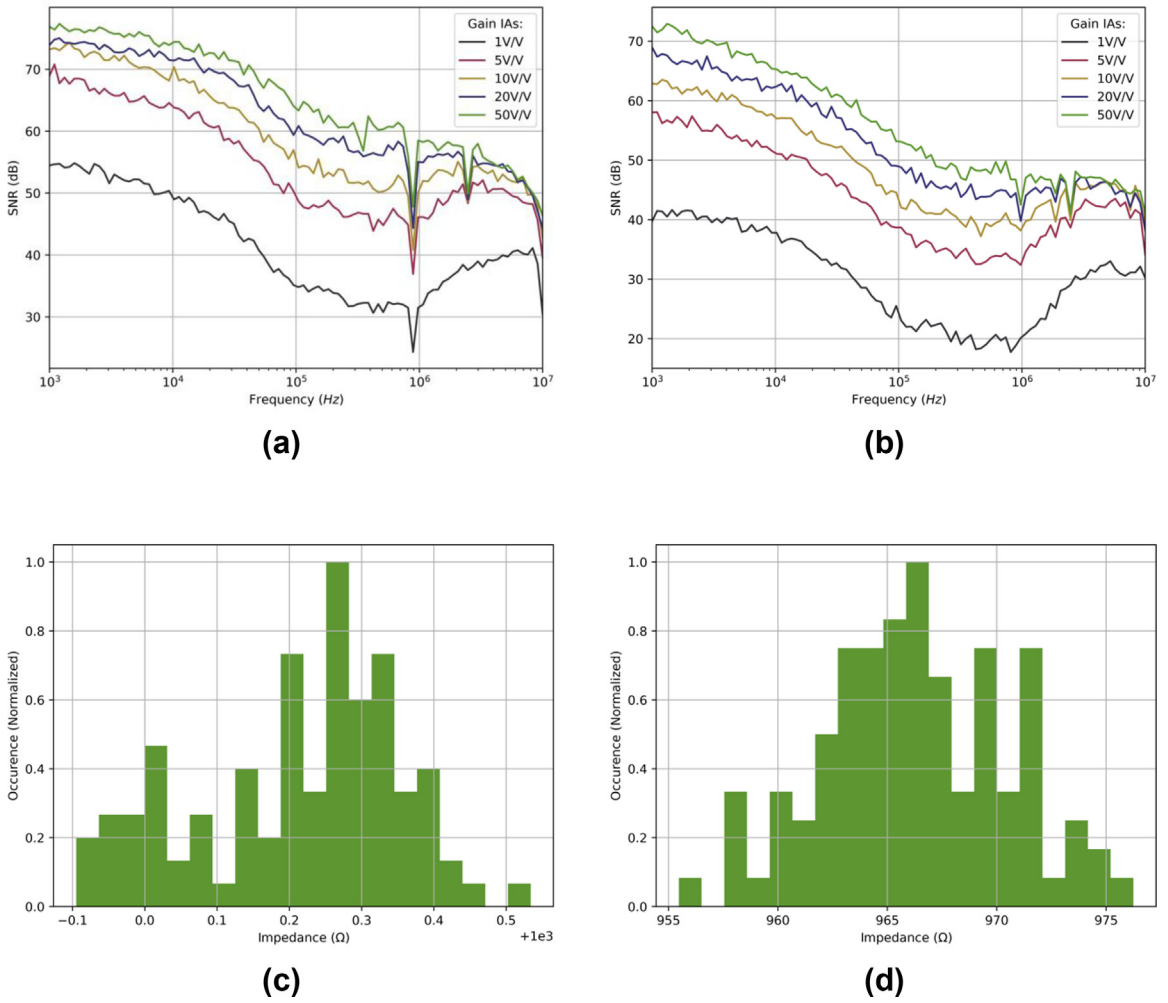

Fig. 19. SNR measurement on a 1kΩ load. (a) In the galvanostatic configuration. (b) In the potentiostatic configuration. Histogram of the measurements at 1 kHz (c) and 10 MHz (d) with the galvanostatic configuration and a gain set to 50 V/V.

measurement, this external power supply can be swapped with batteries. A histogram of the measurement at 1kHz in galvanostatic configuration with the gain set to 50V/V is presented in Fig. 19(c), and (d) for the measurement at 10MHz. About 600mΩ (0.06 %) of spread in the measurement is observed at 1kHz, and a spread of about 21Ω (2.1 %) at 10MHz.

Impedance spectroscopy accuracy on a complex load

To measure the accuracy of the system on a complex impedance, a measurement was performed on a test load (Fig. 20). This load presents an inflection point around 80kHz. Measurement parameters are identical to the previous setup, and both the galvanostatic EIS and potentiostatic EIS configurations are tested.

Ground-truth impedance is measured with a calibrated Keysight E4990A Impedance Analyzer (USA). Error is evaluated for un-calibrated and calibrated measurement, with the exact same calibration data as the previous setup. Data are depicted in Fig. 21. At 1MHz, the absolute magnitude error is about 1 % for the un-calibrated potentiostat EIS and about 1.5 % for the un-calibrated galvanostat EIS. The absolute phase error is 2° for both configurations. This error greatly increases at 10MHz, reaching about 30 % for the un-calibrated potentiostatic configuration, and about 55 % for the galvanostatic measurement. When the Open-Short-Load calibration is applied to the measurement, the relative impedance error remains under 0.3 % from 1kHz to 1MHz for both configurations. Phase error remains under 0.3° in this measurement range. At 10MHz, the magnitude error is about 2.4 % for the galvanostatic measurement and about 3.5 % for the potentiostatic measurement. The phase error is respectively 3° and 3.5°.

Measurements realized with the presented hardware are in a very good agreement with results obtained with a calibrated impedance analyzer. Without calibration, impedance measurement estimation is accurate until 1MHz for both the potentiostatic and galvanostatic measurement methods. This accuracy can be further extended up to 10MHz with the proposed calibration strategy.

Impedance spectroscopy on implantable electrodes

The instrument's ability to perform the analysis of bio-impedance was tested. The impedance of four different implantable electrodes designed for neural stimulation was measured: a CUFF electrode (NC-2.5-3-125umSS, MicroProbes, USA), a custom LIFE electrode [43], a TIME electrode (Neural Probe, Neuronexus, USA) and a custom deep-brain stimulation (DBS) electrode [44].

Each electrode was plunged into a saline solution of a conductivity of about 2 S/m. Impedance was evaluated from 10 Hz to 10 MHz using a potentiostatic measurement, with a measurement signal of 100 mV. Results are depicted in Fig. 22. Each electrode presents a distinguishable impedance footprint, and the α and the β dispersions are clearly visible. One can also note that electrode impedance is ruled by a non-integer behavior. No reaction or bubble accumulation was observed during the time experiment in which electrodes were plugged into the device, showing that the measurement does not induce charge accumulation which would compromise tissue safety for in-vitro or in-vivo experiments.

Instantaneous impedance spectroscopy with multisines excitation

There are a large variety of broadband signals used for instantaneous impedance spectroscopy. We choose a multisine excitation to demonstrate the possibility of instantaneous impedance spectroscopy with the presented system. A multisine signal consists of a sum of K sinewaves:

$$X_{MT} = \sum_{k=1}^{K} A_k sin(2\pi f_k t + \phi_k)$$

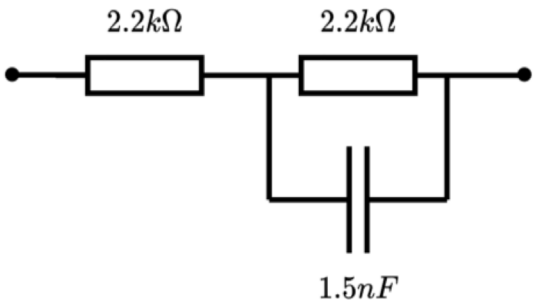

Fig. 20. Complex test load comprised of a 2.2kΩ resistor in parallel with a 1.5nF capacitor, in series with a second 2.2kΩ resistor. The accuracy of the component is not specified as measurement results are compared to calibrated commercially available impedance measurement devices.

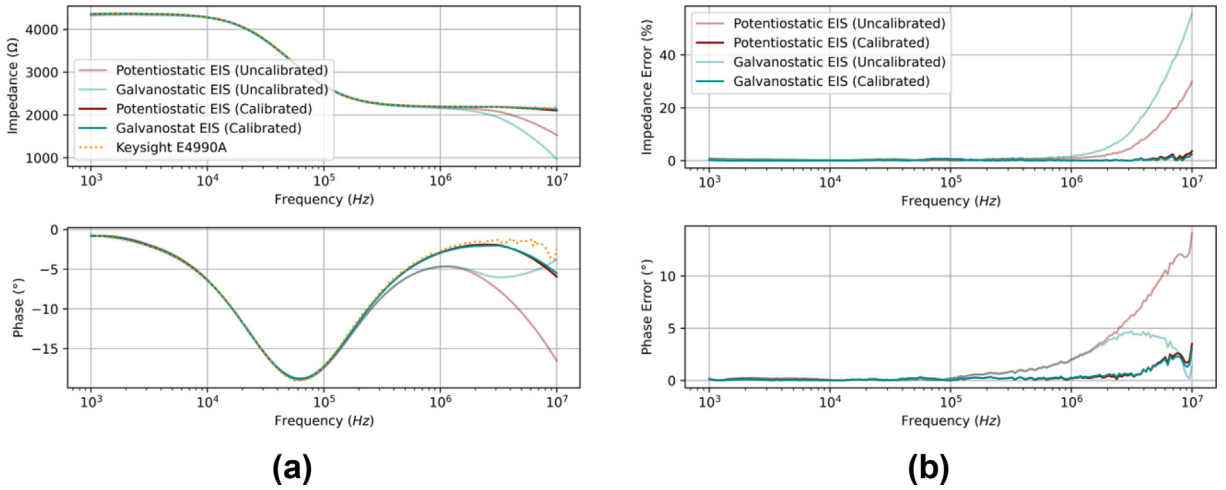

Fig. 21. Complex test load measured with the presented hardware (a), and error when compared to a calibrated Keysight E4990A (b).

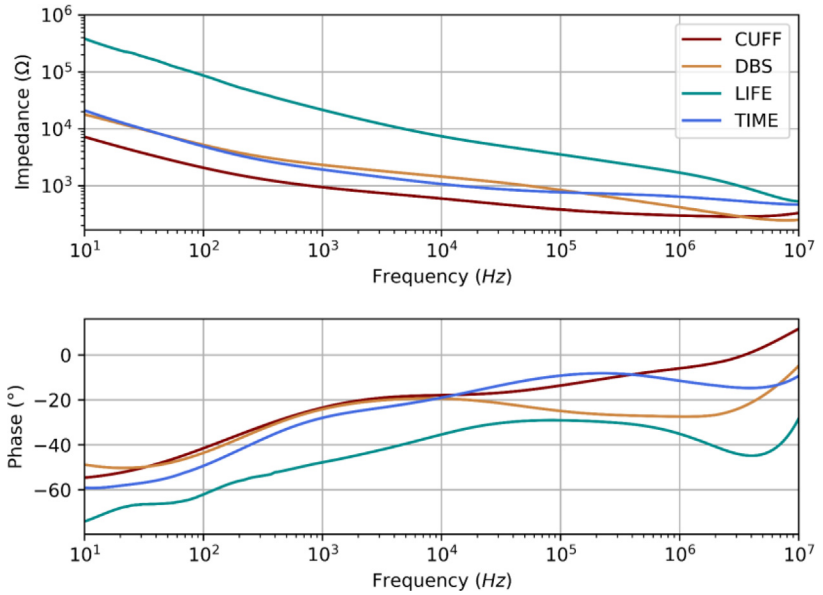

Fig. 22. Impedance measurement realized with the presented hardware, on implanted electrodes for neural stimulation.

The frequency, amplitude, and phase of each sinusoid can be adjusted separately, making this signal flexible. The multisine used in this experiment is composed of 20 tones between 2 kHz and 2 MHz, spaced with an odd-log distribution. The odd-log distribution reduces the error introduced by harmonics generated by nonlinearities [14]. The relative phase ϕ_k of each tone is adjusted to reduce the crest factor of the multitone. Ultimately, the signal amplitude is scaled to obtain an amplitude of 800 mVpp. The excitation signal is depicted in Fig. 23(a).

This signal is applied to the load presented in Fig. 20 in the potentiostatic configuration. Waveform generation and acquisition are synchronized using the internal trigger of the AD2 platform. The resulting current and voltage on the load are digitized at $f_s = 20$Mps on $N = 8192$ samples. Both signals are demodulated at each frequency point by computing a Discrete Time Fourier Transform (DTFT). The instantaneous impedance spectrum is then estimated by computing the ratio of the current and the voltage in the frequency domain. The resulting magnitude and phase are depicted in Fig. 23(b) and compared to a reference measurement with a calibrated Keysight E4990A impedance analyzer. The multisine measurement matches very well the reference measurement. A maximum relative error of 1.5 % is observed on the magnitude and about 1° on the phase estimation. In comparison to the traditional swept sine method, this estimation is slightly less accurate. However, this measurement took only 0.5 ms instead of a couple of seconds for the swept sine method.

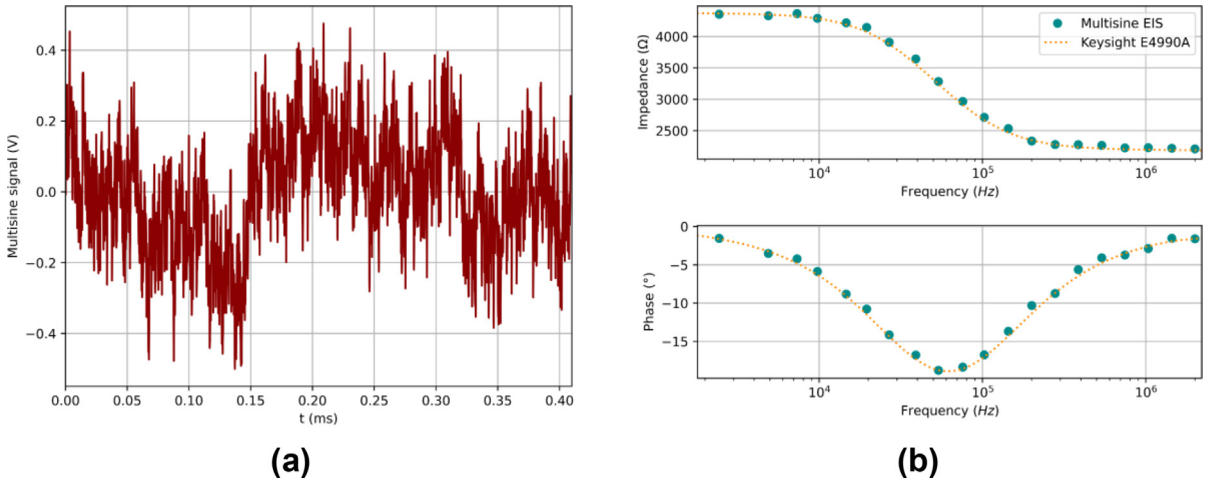

Fig. 23. Generated multisine signal (a) and resulting estimated instantaneous impedance spectrum (b).

Cyclic voltammetry on implantable electrodes

In this section, we demonstrate the possibility of performing cyclic voltammetry on implantable electrodes. A full characterization as well as additional details of the proposed circuit can be found in Ref. [33] and in Ref. [45]. Cyclic voltammetry is performed on a LIFE electrode [43] and a CUFF electrode (NC-2.5-3-125umSS, MicroProbes, USA). Both electrodes are plunged into a bath of saline solution of a conductivity of about 2 S/m. Cyclic voltammetry was performed from −3V to 3 V, with a scan rate of 50 mV/s, 100 mV/s, 200 mV/s, 500 mV/s, and 5000 mV/s.

On the current versus voltage plot of the LIFE electrode (Fig. 24(a)), threshold voltages at which a reaction with water appears are clearly visible. Beyond these thresholds, electrolysis of water results in the formation of oxygen or hydrogen gas. Electrolysis can damage the electrode and the formed gas can damage the surrounding tissues. The voltage region between those two thresholds is called the "water window", and it is usually considered as the safe region for electrical stimulation [21]. The safe region for stimulating with LIFE electrodes is between −1V and +2 V. The safe region is wider for CUFF electrodes (Fig. 24(b)), from about −2V to +3 V. It is worth noting that those thresholds are also related to the scan rate of the voltage span, especially for the CUFF electrode.

Monitoring EIS on an ex-vivo calf brain

Impedance spectroscopy has proven to be a useful tool for monitoring the electrode-tissue interface of implanted DBS electrodes [5,46,47]. Here we demonstrate the feasibility of EIS on an isolated ex-vivo calf brain implanted with DBS electrodes. A custom DBS electrode [44] was inserted in the left frontal lobe and the impedance was evaluated from 10 Hz to

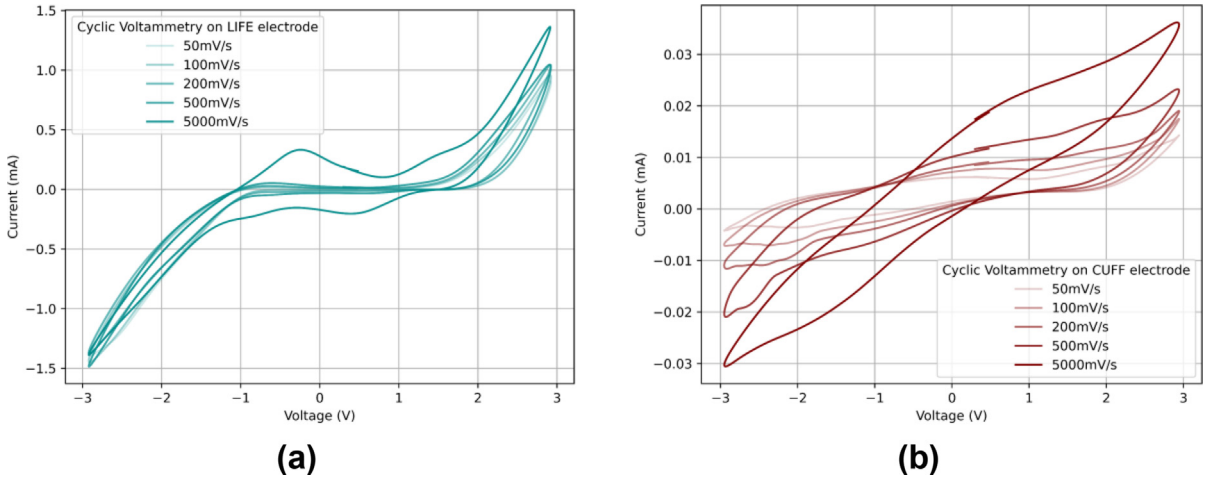

Fig. 24. (a) Cyclic voltammetry on LIFE electrode. (b) Cyclic voltammetry on CUFF electrode.

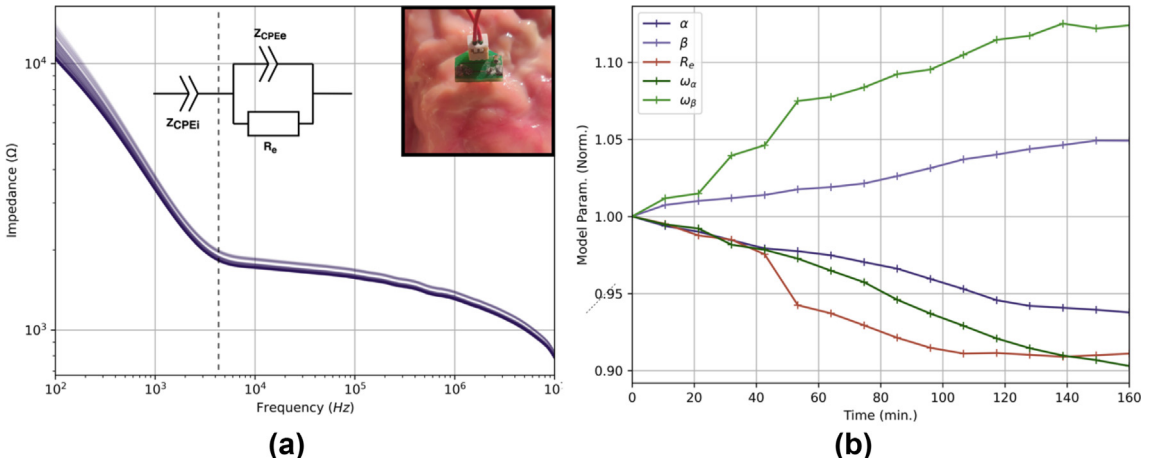

Fig. 25. (a) Impedance of the DBS electrode measured every 10 min. The darker the trace is the later the measurement was performed. (b) Fitted parameters are normalized with values at $t = 0$ and are plotted over time.

10 MHz using a potentiostatic measurement, with a measurement signal of 100 mV. At $t = 0$, the brain was placed inside a tank half-filled with a saline solution with a conductivity of about 2 S/m. The brain was left soaking in the solution for 160 min while impedance was monitored every 10 min. The measurement impedance spectrums are shown in Fig. 25(a).

The measured impedance of the DBS electrode decreases while the tissues are absorbing the highly conductive solution. A drop of 26.8 % in impedance is observed at 100 Hz between the first and last measurements. The drop is about 7.7 % at 10 kHz and about 4.3 % at 1 MHz. Measurements were fitted with an impedance model using constant phase elements [9] (Fig. 25a):

$$Z_{DBS} = Z_{CPE_i} + R_e//Z_{CPE_e} = \left(\frac{\omega_\alpha}{j\omega}\right)^\alpha + \frac{R_e}{1 + R_e\left(\frac{\omega_\beta}{j\omega}\right)^\beta}$$

Parameters of the model were estimated using a non-linear least square estimator and are plotted over time Fig. 25b. The impedance variation over time is well captured with the model, with at least 5 % of variation in the model parameters within the measurement set. Individual analysis of the evolution of each parameter enables a better understating of the underlying mechanisms. For example, the decrease of R_e, modeling the extracellular resistivity, is very well explained by the increase in conductivity due to the absorption of the saline solution. Also, the abrupt shift in impedance measured at $t = 50$ is very well reflected on R_e. No reaction or bubble accumulation was observed during the time of the experiment, and no lesions around the area of electrode insertion were noticed after the experiment.

Conclusion

The proposed BIMMS platform can perform accurate spectroscopy measurements as well as cyclic voltammetry. Performances are summarized in Table 15. A large variety of measurement configurations is possible and automatically handled in software. The low cost and compact form factor in comparison to commercially available systems make it well suited for lab experiments as well as a useful tool for teaching. Scripting capability offers the possibility of long-term autonomous experiments. In combination with a low-cost Raspberry Pi4 mini-computer, remote measurements are possible when direct connection is not favorable. A large number of available IOs offer the possibility of connecting the platform to extension boards, such as an electrode multiplexing board.

From the hardware point of view, the presented design is currently limited by the possibilities offered by the AD2 platform. Despite offering a wide range of possibilities, the lack of access to the FPGA internal functionalities limits the possibilities of time-sensitive applications, such as real-time fast impedance spectroscopy. Replacing the AD2 with a custom data acquisition/generation circuitry would greatly improve the possibilities of the platform but at the cost of long-time development and prototyping. The system could be made more compact by using smaller passives and with a tighter design but would make the assembly of the board more challenging, and possibly more expensive. Components on both sides of the PCB would also help reduce the size of the design. Replacing the electromechanical relays with solid-state switches would also greatly help save space.

The currently provided python library implements all the basic functionalities for using BIMMS. The proposed Graphical User Interface enables an easy use even not knowing about the Python language. Some purely software functionalities are currently being implemented, such as offset cancellation, auto-gain control, current and voltage limitation, saturation detection and so on. All those improvements will be progressively added to the BIMMS library and will be available as an updated

Table 15
Overall performances of the system. [1]Measured on loads comprised between 100 Ω and 10 kΩ. [2]Measured on loads comprised between 10 kΩ and 100 kΩ. [3]Measured at 1 kHz on a 1 kΩ resistor. [4]Measured at 10 MHz on a 1 kΩ resistor.

Bandwidth	Error (<1 MHz)	Error (>1 MHz)	Sensitivity
DC to 10 MHz	<2%[1] <10 %[2]	<10 %[1] <50 %[2]	600mΩ[3] 21Ω[4]
Current Range	Voltage Range	Power Consumption	Cost
10**µA**–2.4 mA	10 mV–8 V	<1 W	$650

version on the dedicated git depository (https://github.com/fkolbl/BIMMS for the development version) and installable through the Pypi platform. Any hardware update or daughter board will also be made available on the git repository.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.ohx.2022.e00387.

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