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OPEN Temperature dependence of **Coulomb oscillations in a few-layer two-dimensional WS2 quantum dot**

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Standard semiconductor fabrication techniques are used to fabricate a quantum dot (QD) made of WS2, where Coulomb oscillations were found. The full-width-at-half-maximum of the Coulomb peaks increases linearly with temperature while the height of the peaks remains almost independent of temperature, which is consistent with standard semiconductor QD theory. Unlike graphene etched QDs, where Coulomb peaks belonging to the same QD can have different temperature dependences, these results indicate the absence of the disordered confining potential. This difference in the potential-forming mechanism between graphene etched QDs and WS2 QDs may be the reason for the larger potential fluctuation found in graphene QDs.

After demonstrating a variety of electronic applications on graphene¹, graphene-like two-dimensional layered materials have attracted the increasing attention of researchers because of their unique properties[2,](#page-5-1)[3.](#page-5-2) Compared with traditional semiconducting materials, two-dimensional layered materials have the advantages of inherent flexibility and an atomically-thin geometry. Moreover, because their interfaces are free of dangling bonds, two-dimensional layered materials can easily be integrated with various substrates. They can also be fabricated in complex sandwiched structures⁴ or even suspended to avoid the influence of the substrate^{[5](#page-5-4)}.

Transition metal dichalcogenides (TMDCs) are considered one of the most promising two-dimensional post-graphene materials for electronics owing to the presence of a band gap ranging from 1 to 2 eV^{6,[7](#page-5-6)}. This band gap results in high on–off ratios in classical electronic devices made out of TMDC[s8](#page-5-7). A variety of electronic devices have been demonstrated on TMDCs, such as field-effect transistors⁹⁻¹³, heterostruc-ture junctions^{14,[15](#page-5-10)} and photodetectors^{16,17}.

Meanwhile, from the aspect of quantum nano-devices, TMDCs have advantages over graphene as well. Unlike etched quantum dots (QDs) made on semimetallic graphene^{[18,](#page-5-13)[19](#page-5-14)}, semiconducting TMDCs have a band gap large enough to form a QD using the electric field. This QD decreases the influence of the edge states, which are a major aspect limiting the performance of graphene nano-devices $20,21$ $20,21$. Recently, theoretical predictions using QDs on TMDCs as qubits have been proposed²², and experimental studies of QDs on WSe₂ have been performed as well²³. However, a detailed study of QDs in TMDCs, and especially the behavior of the Coulomb oscillations, is still not yet available.

Tungsten disulfide (WS_2) is a typical semiconducting TMDC material that has a direct band gap of 2.0 eV in a monolayer and an indirect band gap of 1.4 eV in the bulk crystal⁶. Theoretical models predict that WS₂ should have the highest mobility among the semiconducting TMDCs because of the reduced effective mass²⁴. Several previous studies have shown that the typical carrier mobility of WS₂ is in the range of 20-300 cm²/(V·s)^{[11,](#page-5-20)[25](#page-5-21)[,26](#page-5-22)}.

In this letter, we use standard semiconductor fabrication techniques to fabricate a QD made of WS₂, where Coulomb oscillations are observed. The temperature dependence of the Coulomb peaks is

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Figure 1. Device characterization. (a) Scanning electron microscope image of the WS₂ quantum dot studied in this work. The WS₂ flake is highlighted by the white dotted line, and the four top gates are labeled as MG, LB, PG, RB. The scale bar represents 5μm. (**b**) Three-dimensional schematic view of the device. (**c**) Schematic cross-section of the device. The few-layer WS_2 is deposited on a heavily-doped silicon substrate covered with 100 nm of $SiO₂$. The WS₂ flake is separated from the four top gates (Ti/Au) by 100 nm of ALDgrown Al_2O_3 . Two metal gates (Pd/Au) are connected to the flake and used as source-drain contacts.

investigated, showing that the behavior of Coulomb peaks is in agreement with standard semiconductor QD theory: the full-width-at-half-maximum (FWHM) of the Coulomb peaks increase linearly while the peak height remain almost unchanged when increasing the temperature. The Coulomb oscillations of the QD on WS₂ are different from those of the graphene etched QDs, wherein Coulomb peaks belonging to the same QD can have different temperature dependences. Among these Coulomb peaks, only portions can be understood by the standard semiconductor QD theory, while most of the Coulomb peaks of graphene etched QDs become broader and higher with increasing temperature. Our results indicate the absence of the disordered confining potential, showing a difference between the potential-forming mechanisms of graphene etched QDs and WS_2 QDs, which may be the reason for the larger potential fluctuation found in graphene QDs. Meanwhile, the results may be useful for the fabrication of QDs on graphene-like two-dimensional layered materials.

Results

As shown in Fig. $1(a)$, the few-layer WS, flake used in the experiment has an area of approximately $3 \times 5 \mu m^2$, which is highlighted by the white dotted line in the scanning electron microscope image. A schematic depiction of the device is shown in [Fig. 1\(b\)](#page-1-0). The heavily doped silicon substrate worked as the back gate, which was isolated from the WS_2 by a 100 nm-thick layer of SiO_2 . Here, we used Pd/Au for source-drain contacts ("source" and "drain" in [Fig. 1\(b\)](#page-1-0)) of the WS₂ flake. On the Al_2O_3 insulating layer, four split electrodes ("top gates" in [Fig. 1\(b\)](#page-1-0)) were fabricated using Ti and Au, corresponding to Middle Gate (MG), Left Barrier (LB), Plunger Gate (PG) and Right Barrier (RB) in [Fig. 1\(a\)](#page-1-0). The voltage applied to MG, LB, and RB is mainly to form the confining potential to obtain quantum dot. The effect of PG is not only for confining the dot, but also for tuning the energy levels in the quantum dot.

[Figure 1\(c\)](#page-1-0) shows the schematic cross-section of the device. The experiment was performed in a He3 refrigerator at a base temperature of 240mK. We used the standard lock-in method to probe the electronic signals.

First, we applied a dc voltage to the back gate to accumulate carriers in the WS_2 device. The source-drain current is obtained while sweeping the back gate voltage V_{BG} . As shown in [Fig. 2\(a\)](#page-2-0), the characteristic behavior of an n-doped semiconductor is observed, that when tuning the back gate voltage to be more positive, the current becomes nonzero around $V_{BG} = 5V$. Note that the puddles may be formed in our device since some current oscillations are already evident. After we apply a dc voltage of −2V to the top gates, the current as a function of the dc bias voltage at varying back gate voltages is measured. As shown in Fig. 2(b), over 20 consecutive Coulomb diamonds are observed from V_{BG} = 13.2–14V, indicating the formation of a QD. The fact that the Coulomb diamonds are symmetric suggests equivalent tunnel

Figure 2. Transport measurement of the device. (a) Source-drain current flows through the WS_2 **devices** as a function of back gate voltage, V_{BG} , showing the characteristic behavior of an n-doped semiconductor. (**b**) Over 20 consecutive Coulomb diamonds of a WS₂ quantum dot. Symmetric Coulomb diamonds suggests equivalent tunnel coupling to the source and drain leads. All of the top gates have an applied dc voltage of −2V. (**c**) The relative peak position as a function of peak number p for the first 10 peaks of (**b**). The red dashed line is the linear fit for the data (red open circles). (**d**) A Coulomb diamond measured as a function of the plunger gate voltage $V_{P\text{G}}$. Two black dotted lines mark the two sides of the diamond.

coupling to the source and drain leads. All of the Coulomb diamonds appear to have a similar charging energy E_C of approximately 0.75 meV in logarithmic plotting (Fig. S1 in the supplemental material).

We also investigate the peak spacing of the Coulomb peaks. [Figure 2\(c\)](#page-2-0) shows the relative peak position as a function of peak number p, for the first 10 peaks of [Fig. 2\(b\)](#page-2-0). The relative peak position can be expressed as $V(p)-V_0$, where $V(p)$ is the voltage of the peak p and V_0 is the voltage of the first peak. The data was fitted by a linear function, as shown by red dashed line, suggesting a constant peak spacing of 36.6mV. Using the E_C and peak spacing ΔV , the lever arm of the back gate α_{BG} is calculated to be 0.0205 eV/V. It is also estimated that the average QD radius is 430 nm using the relationship $E_C = e^2/d$ $(8\varepsilon_0\varepsilon_r r)^{27}$, where $\varepsilon_r = 7$ is the relative permittivity of few-layer WS₂²⁸ and *r* is the radius of the QD. Note that because the estimated dot size is comparable to the thickness of the insulating $SiO₂$ layer, the isolated disk approximation should change to a parallel plate approximation. Thus, the result of the estimated QD size should be considered as an upper limit, which is comparable to our geometric design of the top gates.

Further, to confirm that the QD is formed because of the presence of top gates, we use a plunger gate (PG) to tune the energy levels in the QD. As shown in [Fig. 2\(d\),](#page-2-0) a Coulomb diamond is observed. These results are similar to those obtained in previous experiments on $WSe₂²³$. There are two reasons why we don't have a complete Coulomb diamond in [Fig. 2\(d\)](#page-2-0): (1) The thickness of the insulating layer Al_2O_3 is as larger as 100 nm. This will result in a relatively small lever arm α of the top gate, since $\alpha \sim \epsilon/d$, where ε is the relative dielectric constant of the insulating layer, and d is the thickness of the insulating layer. (2) Due to the limitation of ALD-growth quality, ε may also be smaller than theoretical expectation, resulting in a smaller lever arm as well. Moreover, due to the growth quality limitation, applying high voltage to top gates may lead to current leakage in the insulating layer (as shown in [Fig. 2\(d\)\)](#page-2-0). We only applied the voltage to show a dependence on V_{PG} . In fact, comparing the resonant tunneling point in [Fig. 2\(b\)](#page-2-0) to that in [Fig. 2\(d\),](#page-2-0) we found a current difference of about ~10pA, which means there may be leakage between the source and the drain. We think the leakage is caused by the insulating layer of $\mathrm{Al}_2\mathrm{O}_3$. Using the leak current ~10pA, divided by the voltage applied on the top gates, we can estimate that the resistance of the Al₂O₃ layer is about $5 \times 10^{11} \Omega$. Although the resistance is large, it may cause a leakage of several pA, which can be measured in the experiment.

Next, we investigate the temperature dependence of the Coulomb peak to achieve a better understanding of the Coulomb oscillations in WS_2 . According to the standard theory of semiconductor $QDs²⁹$ $QDs²⁹$ $QDs²⁹$, the line shape of the Coulomb peak in the weak coupling regime manifests in different forms for different temperature regimes, such that

Figure 3. Temperature dependence of the Coulomb peaks. (**a**) A typical Coulomb peak of the QD on WS₂ fitted with a Lorentzian (red solid line) and $cosh(x)$ (blue solid line). (Inset) Same figure plotted in the logarithmic scale. (**b**) The FWHM (black open squares) and the peak height (blue open circles) of a typical Coulomb peak as a function of temperature. The dashed lines are linear fits. (**c**) The FWHM of three Coulomb peaks (labeled as peaks 1, 2, and 3) as a function of temperature. The dashed lines show the linear fits for each peak, linearly increasing with temperature. (**d**) The peak height of the three Coulomb peaks in (**c**) (labeled as peaks 1, 2, and 3) as a function of temperature. The peak heights are almost independent of temperature. (**e**) Normalized Coulomb peak height as a function of temperature. The red (blue) dashed line shows the temperature dependence of the peak height obtained from the QD (impurity trap) on WS_2 , which lies in the classical (quantum) regime. The green solid line indicates the temperature dependence of a common peak height obtained from a graphene etched QD taken from ref. [21](#page-5-16).

$$
G/G_{max} = \frac{1}{2} \cosh^{-2} \left(\frac{\delta}{2.5 k_B T} \right) \text{ if } h \Gamma, \Delta E \ll k_B T \ll e^2 / C, \text{ (classical regime)} \tag{1}
$$

$$
G/G_{max} = \frac{\Delta E}{4k_B T} \cosh^{-2} \left(\frac{\delta}{2k_B T}\right) \text{ if } h\Gamma \ll k_B T \ll \Delta E, \, e^2/C, \, \text{(quantum regime)}\tag{2}
$$

where *G* is the conductance of the Coulomb peak, *Gmax* is the maximum conductance at high temperature, Γ is the tunneling rate through the barriers connecting the QD and the reservoirs, $δ$ is the distance to the peak center in terms of energy, ΔE is the average level spacing, and $e²/C$ is the charging energy. If the QD is in the strong coupling regime, the formula that describes the line shape of the peak changes to the well-known Breit–Wigner formula,

$$
G = \frac{2e^2}{h} \frac{(h\Gamma)^2}{(h\Gamma)^2 + \delta^2} \text{ if } T = 0, e^2/C \ll h\Gamma, \Delta E. \tag{3}
$$

The Coulomb peaks in the regime $k_B T \sim h\Gamma$ have the Lorentzian lineshape of Eq. (3), where k_B is Boltzmann's constant and T is the temperature²⁷.

[Figure 3\(a\)](#page-3-0) shows a typical Coulomb peak from the QD on WS_2 , where the data (blue open squares) are fitted using both a Lorentzian curve (red solid line) and a cosh(*x*) curve (blue solid line). The peak is also plotted in the logarithmic scale ([Fig. 3\(a\)](#page-3-0) inset). The data decrease linearly at the tails of the peak, showing a deviation from the Lorentzian line shape. Note that only when $k_B T \ge h\Gamma$ does the slower decay of the Lorentzian tails become clearly visibl[e27](#page-5-23)[,30](#page-5-26). According to the fitting curve, it is estimated that *h*Γ of the QD is not dominated compared to the temperature.

To give a rough estimation of the order of magnitude, we can estimate the average single particle energy of the QD to be $\Delta E = 1.4 \mu eV$ using $\Delta E = \hbar^2 / m^2 r^2$, where *r* is the radius of the QD and $m^* = 0.3 m_e$ is the effective mass in WS_2^{22} . Because the temperature varies in the range 290 mK to 1K, it can be estimated that $k_B T \sim 50 \,\mu\text{eV}$, which suggests that the QD is in the classical regime ($\Delta E \ll k_B T$). We fit the Coulomb peak at different temperatures using Eq. (1). [Figure 3\(b\)](#page-3-0) plots the FWHM (black open squares) and height (blue open circles) of a typical Coulomb peak as a function of temperature, as well as the linear fits (dashed lines) of the data. The FWHM of the Coulomb peak increases linearly with the temperature while the peak height remains almost constant.

Three typical Coulomb peaks in the range of $V_{BG} = 12.32-12.43V$ are also tracked in the same way (labeled as peaks 1, 2, and 3). The FWHM of these peaks as a function of the temperature is shown in [Fig. 3\(c\)](#page-3-0). The FWHM decreases linearly while lowering the temperature. Using the linear fitting slopes and the previously obtained lever arm, we can estimate the FWHM to be $(1.41 \pm 0.07)k_BT$.

Using Eq. (1), the FWHM is calculated to be 4.4 k_{B} T in the classical regime, which is almost three times the value measured in the experiment. The difference in slope between the theory and experiment can be caused by many reasons, such as the tunneling rate broadening and larger effective electron tem-perature^{[27](#page-5-23)}. The deviation from the theoretical expectation suggests that the assumption that the effect of hΓ can be neglected may not be appropriate. There may also be other reasons which need to be further studied.

[Figure 3\(d\)](#page-3-0) shows the Coulomb peak heights of the three peaks as a function of the temperature, exhibiting a behavior that is almost independent of the temperature. This is the signature of Coulomb peaks in the classical regime²⁹. Moreover, when changing to the region where a large bias voltage, V_{SD} , is applied, another series of Coulomb diamonds with a charging energy E_C larger than 30 meV emerge (Fig. S2 in the supplemental material). Because this series of Coulomb peaks has a much larger E_C and is nearly independent of the gate voltages applied on the top gates, it is considered to be the result of an impurity trap. The effective QD radius of this area is estimated to be 10nm, resulting in the single particle energy of ΔE= 2.6 meV. Compared to $k_B T \sim 50 \mu$ eV, Coulomb oscillations of the impurity trap lies in the quantum regime ($k_B T \ll \Delta E$). Similarly, we investigate the temperature dependence of two typical peaks of the impurity trap (Fig. S3 in the supplemental material). The height of the Coulomb peak decrease linearly with increasing temperature, which is the signature of a Coulomb peak in the quantum resonant tunneling regime²⁹.

[Figure 3\(e\)](#page-3-0) shows the normalized peak heights as a function of temperature for Coulomb peaks obtained from the QD (red dashed line) and the impurity trap (blue dashed line) on WS_2 . The peak height of the impurity trap (quantum regime) has a much larger slope that decreases with temperature, which is consistent with theoretical predictions²⁹. Meanwhile, the nonzero slope of the QD (classical regime) may be caused by the influence of the impurity in WS_2 flake. However, although the impurity trap exists in our device, the behavior of the Coulomb peaks is still in agreement with standard semiconductor QD theory. Note that these results are different from those found with graphene etched QDs, wherein Coulomb peaks belonging to the same QD are able to have different temperature dependences. Among these Coulomb peaks, only portions can be understood by the standard semiconductor the-ory, while most of the Coulomb peaks becoming broader and higher with increasing temperature^{21,[31](#page-5-27)}. The temperature dependence of the normalized peak height of graphene etched QDs is also plotted in [Fig. 3\(e\)](#page-3-0) for contrast, using a green solid line (The data is from ref. [21.](#page-5-16)).

Discussion

The anomalous behavior of Coulomb peaks in a graphene etched QD is widely considered to be the result of a disordered confining potential³² since the edge states are formed in the narrow constrictions connecting the QD and the reservoirs. Moreover, this disordered confining potential may limit the performance of the graphene etched QD because low-frequency noise experiments on graphene QDs exhibit a larger fluctuation of potential²¹. Our results, which are consistent with standard semiconductor theory, suggest the existence of an energy-independent tunneling barrier, which is different from the situation existing in graphene QDs. The difference, which relates to the edge states, in the barrier-forming mechanisms of an graphene etched QD and a WS_2 QD, may contribute to the larger noise level found in graphene QDs. Meanwhile, the designed device structure used in our experiment, where a disordered confining potential is absent, may be useful for the fabrication of QDs on graphene-like two-dimensional layered materials.

In summary, we use standard semiconductor fabrication techniques to fabricate a QD on $WS₂$, which is one of the TMDCs materials. The FWHM of the Coulomb peaks increases linearly with temperature while the height of the peaks remains nearly independent of temperature, showing that the behavior of the Coulomb oscillations is consistent with standard semiconductor QD theory. Unlike etched graphene QDs, where Coulomb peaks belonging to the same QD can have different temperature dependences, our results indicate the absence of a disordered confining potential. This difference in the potential-forming mechanisms of graphene etched QDs and $WS₂$ QDs may be the reason for the larger potential fluctuation found in graphene QDs. Meanwhile, the designed device structure used in our experiment, which is isolated from the edge states, illustrates the fabrication of QDs on graphene-like two-dimensional layered materials.

Methods

The WS₂ flakes were produced by mechanically cleaving a bulk WS₂ crystal using the "Scotch tape" method onto a highly-doped silicon substrate covered by 100 nm of $SiO₂$, similar to the method used to fabricate graphene devices^{19[,31](#page-5-27)}. Few-layer flakes were selected using an optical microscope. The flake of the device studied in the experiment has a thickness of approximately 7–10 layers according to our experience. The source-drain electrodes were formed using a standard electron beam lithography (EBL) process followed by electron beam evaporation to deposit 10nm of Pd and 90nm of Au. After a standard lift-off process, an atomic layer deposition (ALD) technique was used to make a 100nm-thick insulating $A₁, O₃$ layer. Then another EBL step was subsequently applied to form a pattern of four split top gates. Using electron beam evaporation, 5nm of Ti and 45nm of Au was deposited to fabricate the top gates. After the Al_2O_3 layer covering the source-drain contacts was etched, the device was bonded to the chip carrier and was ready for measurements.

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Author Contributions

X.-X.S. fabricated the samples. X.-X.S., J.Y. and D.L. performed the measurements. X.-X.S., Z.-Z.Z., H.- O.L., G.C. and M.X. provided theoretical support. Data are analyzed by X.X.S., J.Y. and Z.-Z.Z. The manuscript is prepared by X.-X.S., Z.-Z.Z. and G.-P.G. G.-P.G. supervised the project. All authors contributed in discussing the results and commented on the manuscript.

Additional Information

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