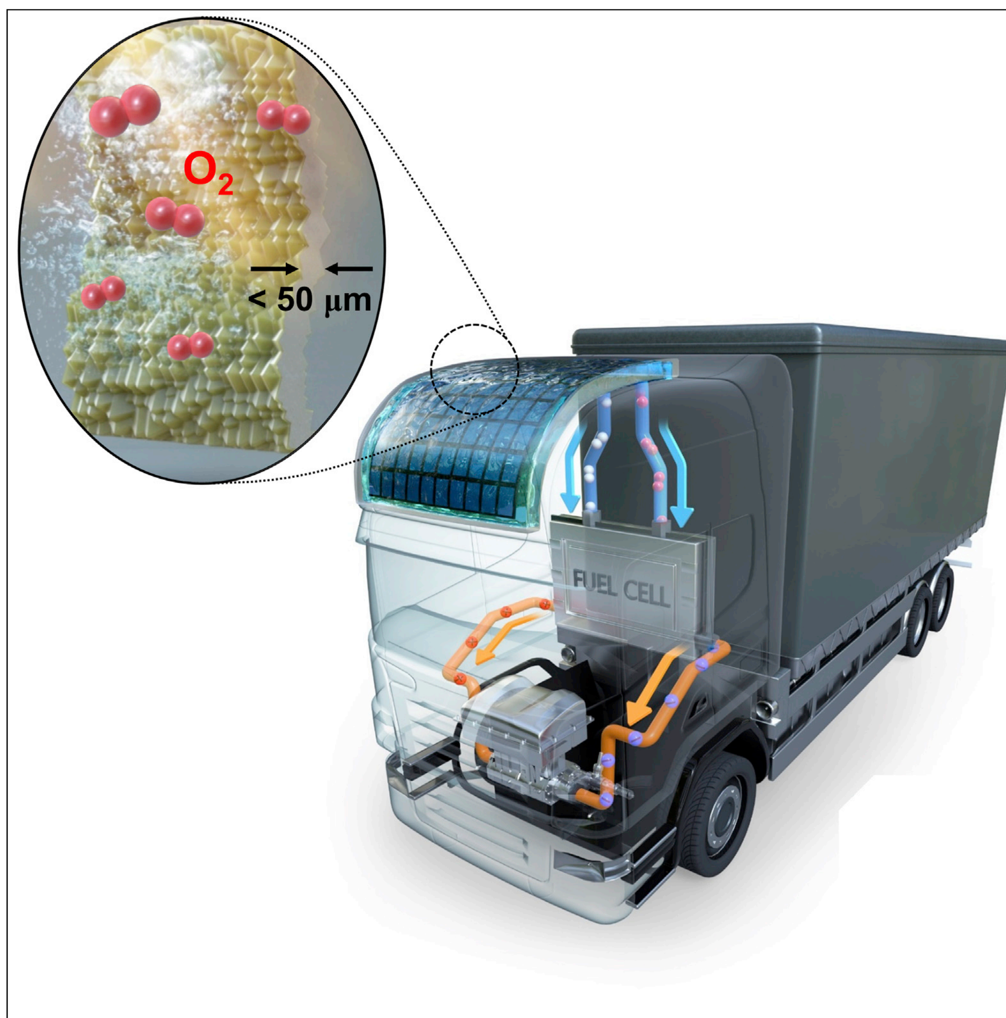
iScience

CellPress
OPEN ACCESS

Article

Thin silicon via crack-assisted layer exfoliation for photoelectrochemical water splitting



Yonghwan Lee, Bikesh Gupta, Hark Hoe Tan, Chennupati Jagadish, Jihun Oh, Siva Karuturi

yhlee@geri.re.kr (Y.L.)
siva.karuturi@anu.edu.au (S.K.)

Highlights

Design and fabrication of thin Si photoanode using crack-assisted layer exfoliation

A systematic investigation of the crack-assisted layer exfoliation method

Optical simulation on the dependence of photoelectrochemical performance on Si thickness

Demonstration of thin Si photoanode with notable photoelectrochemical performance

Lee et al., iScience *24*, 102921
August 20, 2021 © 2021 The Author(s).
https://doi.org/10.1016/j.isci.2021.102921

iScience

CellPress
OPEN ACCESS

Article

Thin silicon via crack-assisted layer exfoliation for photoelectrochemical water splitting

Yonghwan Lee,[1,2,6,*] Bikesh Gupta,[1] Hark Hoe Tan,[1,3] Chennupati Jagadish,[1,3] Jihun Oh,[4] and Siva Karuturi[1,5,*]

SUMMARY

Silicon (Si) has been widely investigated as a feasible material for photoelectrochemical (PEC) water splitting. Compared to thick wafer-based Si, thin Si (<50 μm thickness) could concurrently minimize the material usage allowing the development of cost-effective and flexible photoelectrodes for integrable PEC cells. This work presents the design and fabrication of thin Si using crack-assisted layer exfoliation method through detailed optical simulations and a systematic investigation of the exfoliation method. Thin free-standing Si photoanodes with sub-50 μm thickness are demonstrated by incorporating a nickel oxide (NiO_x) thin film as oxygen evolution catalyst, light-trapping surface structure, and a rear-pn$^+$ junction, to generate a photo-current density of 23.43 mA/cm^2 with an onset potential of 1.2 V (vs. RHE). Our work offers a general approach for the development of efficient and cost-effective photoelectrodes with Si films with important implications for flexible and wearable Si-based photovoltaics and (opto)electronic devices.

INTRODUCTION

Photoelectrochemical (PEC) water splitting provides a promising way to convert intermittent solar irradiation into storable chemical fuels such as hydrogen (H_2) (Lewis and Nocera, 2006; Sharma and Ghoshal, 2015). Designing advanced semiconductor photoelectrodes and obtaining a deeper understanding of their PEC performance are crucial for constructing highly efficient, stable and low-cost PEC cells for practical water splitting. Crystalline silicon (c-Si) has been considered as one of the promising materials for PEC water splitting due to its narrow bandgap (E_g = 1.1 eV) that allows absorption of visible region of the solar spectrum, appropriate band edge positions for water splitting reaction, and availability of mature manufacturing technologies (Chu et al., 2017; Luo et al., 2019). With these advantages, numerous reports appeared on wafer-based c-Si-based photoelectrodes with a thickness of 200–600 μm (Bae et al., 2015; Cai et al., 2017; Chen et al., 2015, 2017; Karuturi et al., 2020; Luo et al., 2019). Neverthless, the relatively high cost of c-Si substrate and modest performance achieved for Si photoelectrodes remained as impediments for cost-effective PEC water splitting for practical application (Jeong et al., 2013; Jung et al., 2015; Powell et al., 2012). In addition, the use of thicker wafers imparts rigidness to photoelectrodes making them unusable where flexibility is required.

One of the promising ways for realizing low-cost PEC-based water splitting with high performance is through utilization of thin (<50 μm) Si for the design of photoelectrodes, thereby reducing the volume of c-Si material by an order of magnitude and promoting enhanced carrier collection (Jung et al., 2015; Lee et al., 2018b; Liu et al., 2020; Massiot et al., 2020; Zhang et al., 2017). In addition to cost reduction, the use of thin Si films offers additional advantages: (1) The performance of the solar energy conversion devices becomes less affected by the material quality (*e.g.*, bulk minority carrier lifetime) (Jeong et al., 2013), (2) enhanced photovoltage can be realized due to photo-generated carrier concentration effect from reduced Si thickness (Brendel and Queisser, 1993; Zhang et al., 2014), (3) the total weight of the device can be lowered, and (4) the high flexibility and impact resistance enables integration on irregular surfaces such as electric vehicles, ships, aeroplanes, and drones (see Figure 1A). In spite of these noticeable advantages, it remained a challenge to fabricate thin Si-based photoelectrodes while maintaining high energy conversion performance, and thus the research on Si films for PEC water splitting is seldom reported.

Various approaches such as chemical etching, epitaxial growth using chemical vapor deposition, and epi-free lift-off and transfer have been developed to fabricate Si thin films with thicknesses ranging from a few

[1]Department of Electronic Materials Engineering, Research School of Physics, The Australian National University, Canberra, ACT 2601, Australia

[2]Convergence Materials Research Center, Gumi Electronics and Information Technology Research Institute (GERI), Gumi 39171, Republic of Korea

[3]Australian Research Council Center of Excellence for Transformative Meta-Optical Systems, Research School of Physics, The Australian National University, Canberra, ACT 2601, Australia

[4]Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon 34141, Republic of Korea

[5]Research School of Engineering, The Australian National University, Canberra, ACT 2601, Australia

[6]Lead contact

*Correspondence: yhlee@geri.re.kr (Y.L.), siva.karuturi@anu.edu.au (S.K.)

https://doi.org/10.1016/j.isci.2021.102921

This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

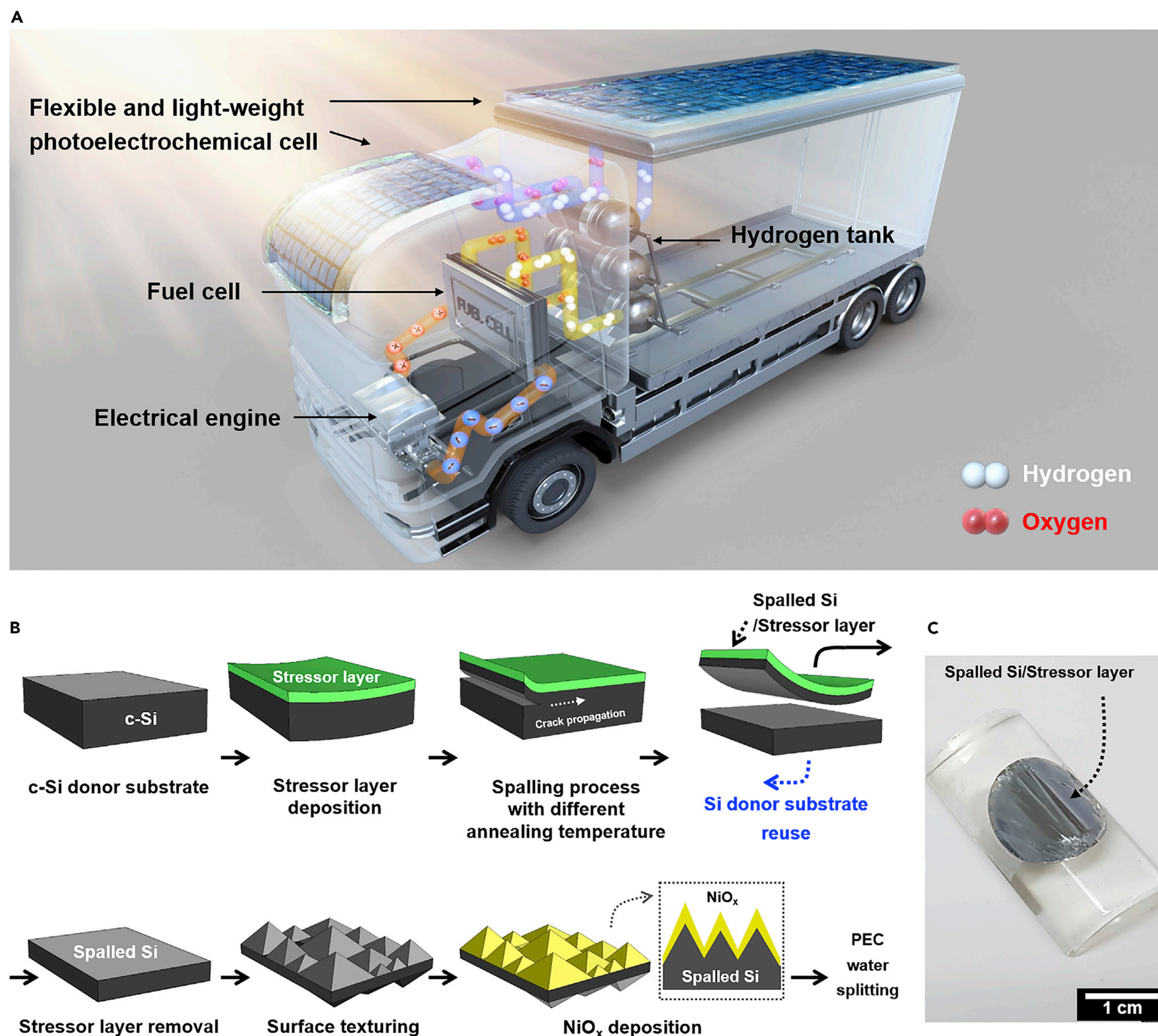


Figure 1. Illustration of integrated PEC cells on curved surfaces and the fabrication procedure for flexible Si photoelectrodes

(A) Schematic illustration of integrated PEC water splitting cells based on flexible photoelectrodes for self-powered hydrogen vehicles.

(B) Schematic illustration of the fabrication procedure for flexible Si photoanodes using the spalling process.

(C) Optical image of ~8 μm-thick flexible spalled Si fabricated by controlled spalling process with 15 μm-thick Ni stressor layer.

to tens of micrometers (Gordon et al., 2009; He et al., 2019; Xue et al., 2020). While the chemical etching process is not cost effective as the films are produced by etching away thick wafers, the other processes such as epitaxial gowth and lift-off are cumbersome and are energy, equipment, and cost intensive. Recently, intended cracking on brittle semiconductor substrates, known as spalling, has been introduced as a cost- and time-efficient approach for realizing wafer-scale flexible devices (Bedell et al., 2012, 2013; Kim et al., 2013; Lee et al., 2020a, 2020b; Shahrjerdi et al., 2013; Zhai et al., 2012). The spalling process enables exfoliation of semiconductor films (*i.e.*, spalled films) from a thick target donor substrate without any material loss by controlling the crack propagation direction in the donor substrate using a tensile-stressed film, called a stressor layer. Thin c-Si has been successfully obtained *via* the spalling process and has been used in fabricating flexible electronic devices and solar cells (Ahn et al., 2017; Li et al., 2017; Weisse et al., 2012). The spalling process proceeds through crack prograpation assisted by either an applied external force or thermal annealing. Although various experimental studies have been performed to understand

the spalling regimes, very little is known about the material quality obtained by these processes, particulary for PEC applications.

Here, we demonstrate free-standing thin Si photoanodes obtained using the spalling process. Optical simulations are carried out to reveal the effect of Si thickness and surface texturing on the PEC performance of spalled Si photoanodes. We systematically investigate the spalling process toward achieving a desirable thickness and material properties of spalled Si for application as a photoanode. Thin Si photoanodes are constructed by coating nickel oxide (NiO_x) catalyst on spalled Si to achieve an excellent photocurrent density of 23.4 mA/cm^2 with an E_{onset} of 1.2 eV, with the inclusion of surface texturing and rear pn$^+$ junction. Finally, we discuss future opportunities to improve the PEC performance of these thin Si photoanodes.

RESULTS

Preparation of thin Si photoanodes via spalling

Figure 1B illustrates the processing steps involved in the fabrication of a Si film using the spalling method and its adoption into a flexible photoanode for PEC water splitting application (see the experimental section for more details). First, Ni is electrodeposited on a c-Si donor substrate to form a tensile stress-inducing stressor layer. A Si film is then exfoliated from the c-Si donor substrate. Figure 1C shows a thin Si obtained via the spalling method. It is noted that the left-over Si donor substrate can be reused to produce additional Si films with repeated spalling steps. Thus, this approach could enable significant cost reduction for Si-based devices, in addition to imparting superior device properties such as flexibility and improved electrical performance. Subsequently, free-standing spalled Si can be obtained by removing the Ni stressor layer using a wet etching process. Surface texturing of free-standing spalled Si is performed using KOH solution to form micrometer-sized random pyramid structure. To adopt spalled Si layers into flexible photoanodes, NiO_x, known as an efficient and transparent oxygen evolution reaction (OER) catalyst, is deposited on the front side of the textured spalled Si using sputter deposition technique. Ga-In alloy is coated on the rear side of the textured spalled Si to form a rear Ohmic contact, which is then connected to a copper wire for electrical contacting. The rear side surface is then shielded using a chemical-resistant epoxy. The final device structure thus consists of a fully functional photoanode for driving the OER under sunlight exposure.

Design of thin Si photoanodes

While the use of Si films for photoelectrodes introduce advantages such as flexibility, cost-reduction, and reduced charge transfer lengths, it could also compromise the light harvesting ability as Si is an indirect bandgap semiconductor needing thicker material (>500 μm thickness) to fully absorb sunlight. To reveal the effect of thickness and role of texturing on light harvesting ability of Si photoanodes, we first carried out optical simulations on planar and textured Si as a function of thickness with water as a surrounding medium (see experimental section for more details). The geometry used for simulation is shown in Figure S1. Figures 2A and 2B show the calculated optical absorption (solid line) as a function of Si thickness with and without surface texturing, respectively. The optical absorption of textured Si is much higher than that of planar Si due to reduced optical reflection by light scattering effect (see Figures 2C and S2A). The optical absorption at shorter wavelengths (<700 nm) is not affected by Si thickness. However, there is significant reduction in optical absorption at longer wavelengths (>700 nm) with decreasing Si thickness. Figure 2D illustrates the dependence of light absorption on incident light wavelength in textured Si. At 450 nm, light absorption mainly occurs at the front surface (see Figure 2D, left), whereas the absorption extends deeper at 1000 nm, due to low absorption coefficients of Si at longer wavelengths (see Figures 2D and S2B). Surface texturing helps to both improve the optical absorption at longer wavelengths and reduce the optical reflection of Si. For instance, light absorptions for 50 μm-thick planar Si at 900 nm wavelengths are 64.4%, while much higher corresponding values of 91.1% are observed for textured Si of the same thickness.

To understand the effect of Si thickness on photoanode performance, we calculated the photo-generated current density with and without texturing as shown in Figure 2E. The photo-generated current density reduces gradually with decreasing thickness for both planar and textured Si due to insufficient absorption depths at longer wavelengths. Textured Si shows significantly enhanced photo-generated current density than planar Si for all thicknesses. For instance, the simulated current densities for 50 μm-thick spalled Si with and without texturing are 37.9 and 27.3 mA/cm^2, respectively, representing a significant enhancement in current generation (~40%) after texturing. Figure 2F shows the influence of the incident angle of light on photo-current density. Textured Si shows superior photo-generated current density than planar Si at all

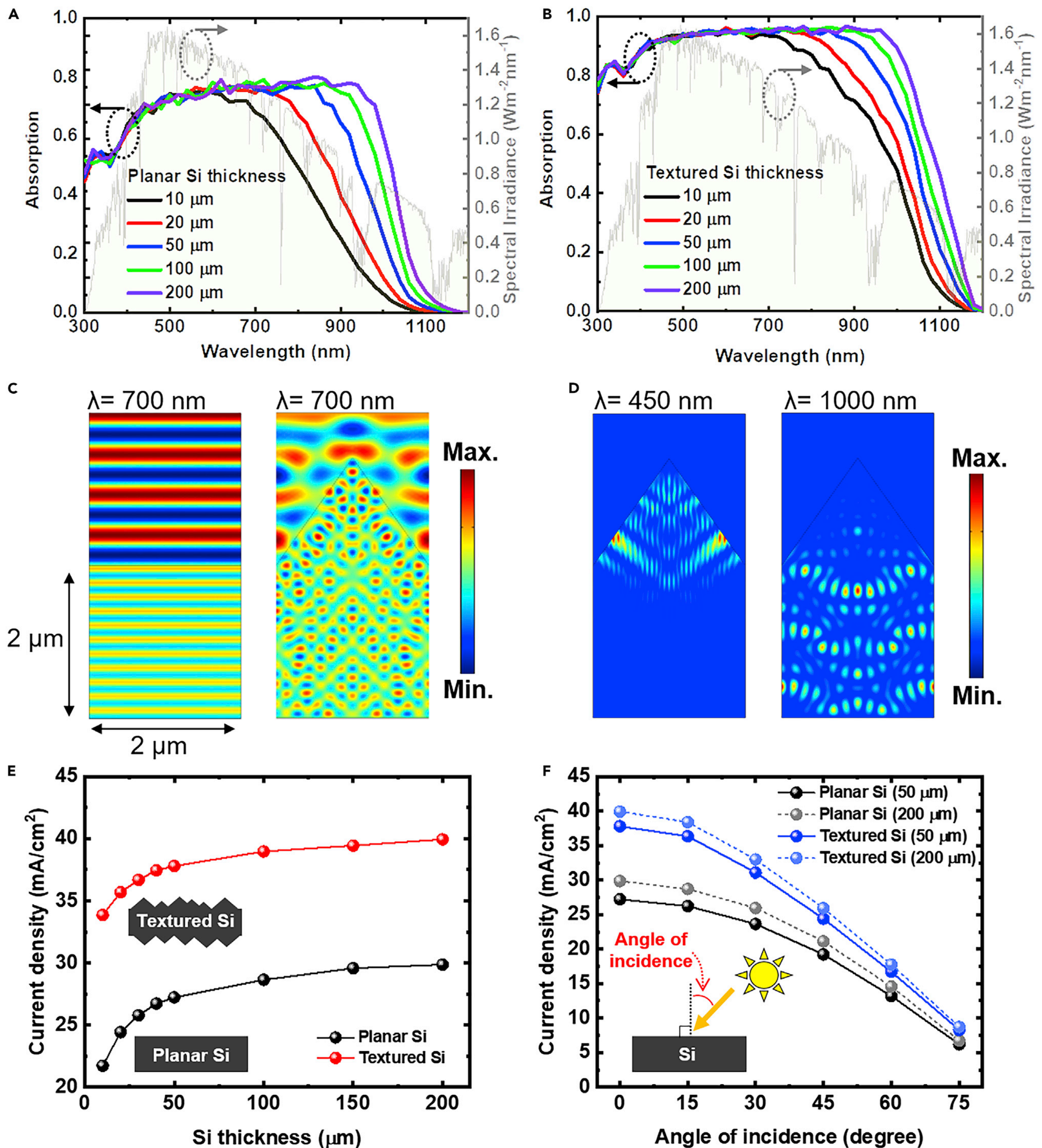


Figure 2. Optical properties of spalled Si films as a function of thickness with and without surface texturing

(A and B) Calculated optical absorption of Si film with (A) planar surface and (B) textured surface as a function of thickness. AM1.5G spectral irradiance is also shown for reference.

(C) Electric field distribution on planar surface (left) and textured surface (right) at the wavelength of 700 nm.

(D) Absorption profile of textured Si at the wavelength of 450 nm (left) and 1000 nm (right).

The calculated photo-generated current density of Si films as a function of (E) thickness and and (F) angle of incidence, for both planar and textured films.

angles (0-75°). Therefore, these results confirm that thin Si photoanodes (20-50 μm) could achieve sufficient light harvesting when double-sided surface texturing is introduced. In addition, transparent metal oxide cocatalyst films such as NiO_x with appropriate thickness could further enhance the photo-generated current density due to their anti-reflection property (Sun et al., 2015).

Fabrication of thin Si via the spalling process

We utilized the spalling process to exfoliate the Si film for photoanodes. In the spalling process, a semiconductor film can be exfoliated from a donor substrate via subsurface crack propagation assisted by either an annealing process or an applied external force. However, the role of the annealing process on layer exfoliation and its influence on the materials properties of spalled semiconductors remain unclear. With the aim of producing high quality thin Si for application as free-standing photoelectrodes, we systematically investigated the spalling process focusing on stressor layer thickness and annealing temperature.

Figure 3A shows the type of spalling as a function of the annealing temperature and stressor layer thickness. It is observed that the spalling process occurs spontaneously when an appropriate thickness of stressor layer and sufficient annealing temperature are used, and we define the spalling condition as spontaneous spalling (red dots in Figure 3A). The annealing process impacts the residual stress σ_s in the Ni stressor layer. Figure 3B shows the top view scanning electron microscope (SEM) images of the Ni stressor layer before and after the annealing process. The nano-sized grains of the electrodeposited Ni layer are enlarged after annealing, which increases the tensile stress in the Ni stressor layer (Abadias et al., 2018; Wang et al., 2004). Figure S3 shows the measured σ_s in the Ni stressor layer as a function of the annealing temperature using X-ray diffraction $\sin^2(\Psi)$ technique (Noyan and Cohen, 2013). The tensile σ_s in as-deposited Ni stressor layer of 403 MPa increases to 526 and 687 MPa when annealed at 300°C and 400°C, respectively.

Suo et al. developed a theoretical model on the spalling process of a bilayered system (Suo and Hutchinson, 1989). For crack propagation in the donor substrate, the energy release rate G has to be higher than the critical energy release rate G_c (*e.g.*, G_c for Si is 6.4 J/m^2) (Callister and Rethwisch, 2013). The following simplified equation shows the dependence of G on σ_s and stressor layer thickness (h_s) in a bilayered system (Lee et al., 2016; Suo and Hutchinson, 1989).

$$G \propto \sigma_s^2 h_s \quad \text{(Equation 1)}$$

Therefore, if G increases to a value higher than G_c of c-Si donor substrate due to an increased σ_s after annealing, it results in spontaneous spalling as shown in Figure 3A.

In the case of non-spontaneous spalling (denoted by blue dots in Figure 3A), the spalling process does not occur due to insufficient G. Bedell et al. demonstrated that the G in a bilayered system can be increased to G_c by applying external mechanical force, which enables the spalling process non-spontaneously to occur even at room temperature (Bedell et al., 2013). This process is defined as controlled spalling.

We investigated the thickness of the spalled Si as a function of h_s. Figure 3C shows the cross-sectional SEM images of the spalled Si fabricated by controlled spalling at room temperature. The resulting spalled thicknesses are 7.6, 26, 34, and 50 μm corresponding to h_s values of 15, 20, 25, and 30 μm, respectively. In addition, we found that the thickness of the spalled Si gradually increases with increasing annealing temperature (see Figure 3D). For instance, the thicknesses of spalled Si with 15 μm-thick Ni stressor layer are 7.6, 22, and 38.5 μm with annealing temperatures of 25°C, 300°C, and 400°C, respectively. The thickness of spalled Si, which is fixed by crack propagation depth in the spalling process, is determined by the dimensional and elastic parameters of the stressor layer (Suo and Hutchinson, 1989). For instance, the crack propagation depth is proportional to stressor layer thickness as shown in Figure 3C (Bedell et al., 2013; Lee et al., 2016; Suo and Hutchinson, 1989). In addition, we anticipate that the annealing process induces a variation of Young's modulus of the electrodeposited Ni stressor layer. Torrents et al. showed that Young's modulus of electrodeposited Ni thin film increases from 165 to 240 GPa after annealing at 227°C (Torrents et al., 2010). As shown in Figure 3B, the nano-crystalline grain growth in the Ni stressor layer after the annealing process increases the Young's modulus of the Ni stressor layer, which further increases the crack propagation depth (Lee, 2018; Suo and Hutchinson, 1989). Consequently, the annealing temperature and stressor layer thickness have to be carefully optimized to obtain the desired thickness of spalled Si.

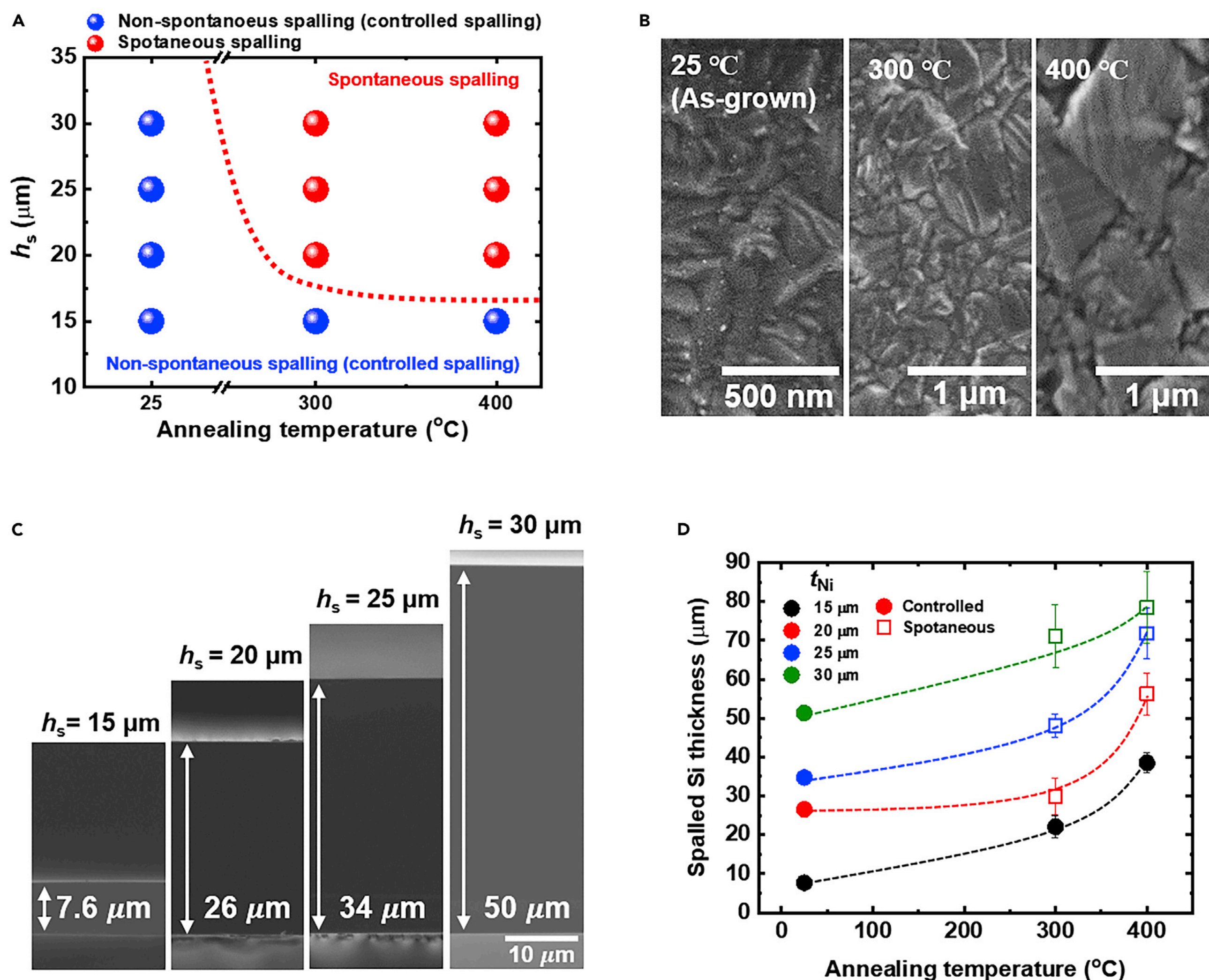


Figure 3. Investigation of the effect of stressor layer thickness and annealing temperature on the spalling process

(A) Type of spalling process as a function of the annealing temperature and stressor layer thickness.

(B) Top view SEM images of a 10 μm-thick Ni stressor layer after annealing at different temperatures.

(C) Cross-sectional SEM images of spalled Si after stressor layer removal. The spalled Si films were fabricated by controlled spalling process at room temperature with different Ni stressor layer thicknesses.

(D) Measured spalled Si thickness as a function of stressor layer thickness and annealing temperature. Data points represent mean ± standard deviation.

Material properties of spalled Si

We investigated the material properties of the free-standing ~50 μm-thick spalled Si fabricated via either the controlled or spontaneous spalling process. The controlled spalling process was conducted at room temperature (25°C) with 30 μm-thick Ni stressor layer, while the spontaneous spalling process was conducted at annealing temperatures of 300°C and 400°C with 25 and 20 μm-thick stressor layers, respectively, to produce ~50 μm-thick spalled Si layers. Figure 4A shows the measured surface profile of the fracture surfaces of the spalled films. The spalled Si fabricated by controlled spalling at room temperature shows a relatively smooth fracture surface with an average surface roughness (R_a) of 466 ± 10 nm (see Figure 4B). On the other hand, the spalled Si fabricated by spontaneous spalling process shows a much rougher fracture surface (see inset in Figure 4B), at 669 ± 275 and 865 ± 85 nm, for the 300°C and 400°C samples, respectively.

Figure 4C shows the measured residual stress σ_{Si} of the spalled Si films as a function of the annealing temperature. σ_{Si} obtained for the 25°C, 300°C, and 400°C samples are 54, 271, and 317 MPa, respectively. We removed the Ni stressor layer from the spalled Si prior to σ_{Si} measurements. Therefore, the measured σ_{Si} of

CellPress
OPEN ACCESS

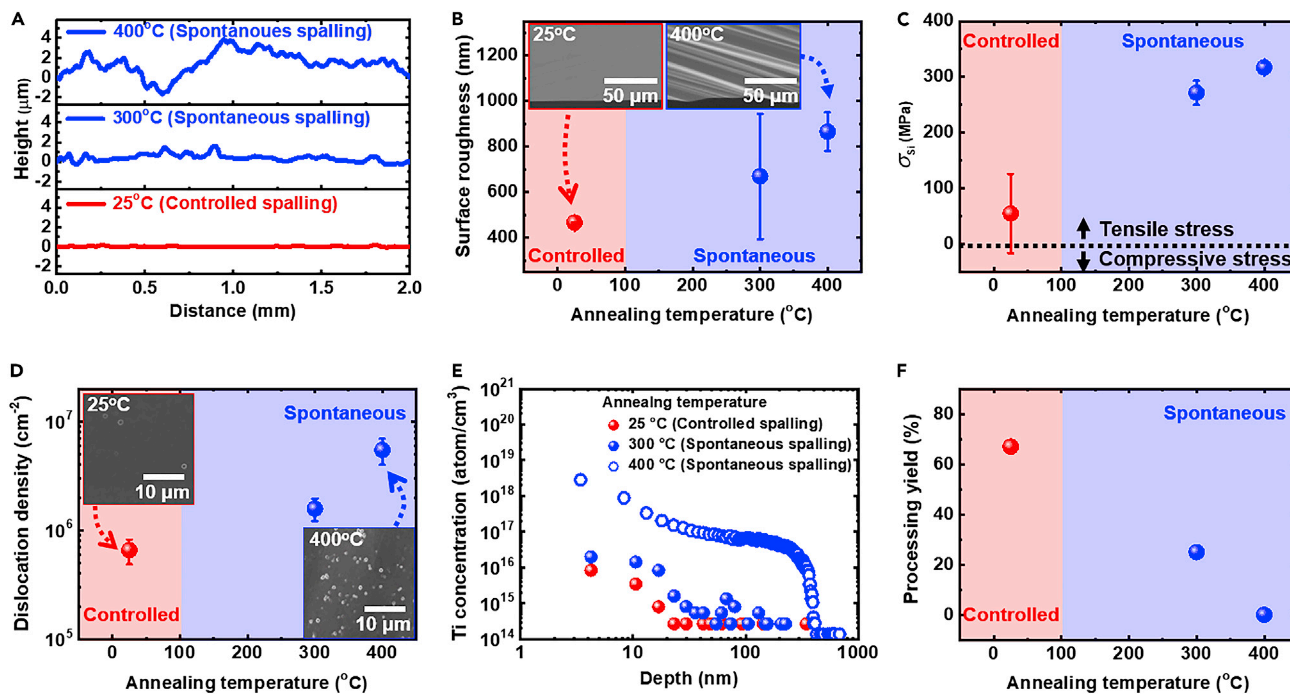


Figure 4. Characterization of material properties of free-standing 50 μm-thick spalled Si

(A–D) (A) Surface profile, (B) surface roughness, (C) residual stress, and (D) dislocation density on the fracture surfaces of spalled Si fabricated at different annealing temperatures. The insets in (B) show the tilted-view SEM images of the fracture surface of spalled Si exfoliated via controlled spalling at room temperature (red box) and spontaneous spalling process at 400°C (blue box). The insets in (D) show the top-view SEM images of the fracture surface of spalled Si after Secco etching process. Data points represent mean $\pm$ standard deviation.

(E) Measured concentration of Ti impurity in the spalled Si after annealing and removal of the Ni stressor layer.

(F) Processing yield of spalled Si after stressor layer removal.

the free-standing spalled Si is induced by surface defects generated during the crack propagation step (Lee et al., 2018). For more detailed analysis, we measured the defect density on fracture surfaces of spalled Si after Secco etching process (see Figure 4D) (d'Aragona, 1972; Fathi, 2007). The observed defect densities after Secco etching are 0.66×10^6, 1.58×10^6, and 5.46×10^6 cm^{-2} for the 25°C, 300°C, and 400°C samples, respectively. The defect density of spalled Si follows the same trend with the measured σ_{Si} as a function of annealing temperature. Our observations confirm that surface roughness, σ_{Si}, and defect density at the fracture surface of spalled Si increase dramatically when spalling is conducted at higher temperatures.

We believe that the dependence of material quality on the annealing temperature originates from a change in crack propagation velocity. In the controlled spalling process conducted at room temperature, the spalling process is carried at a timescale of a few seconds in a defined area of 2 cm diameter to fully exfoliate the spalled Si film from the c-Si donor substrate. However, the spontaneous spalling process at high annealing temperature occurs with high crack propagation velocity, and usually within a few microseconds (Bellanger et al., 2016; Coll et al., 2018). Arakawa et al. experimentally showed that fractured surface roughness in a brittle material is proportional to crack propagation velocity (Arakawa and Takahashi, 1991). Fineberg et al. showed that low crack propagation velocity results in a smoother fractured surface. In addition, micro-branching could also occur at the fracture surface with high crack propagation velocities (Fineberg et al., 1991; Fineberg and Marder, 1999). The micro-branches at the fracture surface exist as surface defects such as nano/micro-cracks which can significantly reduce the performance of Si photoelectrodes (Dhimish and Holmes, 2019). Therefore, the controlled spalling process conducted at room temperature, which allows controllability over crack propagation velocity through an applied external force, is a better approach to exfoliate thin Si with appropriate material property.

In this spalling process, Ti and Ni were used as adhesion and stressor layers, respectively. The metal elements can diffuse into the spalled Si, and could result in performance degradation (Sakiotis, 1982).

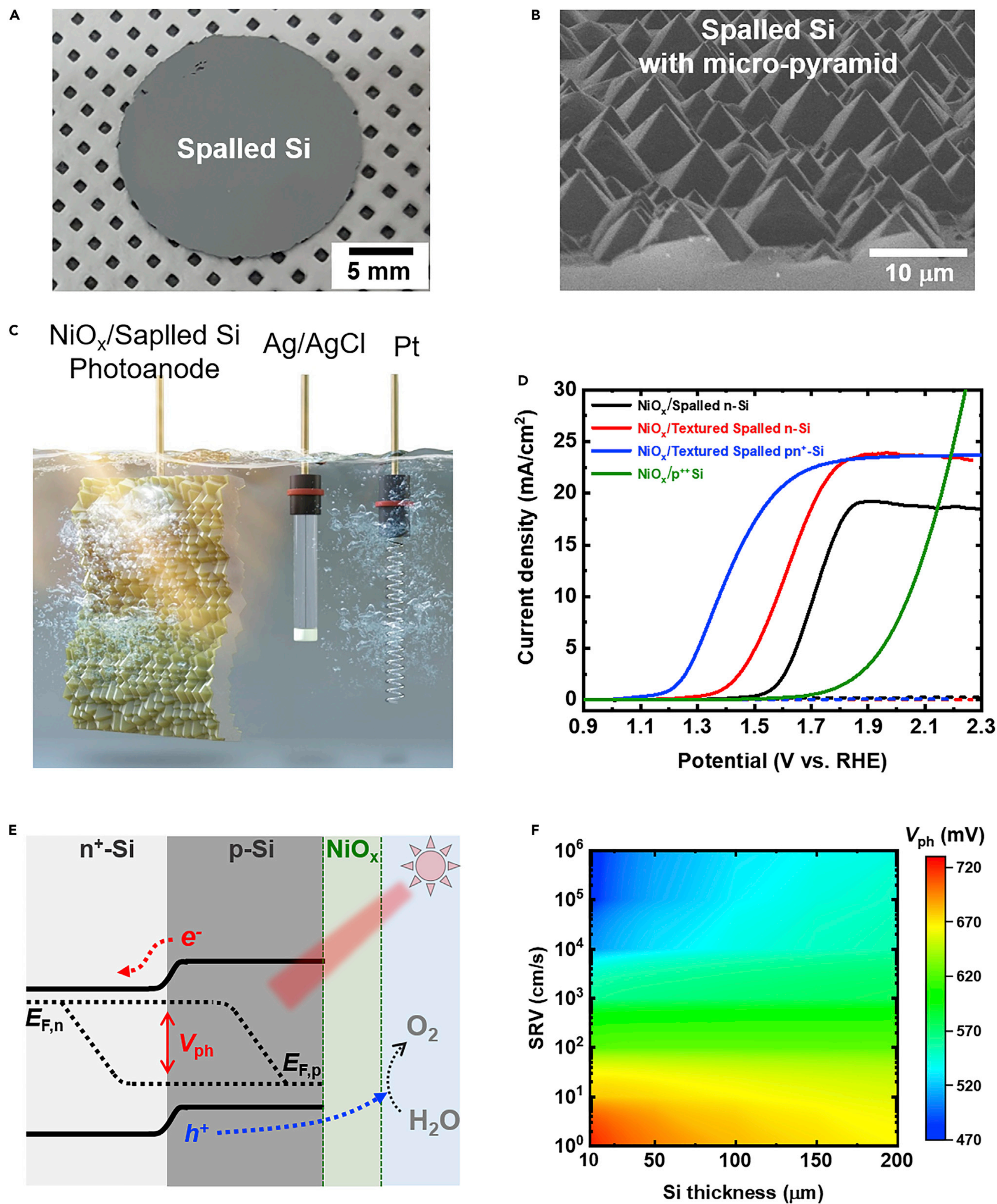


Figure 5. Photoelectrochemical study of ultrathin NiO_x/Si photoanodes

(A) Optical image of a 50 μm-thick spalled Si with a diameter of 2 cm after Ni stressor layer removal. The spalled Si was fabricated by the controlled spalling process using 30 μm-thick Ni based stressor layer at room temperature.

Figure 5. *Continued*

(B) Tilted-view SEM image of the spalled Si after texturing with the KOH wet etching process.

(C) Artist impression of the PEC cell consisting of ultrathin NiO_x -coated spalled Si photoanode in a conventional three electrode configuration.

(D) Current density – potential curves of different spalled Si photoanodes.

(E) Energy bandgap diagram of NiO_x-coated spalled Si photoanode with a pn^+ junction.

(F) Calculated photovoltage (V_{ph}) of spalled Si photoanode with a pn^+ junction as a function of Si thickness and surface recombination velocity (SRV).

Secondary ion mass spectrometry (SIMS) was used to investigate the diffused metal impurity of free-standing spalled Si after the removal of Ti/Ni layers. Figure 4E shows the SIMS depth profile of Ti impurity (see Figure S4 for Ni metal impurity), confirming Ti diffusion of ~30 nm in depth from the surface when the annealing temperature is lower than 300°C. However, the Ti concentration dramatically increased at an annealing temperature of 400°C and the diffusion depth dramatically increased to ~500 nm. This region may need to be removed from the spalled Si before fabricating water-splitting photoelectrodes.

Figure 4F shows the processing yield of free-standing spalled Si after removal of the Ni stressor layer. Fail process occurs due to the formation of horizontal cracks in the spalled Si, which subsequently result in the disintegration of the films into multiple pieces after removal of the Ni stressor layer. The processing yields are 67, 25, and 0% for the 25°C, 300°C, and 400°C samples, respectively. We attribute the reduced processing yield at higher annealing temperature to high surface roughness and residual stress on the fracture surface, which result in undesirable cracking states (Echizenya et al., 2011; Yang et al., 2013).

Application of thin free-standing Si as photoanodes

Figure 5A shows free-standing ~50 μm-thick spalled Si with a diameter of 2 cm produced by the controlled spalling process at room temperature, which presents lowest surface defects after removal of the Ni stressor layer. In addition, the micro-scale pyramid surface structure was obtained using wet-etching process to enhance the photo-generated current density via light scattering effect (see Figure 5B).

Finally, we fabricated and characterized 20 nm-thick NiO_x-coated spalled Si photoanodes with and without surface texture, labeled as NiO_x/Spalled n-Si and NiO_x/Textured Spalled n-Si, in 1M KOH solution using a typical three-electrode configuration under simulated AM1.5G illumination as illustrated in Figure 5C. The NiO_x film on Si serves as an efficient OER catalyst, provides surface protection, and could also function as an anti-reflection layer (Sun et al., 2012, 2015). As shown by the linear sweep voltammetry (LSV) measurements in Figure 5D, the planar photoanode shows an onset potential E_{onset} of 1.54 V (vs. RHE). It is noted that the E_{onset} is defined as the potential required to drive a photo-generated current density of 1 mA/cm^2. The planar and textured samples show saturation current densities J_{sat} of 19.2 and 23.8 mA/cm^2, respectively. Negligible dark current densities are observed (dotted line in Figure 5D), confirming no undesirable side reactions. Texturing leads to an improvement in current density by 4.6 mA/cm^2 due to enhanced light trapping compared to the planar photoanode even ~20 μm of material is removed during the texturing process (see Figure S5). In addition, E_{onset} decreases from 1.56 to 1.39 V, showing enhanced photovoltage (V_{ph}) from the removal of defects on the fracture surface during the surface texturing process (Lee et al., 2018b). This confirms that the surface texturing is crucial to achieve high performance in Si film photoanodes. We also introduced a pn^+ junction into the spalled Si to increase V_{ph}. Figure S6 shows the fabrication procedure for the NiO_x-coated spalled Si photoanode incorporating a rear pn^+ junction and surface texturing process. As clearly seen in Figure 5D (blue solid line), the sample shows a similar photo-current density but reduced E_{onset} due to enhanced V_{ph} (0.65 V) from the rear pn^+ junction compared to the textured sample but without a pn^+ junction. Here, the V_{ph} is approximated as the potential difference between NiO_x/textured spalled pn^+-Si and NiO_x/p^{++}-Si at 10 mA/cm^2 in 1M KOH.

The relatively lower J_{sat} value for all the photoelectrodes compared to the theoretically predicted values as presented in Figure 2E is due to undesired light transmission losses in the quartz cell and the electrolyte solution and a lack of surface passivation resulting in charge recombination (see Figure S7) (Lee et al., 2018; Malitson, 1965; Irvine and Pollack, 1968). J_{sat} can be further enhanced by including an effective passivation layer and introducing rear surface texturing for light trapping enhancement at long wavelength (Sun et al., 2015; Tamang et al., 2016; Zhang et al., 2014).

Further, we theoretically investigated the effect of passivation on the OER performance. Figure 5E shows the energy band diagram of the NiO_x-coated spalled photoanode with a rear pn^+ junction. The splitting of

the electron and hole quasi-Fermi level occurs under light illumination, and the difference between the electron and hole quasi-Fermi levels represents V_{ph}. Figure 5F shows the theoretically calculated V_{ph} of spalled Si photoanodes as a function of thickness and surface recombination velocity (SRV). It can be clearly seen that V_{ph} reduces dramatically when the thickness of Si is decreased under high SRV (*e.g.*, >10^3 cm/s). On the contrary, at low SRV (*e.g.*, <10 cm/s), V_{ph} increases significantly with reducing Si thickness due to increased minority carrier density in the limited light-absorber thickness (Brendel and Queisser, 1993; Zhang et al., 2014). For instance, the calculated V_{ph} values at an SRV of 1 cm/s are 665.9., 681.9, 696.8, and 706.5 mV with Si thicknesses of 200, 100, 50, and 30 μm, respectively. As shown above, V_{ph} of our NiO_x/textured spalled pn^+-Si is 0.65 V and this value is comparable to the theoretically calculated values with Si thickness of 30 μm (0.5–0.7 V). This can be further improved above 0.7 V by incorporating effective surface passivation on thin Si photoanodes leading to superior V_{ph} generation compared to conventional wafer-based (~500 μm) Si photoanodes.

DISCUSSION

In conclusion, free-standing c-Si films with controlled thickness were fabricated using the spalling process. We systematically investigated the thermal annealing effect on the spalling process and the material properties of the spalled Si. The spalled Si fabricated by the controlled spalling process at room temperature shows relatively low surface roughness, low defect density, and high processing yield compared to that fabricated by the spontaneous spalling process at high annealing temperatures. Finally, we demonstrated NiO_x-coated spalled Si photoanodes with micro-pyramid texture and a rear pn^+ junction, which exhibit an E_{onset} of 1.2 V and a J_{sat} of 23.4 mA/cm^2. Our work shows that thin free-standing Si photoelectrodes fabricated using crack-assisted exfoliation hold a great potential to achieve cost-effectiveness, enhanced PEC performance, and importantly allow direct integration on curved surfaces.

LIMITATIONS OF THE STUDY

For high performance Si-based photoanodes, it is crucial to apply efficient co-catalysts with high activity for the OER. In this study involving a proof-of-concept demonstration, we applied transparent NiO_x as oxygen evolution catalyst for the evaluation of the PEC water splitting performance on thin Si-based photoelectrode. The performance of our thin Si-based photoelectrodes can be further significantly improved by incorporating multimetallic/multi-component co-catalysts and adopting a decoupled photoelectrode design which separates the light harvesting from the catalytic interface.

STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

- KEY RESOURCES TABLE
- RESOURCE AVAILABILITY
  - Lead contact
  - Materials availability
  - Data and code availability
- METHOD DETAILS
  - Spalling process for Si film exfoliation
  - Numerical optical simulations of Si film photoanodes
  - Materials characterization
  - Fabrication of *NiO_x*-coated spalled Si photoanodes
  - PEC measurement of spalled Si photoanodes
  - Fabrication of NiO_x/Textured spalled pn^+-Si photoanodes
  - Photovoltage calculation of spalled Si with pn^+ junction

SUPPLEMENTAL INFORMATION

Supplemental information can be found online at https://doi.org/10.1016/j.isci.2021.102921.

ACKNOWLEDGMENTS

We acknowledge the Australian Renewable Energy Agency (ARENA) and the Australian Research Council (ARC) for financial support. We also acknowledge the Australian National Fabrication Facility, ACT node for providing access to the fabrication facilities.

AUTHOR CONTRIBUTIONS

Y. Lee conceptualised the idea, carried out the experiments, analysed the data and wrote the manuscript. S. Karuturi contributed to data analysis, manuscript preparation and project supervision. B. Gupta helped with electrochemical characterizations. H. H. Tan, C. Jagadish, and J. Oh discussed the results and analysed the data. All the authors commented on and revised the manuscript.

DECLARATION OF INTERESTS

The authors declare no conflict of interest.

Received: April 14, 2021
Revised: June 21, 2021
Accepted: July 27, 2021
Published: August 20, 2021

REFERENCES

Abadias, G., Chason, E., Keckes, J., Sebastiani, M., Thompson, G.B., Barthel, E., Doll, G.L., Murray, C.E., Stoessel, C.H., and Martinu, L. (2018). Stress in thin films and coatings: current status, challenges, and prospects. J. Vac. Sci. Technol. A *36*, 020801.

Ahn, J., Chou, H., and Banerjee, S.K. (2017). Graphene-Al2O3-silicon heterojunction solar cells on flexible silicon substrates. J. Appl. Phys. *121*, 163105.

Arakawa, K., and Takahashi, K. (1991). Relationships between fracture parameters and fracture surface roughness of brittle polymers. Int. J. Fract. *48*, 103–114.

Bae, D., Pedersen, T., Seger, B., Malizia, M., Kuznetsov, A., Hansen, O., Chorkendorff, I., and Vesborg, P.C. (2015). Back-illuminated Si photocathode: a combined experimental and theoretical study for photocatalytic hydrogen evolution. Energy Environ. Sci. *8*, 650–660.

Bedell, S.W., Shahrjerdi, D., Hekmatshoar, B., Fogel, K., Lauro, P.A., Ott, J.A., Sosa, N., and Sadana, D. (2012). Kerf-less removal of Si, Ge, and III–V layers by controlled spalling to enable low-cost PV technologies. IEEE J. Photovolt. *2*, 141–147.

Bedell, S.W., Fogel, K., Lauro, P., Shahrjerdi, D., Ott, J.A., and Sadana, D. (2013). Layer transfer by controlled spalling. J. Phys. D Appl. Phys. *46*, 152002.

Bednar, N., Severino, N., and Adamovic, N. (2015). Optical simulation of light management in CIGS thin-film solar cells using finite element method. Appl. Sci. *5*, 1735–1744.

Bellanger, P., Slaoui, A., Minj, A., Martini, R., Debucquoy, M., and Serra, J.M. (2016). First solar cells on exfoliated silicon foils obtained at room temperature by the SLIM-cut technique using an epoxy layer. IEEE J. Photovolt. *6*, 1115–1122.

Brendel, R., and Queisser, H. (1993). On the thickness dependence of open circuit voltages of pn junction solar cells. Sol. Energy Mater. Sol. Cells *29*, 397–401.

Cai, Q., Hong, W., Jian, C., Li, J., and Liu, W. (2017). Impact of silicon resistivity on the performance of silicon photoanode for efficient water oxidation reaction. ACS Catal. *7*, 3277–3283.

Callister, W., and Rethwisch, D. (2013). Fundamentals of Materials Science and Engineering (Wiley).

Chen, Y., Tran, P.D., Boix, P., Ren, Y., Chiam, S.Y., Li, Z., Fu, K., Wong, L.H., and Barber, J. (2015). Silicon decorated with amorphous cobalt molybdenum sulfide catalyst as an efficient photocathode for solar hydrogen generation. ACS Nano *9*, 3829–3836.

Chen, C.-J., Yang, K.-C., Liu, C.-W., Lu, Y.-R., Dong, C.-L., Wei, D.-H., Hu, S.-F., and Liu, R.-S. (2017). Silicon microwire arrays decorated with amorphous heterometal-doped molybdenum sulfide for water photoelectrolysis. Nano Energy *32*, 422–432.

Chu, S., Li, W., Yan, Y., Hamann, T., Shih, I., Wang, D., and Mi, Z. (2017). Roadmap on solar water splitting: current status and future prospects. Nano Futures *1*, 022001.

Coll, P.G., Meier, R., and Bertoni, M. (2018). Dynamics of Crack Propagation during Silicon Spalling (IEEE 7th World Conference on Photovoltaic Energy Conversion), pp. 2537–2539.

d'Aragona, F.S. (1972). Dislocation etch for (100) planes in silicon. J. Electrochem. Soc. *119*, 948–951.

Dhimish, M., and Holmes, V. (2019). Solar cells micro crack detection technique using state-of-the-art electroluminescence imaging. J. Sci. Adv. Mater. Devices *4*, 499–508.

Diffused Ion Implantation Profile Calculator and Graph (2020). https://cleanroom.byu.edu/implantcal.

Echizenya, D., Sakamoto, H., and Sasaki, K. (2011). Effect of mechanical surface damage on Silicon wafer strength. Proced. Eng *10*, 1440–1445.

Farrukh, M.A. (2012). Advanced Aspects of Spectroscopy (Intech).

Fathi, M. (2007). Delineation of crystalline extended defects on multicrystalline silicon wafers. Int. J. Photoenergy *2007*, 18298.

Fineberg, J., and Marder, M. (1999). Instability in dynamic fracture. Phys. Rep. *313*, 1–108.

Fineberg, J., Gross, S.P., Marder, M., and Swinney, H.L. (1991). Instability in dynamic fracture. Phys. Rev. Lett. *67*, 457.

Gordon, I., Vallon, S., Mayolet, A., Beaucarne, G., and Poortmans, J. (2009). Thin-Film Monocrystalline-Silicon Solar Cells on Transparent High-Temperature Glass-Ceramic Substrates (34th IEEE Photovoltaic Specialists Conference), pp. 228–231.

Green, M.A. (1982). Solar Cells: Operating Principles, Technology, and System Applications (Prentice-Hall).

Green, M.A. (2008). Self-consistent optical parameters of intrinsic silicon at 300 K including temperature coefficients. Sol. Energy Mater. Sol. Cells *92*, 1305–1310.

He, J., Hossain, M.A., Lin, H., Wang, W., Karuturi, S.K., Hoex, B., Ye, J., Gao, P., Bullock, J., and Wan, Y. (2019). 15% Efficiency ultrathin silicon solar cells with fluorine-doped titanium oxide and chemically tailored poly (3, 4-ethylenedioxythiophene): poly (styrenesulfonate) as asymmetric heterocontact. ACS Nano *13*, 6356–6362.

Irvine, W.M., and Pollack, J.B. (1968). Infrared optical properties of water and ice spheres. ICARUS *8*, 324–360.

Jeong, S., McGehee, M.D., and Cui, Y. (2013). All-back-contact ultra-thin silicon nanocone solar cells with 13.7% power conversion efficiency. Nat. Commun. *4*, 1–7.

Jung, J.-Y., Park, M.-J., Li, X., Kim, J.-H., Wehrspohn, R.B., and Lee, J.-H. (2015). High performance H 2 evolution realized in 20 μm-thin silicon nanostructured photocathodes. J. Mater. Chem. A *3*, 9456–9460.

Karuturi, S.K., Shen, H., Sharma, A., Beck, F.J., Varadhan, P., Duong, T., Narangari, P.R., Zhang, D., Wan, Y., and He, J.H. (2020). Over 17% efficiency Stand-alone solar water splitting enabled by perovskite-silicon tandem absorbers. Adv. Energy Mater. *10*, 2000772.

Kim, J., Park, H., Hannon, J.B., Bedell, S.W., Fogel, K., Sadana, D.K., and Dimitrakopoulos, C.

(2013). Layer-resolved graphene transfer via engineered strain layers. Science *342*, 833–836.

Lee, Y.H. (2018). Fabrication and Characterization of Ultra-thin Semiconductors for Solar Energy Conversion Devices Using Spalling Process (Doctoral Dissertation) (Korea Advanced Institute of Science and Technology).

Lee, Y.H., Kim, Y.-J., Han, S.M.J., Song, H.-e., and Oh, J. (2016). Sub-5 μm-thick spalled single crystal Si foils by decoupling crack initiation and propagation. Appl. Phys. Lett. *109*, 132101.

Lee, Y.H., Cha, H., Choi, S., Chang, H.S., Jang, B., and Oh, J. (2018). Characterization of atomic-layer-deposited (ALD) Al2O3-passivated sub-50-μm-thick kerf-less Si wafers by controlled spalling. Electron. Mater. Lett. *14*, 363–369.

Lee, Y.H., Kim, J., and Oh, J. (2018b). Wafer-scale ultrathin, single-crystal Si and GaAs photocathodes for photoelectrochemical hydrogen production. ACS Appl. Mater. Inter. *10*, 33230–33237.

Lee, Y., Tan, H.H., Jagadish, C., and Karuturi, S.K. (2020a). Controlled cracking for large-area thin film exfoliation: working principles, status, and prospects. ACS Appl. Electron. Mater. *3*, 145.

Lee, Y., Yang, I., Tan, H.H., Jagadish, C., and Karuturi, S.K. (2020b). Monocrystalline InP thin films with tunable surface morphology and energy band gap. ACS Appl. Mater. Inter. *12*, 36380–36388.

Lewis, N.S., and Nocera, D.G. (2006). Powering the planet: chemical challenges in solar energy utilization. Proc. Natl. Acad. Sci. U SA *103*, 15729–15735.

Li, N., Bedell, S., Hu, H., Han, S.J., Liu, X.H., Saenger, K., and Sadana, D. (2017). Single crystal flexible electronics enabled by 3D spalling. Adv. Mater. *29*, 1606638.

Liu, Z., Sofia, S.E., Laine, H.S., Woodhouse, M., Wieghold, S., Peters, I.M., and Buonassisi, T. (2020). Revisiting thin silicon for photovoltaics: a technoeconomic perspective. Energy Environ. Sci. *13*, 12–23.

Luo, Z., Wang, T., and Gong, J. (2019). Single-crystal silicon-based electrodes for unbiased solar water splitting: current status and prospects. Chem. Soc. Rev. *48*, 2158–2181.

Malitson, I.H. (1965). Interspecimen comparison of the refractive index of fused silica. J. Opt. Soc. Am. *55*, 1205–1209.

Massiot, I., Cattoni, A., and Collin, S. (2020). Progress and prospects for ultrathin solar cells. Nat. Energy *5*, 959–972.

Noyan, I.C., and Cohen, J.B. (2013). Residual Stress: Measurement by Diffraction and Interpretation (Springer).

Powell, D.M., Winkler, M.T., Choi, H., Simmons, C.B., Needleman, D.B., and Buonassisi, T. (2012). Crystalline silicon photovoltaics: a cost analysis framework for determining technology pathways to reach baseload electricity costs. Energy Environ. Sci. *5*, 5874–5883.

PV Lighthouse: Resistivity Calculator (2020). https://www.pvlighthouse.com.au/resistivity.

PV Lighthouse: Wafer Ray Tracer (2016). https://www2.pvlighthouse.com.au/calculators/wafer%20ray%20tracer/wafer%20ray%20tracer.html.

Sakiotis, N. (1982). Role of impurities in silicon solar cell performance. Sol. Cells *7*, 87–96.

Shahrjerdi, D., Bedell, S.W., Bayram, C., Lubguban, C.C., Fogel, K., Lauro, P., Ott, J.A., Hopstaken, M., Gayness, M., and Sadana, D. (2013). Ultralight high-efficiency flexible InGaP/(in) GaAs tandem solar cells on plastic. Adv. Energy Mater. *3*, 566–571.

Sharma, S., and Ghoshal, S.K. (2015). Hydrogen the future transportation fuel: from production to applications. Renew. Sustain. Energy Rev. *43*, 1151–1158.

Sun, K., Park, N., Sun, Z., Zhou, J., Wang, J., Pang, X., Shen, S., Noh, S.Y., Jing, Y., and Jin, S. (2012). Nickel oxide functionalized silicon for efficient photo-oxidation of water. Energy Environ. Sci. *5*, 7872–7877.

Sun, K., Saadi, F.H., Lichterman, M.F., Hale, W.G., Wang, H.-P., Zhou, X., Plymale, N.T., Omelchenko, S.T., He, J.-H., and Papadantonakis, K.M. (2015). Stable solar-driven oxidation of water by semiconducting photoanodes protected by transparent catalytic nickel oxide films. Proc. Natl. Acad. Sci. USA *112*, 3612–3617.

Suo, Z., and Hutchinson, J.W. (1989). Steady-state cracking in brittle substrates beneath adherent films. Int. J. Sol. Struct. *25*, 1337–1353.

Tamang, A., Hongsingthong, A., Jovanov, V., Sichanugrist, P., Khan, B.A., Dewan, R., Konagai, M., and Knipp, D. (2016). Enhanced photon management in silicon thin film solar cells with different front and back interface texture. Sci. Rep. *6*, 1–10.

Torrents, A., Yang, H., and Mohamed, F.A. (2010). Effect of annealing on hardness and the modulus of elasticity in bulk nanocrystalline nickel. Metall. Mater. Trans. A *41*, 621–630.

Wang, Y., Cheng, S., Wei, Q., Ma, E., Nieh, T., and Hamza, A. (2004). Effects of annealing and impurities on tensile properties of electrodeposited nanocrystalline Ni. Scr. Mater. *51*, 1023–1028.

Weisse, J.M., Lee, C.H., Kim, D.R., and Zheng, X. (2012). Fabrication of flexible and vertical silicon nanowire electronics. Nano Lett. *12*, 3339–3343.

Xue, M., Nazif, K.N., Lyu, Z., Jiang, J., Lu, C.-Y., Lee, N., Zang, K., Chen, Y., Zheng, T., and Kamins, T.I. (2020). Free-standing 2.7 μm thick ultrathin crystalline silicon solar cell with efficiency above 12.0%. Nano Energy *70*, 104466.

Yang, C., Mess, F., Skenes, K., Melkote, S., and Danyluk, S. (2013). On the residual stress and fracture strength of crystalline silicon wafers. Appl. Phys. Lett. *102*, 021909.

Zhai, Y., Mathew, L., Rao, R., Xu, D., and Banerjee, S.K. (2012). High-performance flexible thin-film transistors exfoliated from bulk wafer. Nano Lett. *12*, 5609–5615.

Zhang, Y., Stokes, N., Jia, B., Fan, S., and Gu, M. (2014). Towards ultra-thin plasmonic silicon wafer solar cells with minimized efficiency loss. Sci. Rep. *4*, 4939.

Zhang, D., Shi, J., Zi, W., Wang, P., and Liu, S. (2017). Recent advances in photoelectrochemical applications of silicon materials for solar-to-chemicals conversion. ChemSusChem *10*, 4324–4341.

STAR★METHODS

KEY RESOURCES TABLE

REAGENT or RESOURCE	SOURCE	IDENTIFIER
Chemicals		
Nickelchloride hexahydrate	Sigma-Aldrich	CAS: 7791-20-0
Boric acide	Sigma-Aldrich	CAS: 10043-35-3
Software and algorithms		
COMSOL Multiphysics	COMSOL, Inc.	Version 5.4
Other		
Potentiostat	CH Instruments, Inc.	CHI660E
Illuminaiton source	ABET Technology	model 11002-2

RESOURCE AVAILABILITY

Lead contact

Future information and requests for resources should be directed to and will be fulfilled by the lead contact, Yonghwan Lee (yhlee@geri.re.kr)

Materials availability

New unique reagents were not generated in this study.

Data and code availability

Data and code would be made available upon request.

METHOD DETAILS

Spalling process for Si film exfoliation

Mirror-polished 500 μm-thick n-type Czockraski (CZ) c-Si (100) wafers (phosphorus doped, ρ = 1-10 Ω cm) were used as c-Si donor substrates. First, the c-Si donor substrates were cleaned by RCA 1 process, followed by dipping in a diluted HF (5 wt%) solution to remove the native oxide. Subsequently, a bilayer consisting 50 nm Ti (adhesion layer) and 50 nm Ni (seed layer) was deposited on the Si substrates using e-beam evaporator prior to Ni stressor layer deposition using electrodeposition process. A mask with a circular pattern of 2 cm diameter was attached onto the Ni/Ti coated Si substrates to define the electrodeposition area. The substrates were dipped in a diluted HCl (10 wt%) solution for 5 min, followed by rinsing in deionized water. The Ni electrodeposition was conducted in a chlorine-based Ni solution. After the Ni electroplating process, the spalling process was conducted via two different approaches, namely, spontaneous spalling and controlled spalling. For the former method assisted by a thermal annealing process, the Ni/Ti/Si substrates were annealed using a rapid thermal annealing (RTA) system for 5 min under varying annealing temperatures (300–400°C) in Ar atmosphere. After cooling-down in the RTA system, Si layers were spontaneously exfoliated due to the propagation of a sub-surface crack. For the controlled spalling process, an initial sub-surface crack was formed by mechanical wedge at/near the edge of Ni stressor layer and the locally separated Si was grasped by a tweezer and pulled in a vertical direction. Subsequently, the spalled Si was completely peeled away from the c-Si donor substrates. After the spalling process, the Ni stressor layer attached to the spalled Si was removed by wet etching in $HCl/H_2O_2/H_2O$ mixed solution (3:3:10, v/v/v) to produce free-standing Si.

Numerical optical simulations of Si film photoanodes

Light absorption and photocurrent density of c-Si substrates were simulated using Wafer Ray Tracer (WRT) simulation software (Version 1.6.7, PV Lighthouse Pty. Ltd., Australia) at 20 nm intervals and 5000 incident rays with different Si thickness (PV Lighthouse: Wafer Ray Tracer, 2016). The surrounding material was set to H_2O. The incident sunlight was chosen to be AM1.5G and the calculations were performed in the

wavelength range of 300–1200 nm. The refractive indices of the materials used in the simulation were taken from the literature (Green, 2008). The two-dimensional electrical field distribution and absorption profiles were analyzed using the wave optics module of COMSOL Multiphysics 5.4 software package. The detailed simulation structures are described in Figure S1. The absorption profile was calculated with electric field $E(\lambda)$ at specific wavelengths (λ) using the following equation:

$$P_{abs}(\lambda) = \frac{1}{2}\omega\varepsilon''|E(\lambda)|^2 \quad \text{(Equation 2)}$$

where ω is angular frequency which is equal to $2\pi/\lambda$ and ε'' is the imaginary component of complex permittivity of the material (Bednar et al., 2015).

Materials characterization

The thicknesss of spalled Si layers were measured using field-emission scanning electron microscopy (FE-SEM, Nova230, FEI Co., USA). The surface profile and roughness were characterized by surface profilometry (Dektak-8, VEECO, USA). The residual stress at the fracture surface of spalled Si was measured by micro-Raman spectrometer (DXR, Thermo Fisher Scientific, USA) with a laser wavelength of 514 nm. The stress σ_{Si} at the fracture surface in free-standing spalled Si was calculated using the following equation:

$$\sigma_{Si,xx} = \sigma_{Si,yy}(\mathrm{MPa}) = -250 \times \Delta\omega\ (cm^{-1}). \quad \text{(Equation 3)}$$

where $\Delta\omega$ is the Raman peak position shift between unprocessed c-Si donor substrate and free-standing spalled Si (Farrukh, 2012). Secondary ion mass spectrometry (SIMS, IMS 7f, CAMECA, France) was used to investigate the diffused metal impurities at the surface of free-standing spalled Si after the removal of the Ni stressor layer.

Fabrication of NiO_x-coated spalled Si photoanodes

To prepare pyramidal structures on the spalled Si, the 50 μm-thick free-standing Si obtained via the controlled spalling at room temperature was immersed into a mixed solution of KOH, isopropyl alcohol, and H_2O at 70–80°C for 40 min, followed by a cleaning step in $HCl/H_2O_2/H_2O$ mixed solution (1:1:5, v/v/v)) at ~80°C for 10 min. The cleaned spalled Si was immersed in a diluted HF (10 wt%) solution for 1 min to remove the surface native oxide. A 20 nm thick NiO_x cocatalyst film was deposited on the surface of the spalled Si using DC sputtering technique (NiO sputtering target, Ar atmosphere). An ohmic rear contact was formed using an In-Ga eutectic alloy and a copper wire was attached to this contact. In order to isolate and protect the rear contact of the spalled Si photoanodes in electrolyte solutions, the samples were sealed off using an epoxy (Loctite 9460), leaving the front surface (with the NiO_x cocatalyst film) for direct contact with the solution to participate in OER under illumination.

PEC measurement of spalled Si photoanodes

The PEC properties of the spalled Si were characterized in a typical three-electrode measurement configuration using a potentiostat. A Ag/AgCl (3M NaCl) and a Pt coil were used as the reference and counter electrodes, respectively. The illumination source was a 300 W Xe lamp (ABET Technology, model 11,002-2) equipped with AM1.5G filters. Light intensity was set to 1 sun using a reference solar cell. All the PEC polarization curves (*J-E*) were recorded in the anodic direction at a scan rate of 20 mV/s in 1 M KOH solution. All potentials were expressed as reversible hydrogen electrode (RHE) by $E_{RHE} = E_{WE} + (0.209 + 0.059 \times \mathrm{pH})$ V.

Fabrication of NiO_x/Textured spalled pn^+-Si photoanodes

A lightly doped 500 μm-thick p-type Czockraski Si (boron-doped, 1-10 Ω cm) wafers (100) were used. An n^+ region was formed by phosphorus implantation with a dose of 1.2×10^{15} cm^{-2} on top of a p-type Si wafer at an acceleration voltage of 80 keV. Afterward, an annealing process at 1000°C for 30 s in nitrogen (N_2) atmosphere was conducted to cure the damages induced by the ion implantation process. Subsequently, a Ti/Ni (50/50 nm) layer was deposited over the n^+ region of Si substrate using e-beam evaporator followed by Ni electrodeposition process (~30 μm thickness). Controlled spalling process was conducted at room temperature to exfoliate a Si film with the rear pn^+ junction and immersed into the KOH/IPA/H_2O mixed solution at 70–80°C for 40 min for surface texturing. The Ni stressor layer and e-beam evaporated Ti/Ni layer was removed by a $HCl/H_2O_2/H_2O$ mixed solution followed by diluted HF treatment. The 20 nm-thick NiO_x film was deposited on the surface of the spalled Si using DC sputter. Ohmic contact

was formed at the n^+ region using In-Ga eutectic alloy which was further connected to a copper wire. Finally, the sample was sealed with epoxy, leaving only the NiO_x surface in contact with the electrolyte.

Photovoltage calculation of spalled Si with pn^+ junction

The photovoltage V_{ph} of the spalled Si with a rear pn^+ junction was calculated as a function of SRV and Si thickness using the following equations:

$$V_{ph} = \frac{kT}{q} \ln\left(\frac{J_L}{J_0} + 1 \right) \quad \text{(Equation 4)}$$

where k is the Boltzmann constant, T is absolute temperature, q is the electron charge, J_L is the photocurrent density, and J_0 is the diode saturation current density (Green, 1982). J_0 was calculated as:

$$J_0 = \left(\frac{qD_e n_i^2}{L_e N_A} F_P + \frac{qD_h n_i^2}{L_h N_D} F_N \right) \quad \text{(Equation 5)}$$

where D_e is electron diffusivity in p-type region, D_h is hole diffusivity in n-type region, n_i is the intrinsic carrier concentration, L_e is electron diffusion length in p-type region, L_h hole diffusion length in n-type region, N_A is acceptor doping concentration in p-type region, and N_D is donor doping concentration in n-type region. It is noted that the substrate boron doping concentration was calculated using the resistivity calculator by setting the resistivity to 5 $\Omega \cdot$cm (PV Lighthouse: Resistivity Calculator, 2020). L_e, L_h, F_N and F_P were calculated using the following equations:

$$L_e = \sqrt{D_e \tau_e} \quad \text{(Equation 6)}$$

$$L_h = \sqrt{D_h \tau_h} \quad \text{(Equation 7)}$$

$$F_N = \frac{S_h \cosh\left(\frac{W_N}{L_h}\right) + \frac{D_h}{L_h} \sinh\left(\frac{W_N}{L_h}\right)}{\frac{D_h}{L_h} \cosh\left(\frac{W_N}{L_h}\right) + S_h \sinh\left(\frac{W_N}{L_h}\right)} \quad \text{(Equation 8)}$$

$$F_P = \frac{S_e \cosh\left(\frac{W_P}{L_e}\right) + \frac{D_e}{L_e} \sinh\left(\frac{W_P}{L_e}\right)}{\frac{D_e}{L_e} \cosh\left(\frac{W_P}{L_e}\right) + S_e \sinh\left(\frac{W_P}{L_e}\right)} \quad \text{(Equation 9)}$$

where τ_e is the electron carrier lifetime time in p-type region, τ_h is the hole carrier lifetime in n-type region, S_e is the SRV in p-type region, and S_h is SRV in n-type region, W_p is the p-type region width, and W_n is the n-type region width. It is noted that the n- and p-type region width (junction depth) were calculated using a ion implantation calculator (Diffused Ion Implantation Profile Calculator and Graph, 2020). The respective values of the parameters used in the calculations are summarized in Table S1 in the supplemental information.