PHYSICAL SCIENCES

Ferroelectric tunnel junctions integrated on semiconductors with enhanced fatigue resistance

Ningchong Zheng[1]†, Jiayi Li[1,2]†, Haoying Sun[1], Yipeng Zang[1,3], Peijie Jiao[1], Cong Shen[1], Xingyu Jiang[1], Yidong Xia[1], Yu Deng[1]*, Di Wu[1]*, Xiaoqing Pan[4], Yuefeng Nie[1]*

Oxide-based ferroelectric tunnel junctions (FTJs) show promise for nonvolatile memory and neuromorphic applications, making their integration with existing semiconductor technologies highly desirable. Furthermore, resistance fatigue in current silicon-based integration remains a critical issue. Understanding this fatigue mechanism in semiconductor-integrated FTJ is essential yet unresolved. Here, we systematically investigate the fatigue performance of ultrathin bismuth ferrite $BiFeO_3$ (BFO)–based FTJs integrated with various semiconductors. Notably, the BFO/gallium arsenide FTJ exhibits superior fatigue resistance characteristics (>10^8 cycles), surpassing the BFO/silicon FTJ (>10^6 cycles) and even approaching epitaxial oxide FTJs (>10^9 cycles). The atomic-scale fatigue mechanism is revealed as lattice structure collapse caused by oxygen vacancy accumulation in BFO near semiconductors after repeated switching. The enhanced fatigue-resistant behavior in BFO/gallium arsenide FTJ is due to gallium arsenide's weak oxygen affinity, resulting in fewer oxygen vacancies. These findings provide deeper insights into the atomic-scale fatigue mechanism of semiconductor-integrated FTJs and pave the way for fabricating fatigue-resistant oxide FTJs for practical applications.

INTRODUCTION

Ferroelectric tunnel junction (FTJ) memristors, due to the simple structure, low-power consumption, and simple weight update scheme, hold promising potential for applications in memory and neuromorphic computing (*1*–*5*). In general, FTJs are fabricated on the basis of ultrathin epitaxial ferroelectric oxides (*6*–*10*) with rigid substrate (named as epitaxial FTJ) for their high ferroelectric polarization and better stability. Among these, perovskite-type oxide FTJs exhibit well-established superior performance, including ultrahigh R_{ON}/R_{OFF} ratios (*11*), high thermostability (*12*), and subnanosecond read/write speeds (*12*, *13*). For practical industrial applications, it is essential to explore the feasibility of integrating high-performance FTJs on silicon and other semiconductors (named as integrated FTJ) to meet the increasing demands of modern information technologies (*14*–*18*). However, as semiconductor surfaces are typically prone to oxidation and form an amorphous oxide layer, it is challenging to grow crystalline perovskite oxides epitaxially on semiconductors (*19*, *20*). Recently, advanced growth-and-transfer techniques using sacrificial layers have greatly facilitated this integration (*21*–*24*). These techniques enable the fabrication of integrated FTJ devices on various substrates, including semiconductor wafers and flexible substrates, using freestanding membranes such as $BaTiO_3$ (BTO)/$La_{0.7}Sr_{0.3}MnO_3$ (LSMO)/BTO, $SrRuO_3/PbZr_{0.2}Ti_{0.8}O_3/SrRuO_3$, or $BiFeO_3$ (BFO) (*25*–*27*) or BTO/LSMO (*28*). Although these integrated FTJs have achieved a moderate R_{ON}/R_{OFF} ratio (~10^3), the switching reliability-cycling endurance (10^2 to 10^5 cycles) remains inferior compared to those of epitaxial FTJ, deserving further investigations.

A long-standing and crucial issue in FTJs is fatigue, which notably affects device performance. While extensive research has been conducted on the fatigue mechanisms of epitaxial FTJs (*29*–*31*) and HfO_2-based integrated FTJs (*32*–*35*), corresponding studies on integrated FTJs especially based on perovskite oxides are insufficient. Recent researches (*25*–*27*) have shown that the integrated FTJs hold promising potentials for practical applications, the switching reliability-fatigue remains inferior compared to that of epitaxial FTJ. For example, Lu *et al.* (*25*) reported reduced R_{ON}/R_{OFF} ratios with increasing switching cycles in Au/Cu/BTO/LSMO/BTO/SiO_2/Si FTJ. Zheng *et al.* (*27*) observed a decrease in the R_{ON}/R_{OFF} ratios from ~10^3 to ~10^2 after ~10^5 cycles FTJs in Pt/BFO/SiO_2/n^+ Si structures. To date, few studies to date have focused on the fatigue mechanism for tunneling electroresistance (TER) degradation with increasing switching cycles in semiconductor-integrated FTJs based on perovskite oxides, despite the urgent need for a deeper understanding.

Here, we systematically investigate fatigue behavior and uncover the mechanism of FTJ devices fabricated by integrating freestanding BFO with various semiconductors of great technological relevance, such as Si, Ge, and GaAs. Atomic-scale analysis demonstrates that reversal fatigue is triggered by the generation and accumulation of oxygen vacancies, forming a ferroelectric dead layer with a collapsed lattice structure. The fatigue-induced reduction in TER performance and effective polarization is observed in both Pt/BFO/oxide/n^+ Si FTJ (Si-FTJ) and Pt/BFO/oxide/n^+ GaAs FTJ (GaAs-FTJ) prototype devices. Notably, GaAs-FTJ exhibits enhanced fatigue resistance characteristics (>10^8 cycles) compared to Si-FTJ (>10^6 cycles) and approaches the optimal performance (>10^9 cycles) of epitaxial oxide FTJs (*10*, *12*, *13*). The fatigue-resistant performance in GaAs-FTJ is attributed to the higher activation energy required for oxidizing Ga or As, which reduces oxygen vacancies formation and minimizes lattice damage.

RESULTS

Microstructure and electrical performance

The schematic of the FTJs, consisting of the BFO layer, top electrode (Pt), amorphous oxide layer, and conductive semiconductor, is

[1]National Laboratory of Solid State Microstructures, Jiangsu Key Laboratory of Artificial Functional Materials, College of Engineering and Applied Science and Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing 210093, China. [2]Department of Mechanical Engineering, The University of Hong Kong, Pokfulam Road, Hong Kong 999077, China. [3]School of Materials Science and Engineering, Anhui Provincial Key Laboratory of Magnetic Functional Materials and Devices, Anhui University, Hefei 230601, China. [4]Department of Materials Science and Engineering and Department of Physics and Astronomy, University of California, Irvine, Irvine, CA 92697, USA.
*Corresponding author. Email: ynie@nju.edu.cn (Y.N.); diwu@nju.edu.cn (D.W.); dengyu@nju.edu.cn (Y.D.)
†These authors contributed equally to this work.

presented in Fig. 1A. Two kinds of FTJs, Si-FTJ and GaAs-FTJ, featuring a metal-ferroelectric-insulator-semiconductor (MFIS) structure, were fabricated (see Methods for details) and systematically explored to reveal the fatigue mechanism. The microstructures of the two FTJs were characterized using scanning probe microscopy and aberration-corrected scanning transmission electron microscope (STEM) images. Z-contrast high-angle annular dark-field (HAADF) cross-sectional images (Fig. 1, B and C) illustrate the atomically sharp interfaces and lattice structure of the as-fabricated samples. The out-of-plane and in-plane lattice parameters of the BFO membranes on Si and GaAs (Fig. 1D) substrates show a similar pseudocubic structure, confirming nearly identical lattice structures and initial polarization before switching. To investigate whether the amorphous oxide layers on semiconductor surfaces influence the ferroelectric domain switching of BFO, we conducted piezoresponse force microscopy (PFM) measurements. Clear out-of-plane polarization reversals (Fig. 1, E and F) are observed in the BFO layers on the MFIS structure. Moreover, the identical intrinsic domain structures—out-of-plane single domain with spontaneous downward polarization—and similar domain switching results were confirmed. This similarity suggests that the initial ferroelectric properties of BFO membranes are independent of the underneath semiconductors.

Typical current density-voltage (*J-V*) curves (Fig. 1, G and H) and resistance-voltage (*R-V*) hysteresis loops (fig. S1) are presented to illustrate the nonvolatile conductance switching in Si-FTJ and GaAs-FTJ devices. By switching the polarization of BFO, both devices demonstrate on and off states, through modulation of the depletion/accumulation region at the BFO/semiconductors (Si and GaAs) interface via the ferroelectric field effect (*27*, *36*, *37*). The ON and OFF resistances were repeatedly validated in 15 different devices for each FTJ, manifesting similar R_{ON}/R_{OFF} ratios greater than 10^3 and indicating high uniformity and reproducibility of these BFO-based FTJs (fig. S2, A and B). In addition, the two devices also feature good retention properties at room temperature and 383 K for a duration up to 10^5 s. Data extrapolation (*38*) also suggests that the retention time exceeds 10 years (fig. S2, C and D). Furthermore, the resistance of the two FTJs can be gradually tuned from the ON state to various nonvolatile intermediate resistance states, demonstrating their memristor-like performance and potential for constructing electrical synapses (fig. S3). Notably, the FTJs based on BFO and BFO/$PbTiO_3$ integrated with Si also exhibit ultrafast (1 ns) memristive switching behaviors in our previous work (*27*). These reliability features provide fundamental insights for using integrated FTJs in reliable nonvolatile memory and advanced computing applications (*2*, *39*).

Fatigue behavior

To gain insight into the resistive fatigue behavior in the Si-FTJ and GaAs-FTJ, we applied periodic bipolar pulse voltages, as shown in the inset of Fig. 2A. This pulse waveform repeatedly flipped the polarization of BFO, enabling the collection of resistance-cycle (*R-N*) curves. On the basis of the *R-V* results, write voltages of −5.5 V/+5 V were selected, resulting in fully saturated switching behavior for the two devices. Setting the pulse duration (t_d) of 300 ns, the saturated R_{OFF}/R_{ON} ratios are well maintained for over 10^5 and 10^7 cycles for the Si-FTJ and GaAs-FTJ devices (Fig. 2A), respectively. After 10^6 and 10^8 cycles, the residual R_{ON}/R_{OFF} ratios are ~4×10^2 and ~10^3 for the Si-FTJ and GaAs-FTJ, respectively. A comparison

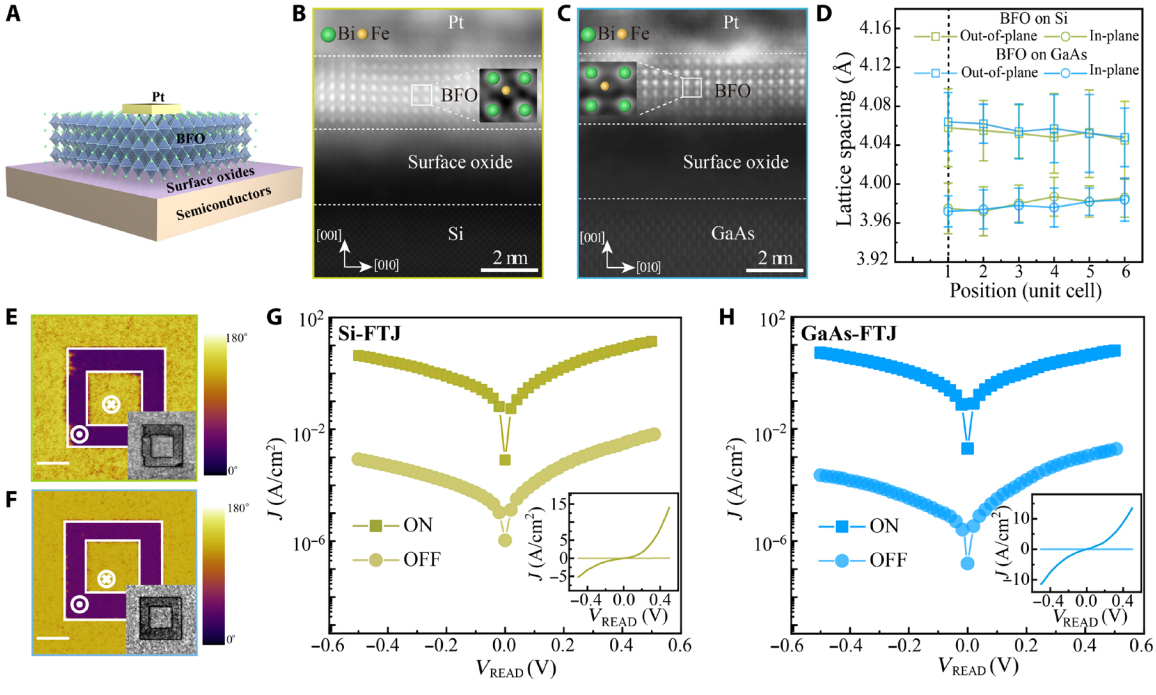

Fig. 1. Structure, ferroelectricity, and electrical characteristics of the BFO membranes integrated on Si and GaAs wafers. (**A**) Schematic illustration of the FTJ structures consisting of the top electrode (Pt), ultrathin BFO membranes, and the bottom conductive semiconductors. Both Si and GaAs substrates exhibit thin surface oxidation layers. Zoom-in HAADF-STEM images showing the stacking structure and atomically sharp interfaces of the Si-FTJ (**B**) and GaAs-FTJ (**C**). (**D**) In-plane and out-of-plane lattice spacing of the two heterostructures. PFM phase images of the Si-FTJ (**E**) and GaAs-FTJ (**F**) taken with ±6-V write voltages are shown, and the insets display the corresponding PFM amplitude. Scale bars, 1 μm. Typical *J-V* curves of Si-FTJ (**G**) and GaAs-FTJ (**H**) devices using pulse voltages (V_p, −5.5 and +5 V) with pulse duration (t_d) of 300 ns show voltage-dependent bipolar switching behavior. Insets show the *J-V* curves on a linear scale.

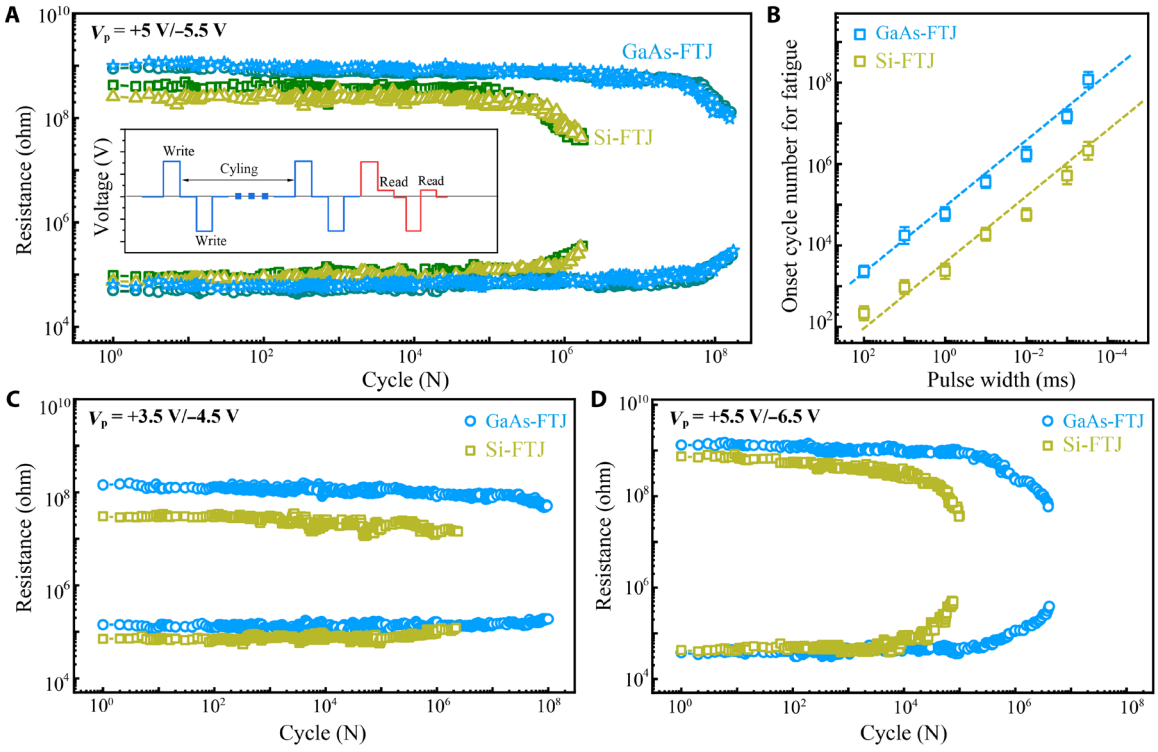

Fig. 2. Resistance fatigue performance of Si-FTJ and GaAs-FTJ. (**A**) Resistance-cycle (*R-N*) curves for the on and off states of the two devices were measured with a pulse width of 300 ns and a read voltage (V_r) of 0.2 V. The inset provides the pulse sequence used in the fatigue measurement process. (**B**) Extracting from the *R-N* curves shown in (A) and figs. S4 and S5, a statistical result of the cycle numbers for the two devices was conducted when the saturation switching ratios decayed to ~10% of the initial R_{ON}/R_{OFF} ratio under various pulse durations. Resistance fatigue of the two devices measured at lower (**C**) and oversaturated (**D**) pulse voltages, demonstrating alleviated and accelerated relaxation of fatigue compared to the saturated cycling behavior in (A).

of relevant performance metrics for the integrated FTJs against those of epitaxial FTJs is demonstrated in table S1. Obviously, under the same conditions, the GaAs-FTJ devices exhibit much better fatigue-resistant performance compared with the Si-FTJ devices. This enhanced fatigue resistance behavior is still observed at various t_d values (figs. S4 and S5) for GaAs-FTJ devices. The onset cycle numbers of electroresistance ratio cycle at different t_d values are summarized and depicted in Fig. 2B, demonstrating a dependency of fatigue on pulse duration. To further evaluate the improved endurance performance of the GaAs-FTJ, we tested different write voltages, all showing notable enhancement over the Si-FTJ (Fig. 2, C and D). In addition, the fatigue phenomenon becomes increasingly pronounced in integrated BFO-based FTJs as the switching voltages increase, differing from the fatigue mechanism primarily by the pinning effect of charged defects at ferroelectric domain walls in HfO_2 and perovskite oxides (*32*, *35*, *40*, *41*). These results also suggest the intrinsic fatigue-resistant properties of the GaAs-FTJ, regardless of pulse width or pulse voltage. Moreover, the influence of BFO thickness on electrical behavior and fatigue performance was investigated (fig. S6), revealing a trade-off between improved fatigue resistance and suppressed FTJ performance (R_{OFF}/R_{ON} ratio) as the ferroelectric layer thickness increases.

Atomic-scale fatigue analysis

To identify the factors that contribute to the resistance fatigue of the Si-FTJ and GaAs-FTJ, we analyze their atomic structures before and after identical endurance testing cycles by HAADF-STEM measurements (Fig. 3). Compared to the initial structures of the two devices (Fig. 3, A and C), the fatigued devices reveal notable alterations in the lattice structures of the BFO layers (Fig. 3, B and D). The damage in the BFO structure can be categorized into two kinds of regions: region I and region II. After fatigue, region I shows a contrast of *A*-site Bi and *B*-site Fe, while region II exhibits noticeable destruction of the local perovskite structures of BFO, causing the contrasts to disappear. The lattice destruction in the Si-FTJ after fatigue is much more pronounced than that in the GaAs-FTJ (Fig. 3B), accounting for its worse fatigue performance. Further structural comparison of the fatigued Si-FTJ and GaAs-FTJ is performed on the basis of low-magnification HAADF images (fig. S7).

Electron energy loss spectroscopy (EELS) spectra of the Fe$L_{2,3}$-edge of the pristine and fatigued states (Fig. 3, E and H) were extracted from the marked regions in Fig. 3 (A to D) to analyze the oxidation state of Fe. The Fe energy loss near-edge structure L_3/L_2 white-line ratio was calculated using the Pearson method (*42*) (fig. S8), with peak positions determined by Gaussian fitting (*43*). A decrease in the Fe valence is observed in fatigued samples, compared with the pristine samples (Fig. 3, F and G). Similar phenomenon has also been observed in the $LaFeO_3/LaTiO_3$ heterojunction interface, accompanied by the formation of oxygen vacancies (*43*). The formation and aggregation of oxygen vacancies are likely due to the ionization effect caused by electron injection from the electrodes and their subsequent migration during electrical cycling. This process weakens the Fe—O chemical bonds and increases the possibility of oxygen ions escaping from the BFO lattices. Consequently, the perovskite BFO lattice distortion becomes distinct and eventually dominates as

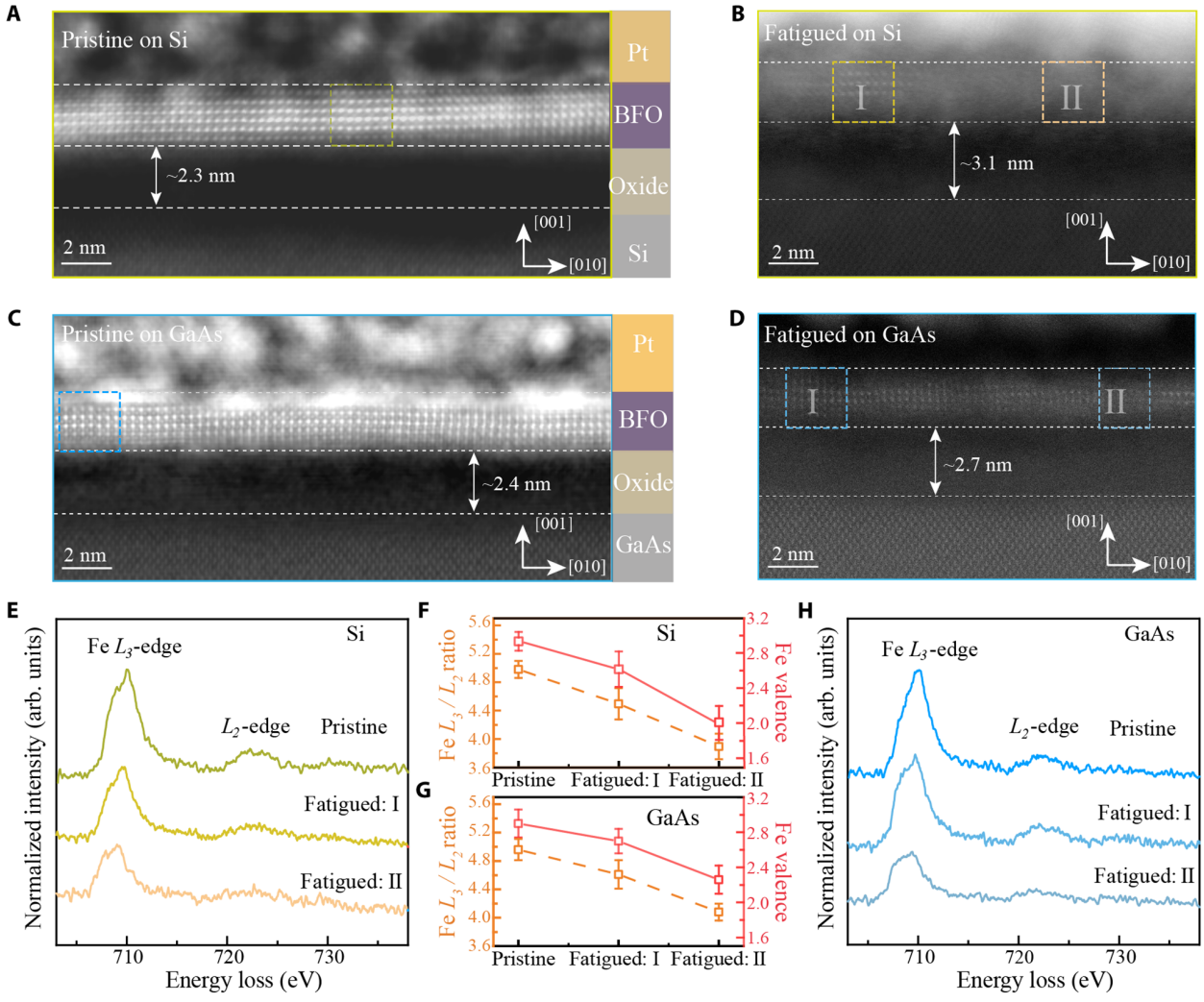

Fig. 3. Atomic structures and Fe ionic valence states in the pristine and fatigued samples. HAADF-STEM images of pristine and fatigued FTJs with BFO barriers integrated on Si (**A** and **B**) and GaAs (**C** and **D**) wafers. In (B) and (D), region I shows the BFO layer with perovskite lattices after fatigue, while region II shows the BFO layer without perovskite lattices after fatigue. EELS spectra of Fe $L_{2,3}$-edges for the pristine states and regions I and II in the fatigued states of Si-FTJ (**E**) and GaAs-FTJ (**H**), respectively. Fe L_3/L_2-edge ratio and Fe valence are extracted from (E) and (H) for Si-FTJ (**F**) and GaAs-FTJ (**G**), respectively. arb. units, arbitrary units.

oxygen deficiency increases. In addition, the reduction of the Fe valence is mainly observed at the bottom layer of the BFO in the two FTJs, as shown in fig. S9. This suggests that oxygen vacancies tend to aggregate at the interface between the BFO and the amorphous oxide layers, likely due to oxygen escape from the BFO bottom layer. Figure 3F shows a more pronounced decrease in the Fe valence state in the fatigued Si-FTJ compared to the fatigued GaAs-FTJ (Fig. 3G), indicating a higher concentration of oxygen vacancies. This greater accumulation of oxygen vacancies suggests a more notable escape of oxygen, which could potentially lead to further oxidation of Si. It is evidenced by the increased thickness of the amorphous oxide layers observed after fatigue testing, with the layer in the Si-FTJ (~3.1 nm) being thicker than that in the GaAs-FTJ (~2.7 nm). Here, the thickness of the amorphous oxide layer is roughly defined on the basis of the lattice boundaries observed in the HAADF images (Fig. 3, A to D). The increased thickness reflects a greater possibility of oxygen escape, which may be attributed to the higher oxygen affinity of silicon compared to gallium and arsenic (*44*, *45*). This results in a larger accumulation of oxygen vacancies and an earlier onset of resistance fatigue in the Si-FTJ. Moreover, to further verify the fatigue mechanism, we performed extended experiments using Ge substrates with a weak oxygen affinity. The saturated R_{OFF}/R_{ON} ratio of the Pt/BFO/GeO_2/Ge-FTJ is well maintained for over 10^7 cycles, as shown in fig. S10, also demonstrating a better fatigue-resistant behavior compared to Si-based FTJ.

By comparing the behavior of the two FTJs in the pristine and fatigued states (Fig. 3, A versus B and C versus D), the fatigue mechanism of the two FTJs with the MFIS structures can be understood as follows: During repetitive cycling, oxygen vacancies accumulate at the bottom interface between BFO and semiconductors, leading to the formation of a ferroelectric dead layer in region II. As cycling continues, the concentration of oxygen vacancies increases, accompanied by a greater escape of oxygen. This phenomenon manifests in microscopic outcomes: a reduction in the Fe valence state and degradation of the perovskite lattice structure. At a macroscopic level, these changes ultimately lead to the degradation of TER performance.

Ferroelectric and domain dynamics characterization

Fatigue-induced variations in ferroelectricity can also be demonstrated by vertical piezoelectric signals in the pristine and fatigued BFO layers (Fig. 4). Before PFM measurements, the top electrode (Pt) is exfoliated to avoid any additional interference from its high ductility. Both fatigued FTJs exhibited flat surface morphologies after electrode removal (Fig. 4, B and D), indicating no obvious damage to the BFO barrier layer. Ferroelectric properties are characterized by collecting PFM hysteresis loops from a 4 by 4 grid of positions within a 5 μm–by–5 μm area. Pristine devices both exhibit 180° phase contrast and typical butterfly-type amplitude loops (Fig. 4, I and K), while the fatigued devices show decreased phase contrast, with loops that are even indistinguishable (Fig. 4, J and L). Spatial distributions of the ferroelectric properties of the BFO layer are illustrated by mapping the phase contrast (ΔPhase) at 4 by 4 grid positions. The pristine BFO barriers are uniform (Fig. 4, E and G), with almost all loops displaying the same blue contrast (180°). In the fatigued GaAs-FTJ, some brown areas appear within the blue contrast (Fig. 4F), whereas in the fatigued Si-FTJ, the blue contrast almost disappears (Fig. 4H). Additional out-of-plane PFM images of the fatigued devices are presented in fig. S11. These observations suggest that the fatigued devices exhibit relatively weak phase contrast, corresponding to the degraded piezoelectric responses. The degradation can be attributed to a loss of ferroelectricity caused by the destruction of the BFO lattices. Moreover, the phase contrast of fatigued BFO/Si (Fig. 4F) is much weaker than that of fatigued BFO/GaAs (Fig. 4H), implying that the piezoelectric response of BFO/Si is lower after endurance cycling.

The fatigue-induced oxygen aggregation, which accompanies ferroelectric degradation, is further reflected in the electrical properties (*46*) of FTJs. The fatigue-induced oxygen aggregation, accompanied ferroelectric degradation, is further reflected in the electrical properties of FTJs. Transport performance and barrier profiles in the pristine and fatigued states are demonstrated in figs. S12 to S16 and text S1. Moreover, the temperature-dependent *I*-*V* and *C*-*V* and low-frequency noise (*47*) characteristics (figs. S13 to S16) are analyzed to reveal the tunneling model and transport mechanism. In comparison to the pristine FTJs, 1/*f* noise behavior (*47*) is observed in the fatigued FTJs (fig. S16), arising from the accumulated defects in the BFO and accompanied by a transition in the conduction mechanism. In the fatigued devices, the reduced effective polarization of BFO weakens the ferroelectric modulation of the barrier, leading to decreased contrast between on and off states (fig. S12, C to F). In comparison with the fatigued Si-FTJ, GaAs-FTJ demonstrates stronger ferroelectric modulation of the barrier height and width after fatigue, thus having enhanced fatigue resistance characteristics.

To further comprehensively understand the switching mechanism in the pristine and fatigued samples, we investigated ferroelectric

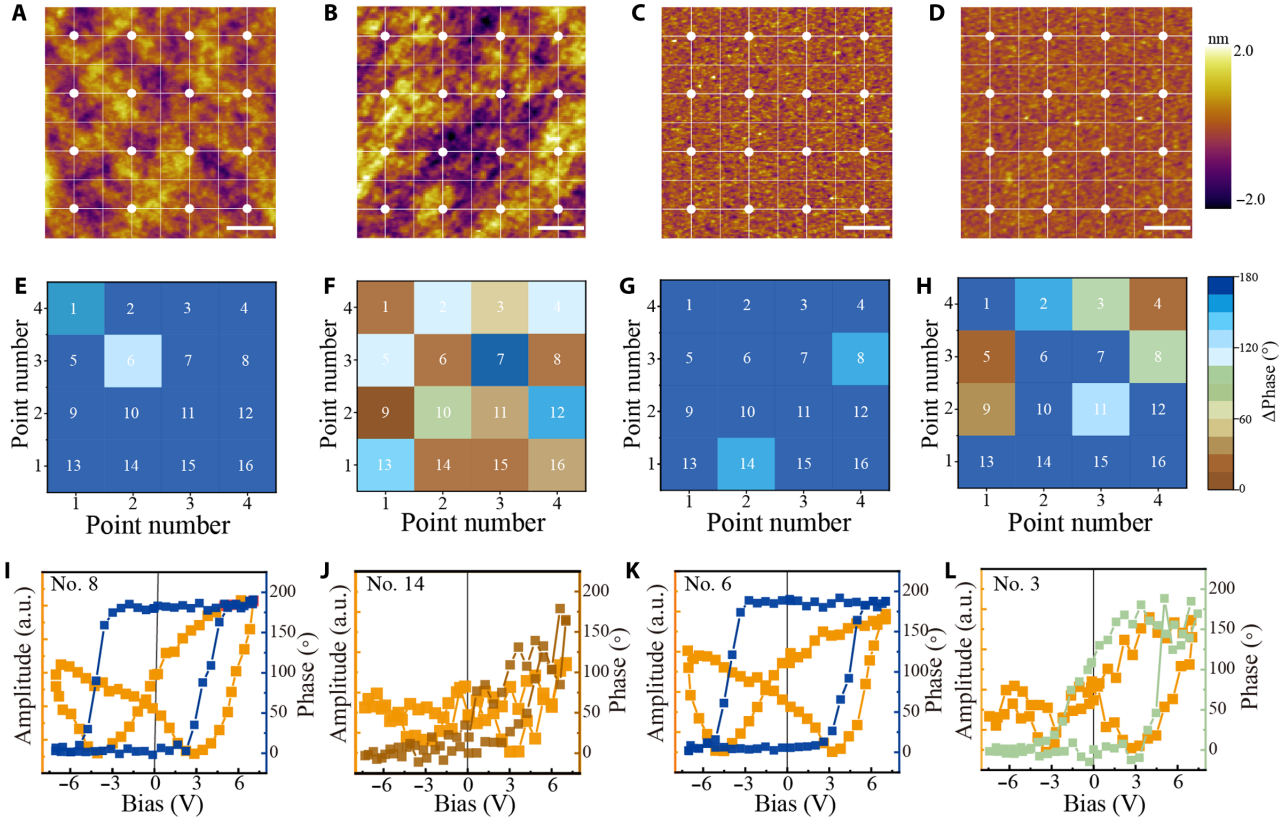

Fig. 4. Ferroelectric properties observed in the pristine and fatigued samples. Atomic force microscope topography images of the Si-FTJ and GaAs-FTJ in pristine (**A** and **C**) and fatigued (**B** and **D**) states, respectively. Note that the topography images of fatigued samples [(B) and (D)] show exfoliation. Scale bars, 1 μm. Phase contrast mappings of the PFM hysteresis loops extracted at 16 array points on the BFO for Si-FTJ (**E** and **F**) and GaAs-FTJ (**G** and **H**) in the pristine and fatigued samples. The color bar represents ΔPhase that is confirmed at the bias of 0 V. Typical PFM hysteresis loops of the two FTJs in pristine and fatigued states, corresponding to the color mappings [(E) to (H)] of (**I**) ~180°, (**J**) ~20° (**K**) ~180°, and (**L**) ~100° for ΔPhase, respectively. a.u., arbitrary units.

domain dynamic behaviors (Fig. 5 and fig. S17) and the temperature-dependent properties of domain switching (fig. S18). The direct relationship between the junction resistance (R) and the normalized reversed area (S), where S represents the area fraction of the downward to upward ferroelectric domain states, is described using a simple parallel resistance model (*12*, *48*), $1/R = 1 - S/R_{ON} + S/R_{OFF}$. We plot ($S$) as a function of the cumulative pulse duration for both pristine (fig. S17, A and C) and fatigued (Fig. 5, A and C) FTJs. In addition, the distributions of switching period at different voltages, extracted from the S-t curves using the nucleation-limited switching (NLS) model (*49*, *50*) (see Methods), reflect domain nucleation and growth characteristics in the pristine and fatigued BFO layers. In both fatigued samples (Fig. 5, B and D), the mean switching time (t_{mean}) increases, and the distributions become broader compared to pristine samples (fig. S17, B and D) at the same write voltage, likely due to the aggregation of oxygen vacancies that hinder domain switching (*31*).

Notable differences in distribution, switching time, and saturable reversal voltage have been observed between two fatigued devices. For instance, at 5.5 V, the Si-FTJ displays a mean switching time (t_{mean}) of ~1.95×10^{-7} s with a broader distribution (Fig. 5B), whereas the GaAs-FTJ demonstrates a faster t_{mean} of ~7.8×10^{-8} s with a sharper distribution (Fig. 5D). At 6.2 V, GaAs-FTJ achieves a sharp distribution, whereas Si-FTJ requires a higher voltage of 7 V to achieve a similar effect. This difference is attributed to the higher concentration of charged oxygen vacancies in the Si-FTJ, necessitating stronger electrical stimulation to disperse accumulated charges and release blocked domains (*31*). The increased lattice collapse of Si-FTJ also implies that nucleation and growth are more challenging during domain reversal, resulting in longer switching times and higher activation fields. According to Merz's law, $t_{mean} \propto \exp(-E_a/E)$ (*51*), the fatigued GaAs-FTJ exhibits a lower activation field of 3.85 V/nm compared to the 4.94 V/nm in fatigued Si-FTJ (Fig. 5, B and D, insets). This indicates that the Si-FTJ requires more energy for domain flipping, consistent with the blocked switching due to increased defect accumulation.

DISCUSSION

Fatigue behavior and underlying mechanism in oxide-based FTJs integrated with Si and GaAs were systematically demonstrated and analyzed. Microstructural analysis reveals that the fatigue performance can be attributed to the accumulation of oxygen vacancies at the BFO/semiconductor interface during repetitive switching. The accumulation results in the local destruction of perovskite lattice and a reduction in effective polarization. Moreover, compared to Si-FTJ, GaAs-FTJ exhibits much better fatigue-resistant characteristics due to the lower lattice destruction and ferroelectric loss. This advantage arises from the weaker interactions between oxygen and gallium/arsenic, which lead to a lower accumulation of oxygen vacancies and minimize structural damage during endurance cycling. These results reveal the atomic-scale fatigue mechanisms in integrated FTJs and provide valuable insights for developing fatigue-resistant oxide FTJs, thereby enhancing the prospects of oxide integration on semiconductors. These findings also provide useful insights for the development

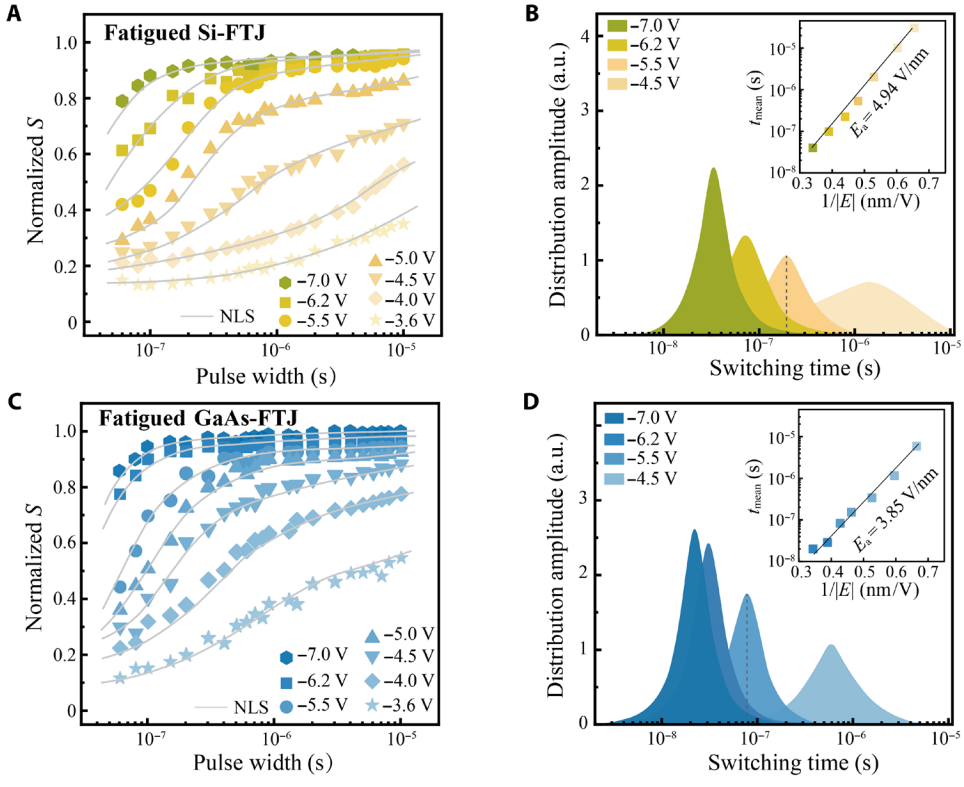

Fig. 5. Ferroelectric domain switching characteristics of the two fatigued FTJs. Relative area fraction (S) versus pulse width and voltage for the fatigued Si-FTJ (**A**) and fatigued GaAs-FTJ (**C**). The solid lines represent fits using the NLS model (see Methods). Lorentzian distribution of switching times is extracted from the fits in (A) and (C) under various switching voltages. Results are shown in (**B**) for the fatigued Si-FTJ and in (**D**) for the fatigued GaAs-FTJ. Insets illustrate the evolution of the mean switching time (t_{mean}) as a function of the inverse electric field (1/|E|), with solid lines representing the fitting results according to Merz's law (*48*, *50*).

of other ferroelectric-based devices, such as ferroelectric field effect transistors, on semiconductor platforms.

METHODS

Device preparation

The 6–unit cell–thick BFO thin films were epitaxially grown on a (001)-oriented $SrTiO_3$ (STO) single-crystalline substrate with a water-soluble $Sr_3Al_2O_6$ (SAO) layer using oxide molecular beam epitaxy. Before deposition, the STO substrates were treated with an hydrofluoric acid (HF) buffer solution and then annealed at 1000°C for 80 min in an O_2 atmosphere to achieve a TiO_2-terminated step-terrace surface. The SAO film was deposited at 850°C and an O_2 pressure at 1×10^{-6} torr. The BFO film was deposited at 480°C and an O_3 pressure at 3×10^{-8} torr. In addition, the transfer method of the obtained free-standing BFO membranes from oxide substrates to the semiconductors was presented in the previous report (*27*). Before the transfer, the surface of Si (≤0.01 ohm·cm) was cleaned using a wet chemical cleaning process, followed by the application of a buffer solution (1:10 HF:H_2O) to eliminate the surface oxide layers. The GaAs (≤0.01 ohm·cm) underwent a similar cleaning process to ensure surface cleanliness. Subsequently, the transfer process of transferring BFO to semiconductor substrates occurred in glove box under an Ar gas atmosphere. A circular Pt top electrode array with a diameter of ~20 μm and a thickness of ~30 nm was deposited on the BFO surface by sputtering through a shadow mask to form the FTJ devices.

Characterizations

Cross-sectional samples were fabricated using a focused ion beam technique with the Helios G4 UX (Thermo Fisher Scientific) dual-beam system. HAADF images were obtained using a double spherical aberration-corrected STEM/TEM FEI Titan3 G2 60-300 microscope at 300 kV with a Super-X EDS system. The EELS spectra were collected with an energy dispersion of 0.25 eV per channel. Surface topographies and room-temperature ferroelectric properties were measured using an Asylum Research MFP-3D Infinity atomic force microscope. The PFM hysteresis loops were collected in the DART (dual ac resonance tracking) mode with triangle pulse waveform applied to the probe using conductive Pt/Ir-coated Si cantilevers (NanoWorld EFM). The resistance switching and fatigue performance of the two FTJs were characterized using the Keithley 2400 source meter and Keithley 4200-SCS semiconductor characterization system with a 4225-PMU module at room temperature in a Cascade Summit 11000B-M probe station. The testing pulse was applied to the top electrode Pt, while the semiconductors acting as the bottom electrode were always grounded.

Ferroelectric domain switching dynamics

The area fraction (S) versus t curves of ferroelectric switching follow the NLS (*49*, *50*). In this model, resistive switching is considered to be inhomogeneous across different regions, and the switching kinetics can be described in terms of the distribution function of the nucleation probabilities in these areas (*49*, *50*). The NLS model with a broad Lorentzian distribution of the logarithm of switching time (t_{sw}) is formulated as follows (*48*, *50*)

$$F(\log t_{sw}) = \frac{S_i}{\pi}\left[\frac{w}{(\log t_{sw} - \log t_{mean})^2 + w^2}\right] \quad (1)$$

Here, S_i is a normalized constant, t_{mean} is the mean switching time, and w and $\log t_{mean}$ denote the half-peak width and center of the Lorentzian distribution, respectively. The normalized summed switched area S can be expressed as follow (*12*, *48*)

$$S = \sum_{i=1}^{2} S_i\left(\frac{1}{2} + \frac{1}{\pi}\arctan\frac{\log t_d - \log t^i_{mean}}{w_i}\right) \quad (2)$$

Supplementary Materials

This PDF file includes:

Supplementary Text S1
Figs. S1 to S18
Table S1
References

REFERENCES AND NOTES

1. D. Ielmini, H.-S. P. Wong, In-memory computing with resistive switching devices. *Nat. Electron.* **1**, 333–343 (2018).
2. W. Zhang, B. Gao, J. Tang, P. Yao, S. Yu, M.-F. Chang, H.-J. Yoo, H. Qian, H. Wu, Neuro-inspired computing chips. *Nat. Electron.* **3**, 371–382 (2020).
3. M. A. Zidan, J. P. Strachan, W. D. Lu, The future of electronics based on memristive systems. *Nat. Electron.* **1**, 22–29 (2018).
4. Q. Xia, J. J. Yang, Memristive crossbar arrays for brain-inspired computing. *Nat. Mater.* **18**, 309–323 (2019).
5. M. Hu, C. E. Graves, C. Li, Y. Li, N. Ge, E. Montgomery, N. Davila, H. Jiang, R. S. Williams, J. J. Yang, Q. Xia, J. P. Strachan, Memristor-based analog computation and neural network classification with a dot product engine. *Adv. Mater.* **30**, 1705914 (2018).
6. V. Garcia, S. Fusil, K. Bouzehouane, S. Enouz-Vedrenne, N. D. Mathur, A. Barthélémy, M. Bibes, Giant tunnel electroresistance for non-destructive readout of ferroelectric states. *Nature* **460**, 81–84 (2009).
7. A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthélémy, J. Grollier, A ferroelectric memristor. *Nat. Mater.* **11**, 860–864 (2012).
8. A. Chanthbouala, A. Crassous, V. Garcia, K. Bouzehouane, S. Fusil, X. Moya, J. Allibe, B. Dlubak, J. Grollier, S. Xavier, C. Deranlot, A. Moshar, R. Proksch, N. D. Mathur, M. Bibes, A. Barthélémy, Solid-state memories based on ferroelectric tunnel junctions. *Nat. Nanotechnol.* **7**, 101–104 (2012).
9. V. Garcia, M. Bibes, Ferroelectric tunnel junctions for information storage and processing. *Nat. Commun.* **5**, 4289 (2014).
10. Z. Wen, D. Wu, Ferroelectric tunnel junctions: Modulations on the potential barrier. *Adv. Mater.* **32**, 1904123 (2020).
11. J. Li, N. Li, C. Ge, H. Huang, Y. Sun, P. Gao, M. He, C. Wang, G. Yang, K. Jin, Giant electroresistance in ferroionic tunnel junctions. *iScience* **16**, 368–377 (2019).
12. C. Ma, Z. Luo, W. Huang, L. Zhao, Q. Chen, Y. Lin, X. Liu, Z. Chen, C. Liu, H. Sun, X. Jin, Y. Yin, X. Li, Sub-nanosecond memristor based on ferroelectric tunnel junction. *Nat. Commun.* **11**, 1439 (2020).
13. Z. Luo, Z. Wang, Z. Guan, C. Ma, L. Zhao, C. Liu, H. Sun, H. Wang, Y. Lin, X. Jin, Y. Yin, X. Li, High-precision and linear weight updates by subnanosecond pulses in ferroelectric tunnel junction for neuro-inspired computing. *Nat. Commun.* **13**, 699 (2022).
14. S. Salahuddin, K. Ni, S. Datta, The era of hyper-scaling in electronics. *Nat. Electron.* **1**, 442–450 (2018).
15. A. Sebastian, M. Le Gallo, R. Khaddam-Aljameh, E. Eleftheriou, Memory devices and applications for in-memory computing. *Nat. Nanotechnol.* **15**, 529–544 (2020).
16. Y. Liu, X. Duan, H.-J. Shin, S. Park, Y. Huang, X. Duan, Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
17. K.-H. Kim, I. Karpov, R. H. Olsson III, D. Jariwala, Wurtzite and fluorite ferroelectric materials for electronic memory. *Nat. Nanotechnol.* **18**, 422–441 (2023).
18. J. Shim, S.-H. Bae, W. Kong, D. Lee, K. Qiao, D. Nezich, Y. J. Park, R. Zhao, S. Sundaram, X. Li, H. Yeon, C. Choi, H. Kum, R. Yue, G. Zhou, Y. Ou, K. Lee, J. Moodera, X. Zhao, J.-H. Ahn, C. Hinkle, A. Ougazzaden, J. Kim, Controlled crack propagation for atomic precision handling of wafer-scale two-dimensional materials. *Science* **362**, 665–670 (2018).
19. R. A. McKee, F. J. Walker, M. F. Chisholm, Crystalline oxides on silicon: The first five monolayers. *Phys. Rev. Lett.* **81**, 3014–3017 (1998).
20. S. R. Bakaul, C. R. Serrao, M. Lee, C. W. Yeung, A. Sarker, S.-L. Hsu, A. K. Yadav, L. Dedon, L. You, A. I. Khan, J. D. Clarkson, C. Hu, R. Ramesh, S. Salahuddin, Single crystal functional oxides on silicon. *Nat. Commun.* **7**, 10547 (2016).
21. D. Lu, D. J. Baek, S. S. Hong, L. F. Kourkoutis, Y. Hikita, H. Y. Hwang, Synthesis of freestanding single-crystal perovskite films and heterostructures by etching of sacrificial water-soluble layers. *Nat. Mater.* **15**, 1255–1260 (2016).

22. D. Ji, S. Cai, T. R. Paudel, H. Sun, C. Zhang, L. Han, Y. Wei, Y. Zang, M. Gu, Y. Zhang, W. Gao, H. Huyan, W. Guo, D. Wu, Z. Gu, E. Y. Tsymbal, P. Wang, Y. Nie, X. Pan, Freestanding crystalline oxide perovskites down to the monolayer limit. *Nature* **570**, 87–90 (2019).
23. H. Sun, J. Wang, Y. Wang, C. Guo, J. Gu, W. Mao, J. Yang, Y. Liu, T. Zhang, T. Gao, H. Fu, T. Zhang, Y. Hao, Z. Gu, P. Wang, H. Huang, Y. Nie, Nonvolatile ferroelectric domain wall memory integrated on silicon. *Nat. Commun.* **13**, 4332 (2022).
24. L. Han, C. Addiego, S. Prokhorenko, M. Wang, H. Fu, Y. Nahas, X. Yan, S. Cai, T. Wei, Y. Fang, H. Liu, D. Ji, W. Guo, Z. Gu, Y. Yang, P. Wang, L. Bellaiche, Y. Chen, D. Wu, Y. Nie, X. Pan, High-density switchable skyrmion-like polar nanodomains integrated on silicon. *Nature* **603**, 63–67 (2022).
25. D. Lu, S. Crossley, R. Xu, Y. Hikita, H. Y. Hwang, Freestanding oxide ferroelectric tunnel junction memories transferred onto silicon. *Nano Lett.* **19**, 3999–4003 (2019).
26. M. Abuwasib, C. R. Serrao, L. Stan, S. Salahuddin, S. R. Bakaul, Tunneling electroresistance effects in epitaxial complex oxides on silicon. *Appl. Phys. Lett.* **116**, 032902 (2020).
27. N. Zheng, Y. Zang, J. Li, C. Shen, P. Jiao, L. Zhang, H. Wang, L. Han, Y. Liu, W. Ding, X. Yang, L. Nian, J. Ma, X. Jiang, Y. Yin, Y. Xia, Y. Deng, D. Wu, X. Li, X. Pan, Y. Nie, Perovskite-oxide-based ferroelectric synapses integrated on silicon. *Adv. Funct. Mater.* **34**, 2316473 (2024).
28. Z.-D. Luo, J. J. P. Peters, A. M. Sanchez, M. Alexe, Flexible memristors based on single-crystalline ferroelectric tunnel junctions. *ACS Appl. Mater. Interfaces* **11**, 23313–23319 (2019).
29. S. Boyn, S. Girod, V. Garcia, S. Fusil, S. Xavier, C. Deranlot, H. Yamada, C. Carretero, E. Jacquet, M. Bibes, A. Barthelemy, J. Grollier, High-performance ferroelectric memory based on fully patterned tunnel junctions. *Appl. Phys. Lett.* **104**, 052909 (2014).
30. A. V. Ievlev, S. Kc, R. K. Vasudevan, Y. Kim, X. Lu, M. Alexe, V. R. Cooper, S. V. Kalinin, O. S. Ovchinnikova, Non-conventional mechanism of ferroelectric fatigue via cation migration. *Nat. Commun.* **10**, 3064 (2019).
31. Y. Yang, M. Wu, X. Zheng, C. Zheng, J. Xu, Z. Xu, X. Li, X. Lou, D. Wu, X. Liu, S. J. Pennycook, Z. Wen, Atomic-scale fatigue mechanism of ferroelectric tunnel junctions. *Sci. Adv.* **7**, eabh2716 (2022).
32. K.-Y. Chen, P.-H. Chen, R.-W. Kao, Y.-X. Lin, Y.-H. Wu, Impact of plasma treatment on reliability performance for $HfZrO_x$-based metal-ferroelectric-metal capacitors. *IEEE Electron Device Lett.* **39**, 87–90 (2017).
33. S. S. Fields, S. W. Smith, P. J. Ryan, S. T. Jaszewski, I. A. Brummel, A. Salanova, G. Esteves, S. L. Wolfley, M. D. Henry, P. S. Davids, J. F. Ihlefeld, Phase-exchange-driven wake-up and fatigue in ferroelectric hafnium zirconium oxide films. *ACS Appl. Mater. Interfaces* **12**, 26577–26585 (2020).
34. N. Feng, H. Li, B. Peng, F. Zhang, P. Cai, L. Zhang, R. Wang, R. Huang, Metal–ferroelectric–semiconductor tunnel junction: Essential physics and design explorations. *IEEE Trans. Electron Devices* **70**, 3382–3389 (2023).
35. B. Zeng, S. Xie, S. Zhang, H. Huang, C. Ju, S. Zheng, Q. Peng, Q. Yang, Y. Zhou, M. Liao, Polarization fatigue mechanism of laminated hafnium zirconium oxide ferroelectric thin films. *Acta Mater.* **272**, 119920 (2024).
36. P. Chang, G. Du, J. Kang, X. Liu, Conduction mechanisms of metal-ferroelectric- insulator-semiconductor tunnel junction on N- and P-type semiconductor. *IEEE Electron Device Lett.* **42**, 118–121 (2021).
37. K. Lee, J. Byun, K. Park, S. Kang, M. S. Song, J. Park, J. Lee, S. C. Chae, Giant tunneling electroresistance in epitaxial ferroelectric ultrathin films directly integrated on Si. *Appl. Mater. Today* **26**, 101308 (2022).
38. Z. Wen, C. Li, D. Wu, A. Li, N. Ming, Ferroelectric-field-effect-enhanced electroresistance in metal/ferroelectric/semiconductor tunnel junctions. *Nat. Mater.* **12**, 617–621 (2013).
39. L. Zhao, H. Fang, J. Wang, F. Nie, R. Li, Y. Wang, L. Zheng, Ferroelectric artificial synapses for high-performance neuromorphic computing: Status, prospects, and challenges. *Appl. Phys. Lett.* **124**, 030501 (2024).
40. A. K. Tagantsev, I. Stolichnov, E. L. Colla, N. Setter, Polarization fatigue in ferroelectric films: Basic experimental findings, phenomenological scenarios, and microscopic features. *J. Appl. Phys.* **90**, 1387–1402 (2001).
41. J. Glaum, M. Hoffman, Electric fatigue of lead-free piezoelectric materials. *J. Am. Ceram. Soc.* **97**, 665–680 (2014).
42. D. H. Pearson, C. C. Ahn, B. Fultz, White lines and *d*-electron occupancies for the 3*d* and 4*d* transition metals. *Phys. Rev. B* **47**, 8471–8478 (1993).
43. C. Gu, M. Gu, C. Zhang, Z. Yuan, Z. Gu, J. Zhou, Y. Nie, P. Wang, X. Pan, Atomic-resolution study of charge transfer effects at the $LaTiO_3/LaFeO_3$ interface. *Phys. Rev. B* **104**, 085115 (2021).
44. H. Li, J. Robertson, Germanium oxidation occurs by diffusion of oxygen network interstitials. *Appl. Phys. Lett.* **110**, 222902 (2017).
45. M. Fleischer, W. Hanrieder, H. Meixner, Stability of semiconducting gallium oxide thin films. *Thin Solid Films* **190**, 93–102 (1990).
46. Q. Zhang, X. He, J. Shi, N. Lu, H. Li, Q. Yu, Z. Zhang, L.-Q. Chen, B. Morris, Q. Xu, P. Yu, L. Gu, K. Jin, C.-W. Nan, Atomic-resolution imaging of electrically induced oxygen vacancy migration and phase transformation in $SrCoO_{2.5-\sigma}$. *Nat. Commun.* **8**, 104 (2017).
47. W. Shin, K. K. Min, J. H. Bae, J. Yim, D. Kwon, Y. Kim, J. Yu, J. Hwang, B. G. Park, D. Kwon, J. H. Lee, Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy. *Nanoscale* **14**, 2177–2185 (2022).
48. S. Boyn, J. Grollier, G. Lecerf, B. Xu, N. Locatelli, S. Fusil, S. Girod, C. Carrétéro, K. Garcia, S. Xavier, J. Tomas, L. Bellaiche, M. Bibes, A. Barthélémy, S. Saïghi, V. Garcia, Learning through ferroelectric domain dynamics in solid-state synapses. *Nat. Commun.* **8**, 14736 (2017).
49. A. K. Tagantsev, I. Stolichnov, N. Setter, J. S. Cross, M. Tsukada, Non-Kolmogorov-Avrami switching kinetics in ferroelectric thin films. *Phys. Rev. B* **66**, 214109 (2002).
50. J. Y. Jo, H. S. Han, J.-G. Yoon, T. K. Song, S.-H. Kim, T. W. Noh, Domain switching kinetics in disordered ferroelectric thin films. *Phys. Rev. Lett.* **99**, 267602 (2007).
51. W. J. Merz, Domain formation and domain wall motions in ferroelectric $BaTiO_3$ single crystals. *Phys. Rev.* **95**, 690–698 (1954).
52. F.-C. Chiu, A review on conduction mechanisms in dielectric films. *Adv. Mater. Sci. Eng.* **2014**, 578168 (2014).
53. A. Gruverman, D. Wu, H. Lu, Y. Wang, H. W. Jang, C. M. Folkman, M. Y. Zhuravlev, D. Felker, M. Rzchowski, C. B. Eom, E. Y. Tsymbal, Tunneling electroresistance effect in ferroelectric tunnel junctions at the nanoscale. *Nano Lett.* **9**, 3539–3543 (2009).
54. Z. Xi, J. Ruan, C. Li, C. Zheng, Z. Wen, J. Dai, A. Li, D. Wu, Giant tunnelling electroresistance in metal/ferroelectric/semiconductor tunnel junctions by engineering the Schottky barrier. *Nat. Commun.* **8**, 15217 (2017).

Acknowledgments

Funding: This work was supported by the National Natural Science Foundation of China (12434002, U24A2011, 12274202) and National Key R&D Program of China (2022YFA1402502 and 2021YFA1400400). H.S. acknowledges the China National Postdoctoral Program for Innovative Talents (grant no. BX20230152) and the China Postdoctoral Science Foundation (grant no. 2024 M751368) and the Natural Science Foundation of Jiangsu Province (No. BK20241189). Y.N. acknowledges the Natural Science Foundation of Jiangsu Province (No. BK20233001). Y.Z. acknowledges the Natural Science Foundation of Education Department of Anhui Province-key project (2024AH050082). **Author contributions:** Writing—original draft: N.Z., H.S., and Y.N. Conceptualization: N.Z., D.W., and Y.N. Investigation: N.Z., J.L., Y.Z., P.J., Y.D., and Y.N. Writing—review and editing: N.Z., H.S., D.W., and Y.N. Methodology: N.Z., J.L., Y.Z., and Y.N. Resources: N.Z., J.L., H.S., Y.Z., and Y.N. Funding acquisition: H.S., Y. D., D.W., and Y.N. Data curation: N.Z., J.L., P.J., C.S., D.W., Y.D., and Y.N. Validation: N.Z., J.L., H.S., Y.Z., P.J., C.S., X.J., X.P., Y.D., D.W., Y.X., and Y.N. Supervision: N.Z., Y.D., D.W., and Y.N. Formal analysis: N.Z., J.L., H.S., Y.D., D.W., and Y.N. Software: N.Z., J.L., P.J., C.S., D.X., Y.D., D.W., and Y.N. Project administration: H.S., D.W., Y. D., and Y.N. Visualization: N.Z., J.L., H.S., Y.Z., X.J., Y.D., D.W., and Y.N. **Competing interests:** The authors declare that they have no competing interests. **Data and materials availability:** All data needed to evaluate the conclusions in the paper are present in the paper and/or the Supplementary Materials.

Submitted 6 August 2024
Accepted 7 March 2025
Published 11 April 2025
10.1126/sciadv.ads0724