



Article

A Tunable-Gain Transimpedance Amplifier for CMOS-MEMS Resonators Characterization

Rafel Perelló-Roig ^{1,2}, Jaume Verd ^{1,2,*} , Sebastià Bota ^{1,2} and Jaume Segura ^{1,2}

¹ Electronic Systems Group (GSE-UIB), University of the Balearic Islands, 07122 Palma, Spain; rafel.perello@uib.es (R.P.-R.); sebastia.bota@uib.es (S.B.); jaume.segura@uib.es (J.S.)

² Health Research Institute of the Balearic Islands, IdISBa, 07010 Palma, Spain

* Correspondence: jaume.verd@uib.es; Tel.: +34-971-172006

Abstract: CMOS-MEMS resonators have become a promising solution thanks to their miniaturization and on-chip integration capabilities. However, using a CMOS technology to fabricate microelectromechanical system (MEMS) devices limits the electromechanical performance otherwise achieved by specific technologies, requiring a challenging readout circuitry. This paper presents a transimpedance amplifier (TIA) fabricated using a commercial 0.35- μm CMOS technology specifically oriented to drive and sense monolithically integrated CMOS-MEMS resonators up to 50 MHz with a tunable transimpedance gain ranging from 112 dB to 121 dB. The output voltage noise is as low as 225 nV/Hz^{1/2}—input-referred current noise of 192 fA/Hz^{1/2}—at 10 MHz, and the power consumption is kept below 1-mW. In addition, the TIA amplifier exhibits an open-loop gain independent of the parasitic input capacitance—mostly associated with the MEMS layout—representing an advantage in MEMS testing compared to other alternatives such as Pierce oscillator schemes. The work presented includes the characterization of three types of MEMS resonators that have been fabricated and experimentally characterized both in open-loop and self-sustained configurations using the integrated TIA amplifier. The experimental characterization includes an accurate extraction of the electromechanical parameters for the three fabricated structures that enables an accurate MEMS-CMOS circuitry co-design.

Keywords: transimpedance amplifier; RF MEMS; oscillator; CMOS-MEMS



Citation: Perelló-Roig, R.; Verd, J.; Bota, S.; Segura, J. A Tunable-Gain Transimpedance Amplifier for CMOS-MEMS Resonators Characterization. *Micromachines* **2021**, *12*, 82. <https://doi.org/10.3390/mi12010082>

Received: 30 December 2020

Accepted: 12 January 2021

Published: 15 January 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Microelectromechanical systems (MEMS) resonators are becoming more and more used nowadays for RF and sensing applications. The use of these devices as the frequency-determining element in an oscillator circuit is a common demand in RF signal processing systems, leading to a reduction in area and power consumption [1]. Thanks to their small size and miniaturization capabilities, MEMS elements can prevent the use of discrete elements such as inductors and quartz crystals [2–5]. On the other hand, system-on-chip applications demand the integration of not only the MEMS signal conditioning circuitry, but also the electronics required to drive the mechanical system at resonance while continuously tracking its resonant frequency [6]. In this sense, the use of an oscillator circuit has additional advantages given its inherent capability of providing a pseudo-digital output signal rather than an analog one.

Various approaches can be found in the literature to implement resonators. It has been proven that resonant MEMS structures can be fabricated using standard CMOS processes combined with surface micromachining [1,6–11]. This approach enables the possibility of developing monolithically integrated systems that use electrostatic actuation and capacitive readout to drive and sense, respectively. the motion of a mechanical resonator, with benefits in terms of area reduction and noise performance.

However, when using CMOS technology, both the materials available to fabricate the MEMS structures as well as the technological design rules to define the MEMS sizes

limit the electromechanical performance [10,12,13]. In the case of resonators, the scaling-down trend in the new generation of MEMS usually results in a reduction of the coupling capacitance between the moving structure and the sense electrode (C_{sense}), an increase in the resonant frequency, and a decrease in the quality factor. In addition, the maximum DC voltage (V_{dc}) applied between the moving and the fixed electrodes is limited by the pull-in voltage, or in any case, by the resonator linear operation range. As a consequence, the capacitive signal current, I_{sig} , injected in the sense electrode,

$$I_{sig} = V_{dc} \frac{\partial C_{sense}}{\partial t}, \quad (1)$$

is reduced to very low values. A transimpedance amplifier (TIA) with large gain and small input-referred noise, is typically used to convert I_{sig} to a voltage feed at subsequent stages [14]. This voltage is often applied back to the resonator input with appropriate gain and phase to generate self-excited oscillations operating as parallel or series oscillators [6,8].

From these considerations, the motivation of this work is to develop a transimpedance amplifier suitable to drive monolithically integrated capacitive CMOS-MEMS resonators operating up to ~ 50 MHz and exhibiting large transimpedance gain (in the range of $10^6 \text{ V}\cdot\text{A}^{-1}$) with a neglectable dependence on C_{sense} . The last provides a reliable tool for an accurate experimental characterization of MEMS resonators in the design stage, which might present an unknown or hard-to-predict equivalent parasitic capacitance value at the sense node, mostly associated with the MEMS resonator layout [15]. Thus, achieving a transimpedance gain independent of the fabricated structure is helpful for completing an accurate design and further parameter extraction during the redesign iterations accomplished to optimize the CMOS-MEMS required performance.

In this work, three MEMS resonators comprehending a broad range of dimensions (Figure 1) were designed, fabricated, and experimentally characterized by the addressed TIA amplifier obtaining its electromechanical parameters and comparing them with a theoretical model. Section 2 of this paper is devoted to the TIA amplifier, the theoretical model for the resonators is presented in Section 3, and the fabrication process is addressed in Section 4. Finally, Section 5 shows the experimental data collected and a summary of the work, and final conclusions and are given in Section 6.

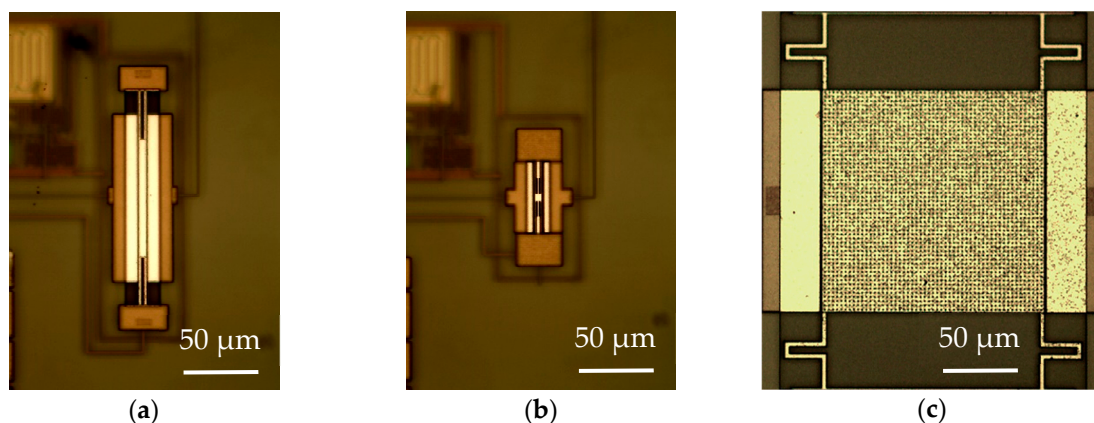


Figure 1. Optical image of the fabricated microelectromechanical system (MEMS) resonators: (a) PR1; (b) PR2; (c) PR3.

2. Transimpedance Amplifier

A transresistance amplifier uses a resistor (passive or active) as the primary gain element to convert the MEMS capacitive current into a voltage. For high transresistance gains, the oscillator noise performance is usually quite poor and is dominated by the input resistor noise [10,16,17]. Thus, the two main types of CMOS oscillator topologies that have found practical applicability to MEMS resonators are the TIA-based oscillator [17] and the Pierce oscillator [18–21]. The TIA circuit converts the input current I_{sig} into an output

voltage V_o that is used to self-excite the MEMS based oscillator circuit. The main challenge when designing a resonator-based oscillator is the quite large resonator-equivalent motional resistance R_M (the circuit oscillates as long as the forward gain of the TIA overcomes the resonator series loss represented by R_M).

The other alternative, the Pierce oscillator [18], uses a capacitive input to integrate the current from the resonator and convert it into a voltage at the sense node. The Pierce circuit topology is, in general, superior in terms of the oscillator noise figure since it exhibits an extremely high input-impedance [22,23]. Thus, the gain is provided by a noiseless capacitive input element rather than a lossy resistive element. One of the drawbacks of the Pierce oscillator topology is its inherent dependence of the open-loop gain with the parasitic capacitance C_p at the sense node. This drawback does not represent a real limitation when the design is customized for a well-known resonator working under adequate operating conditions but lacks in versatility to deal with resonators with different characteristics since its contribution to C_p is hard to accurately estimate from the resonator layout. Moreover, they are difficult to interface with high-impedance MEMS devices [17]. Figure 2 illustrates the expected dependence of the transimpedance gain vs. the parasitic capacitance C_p for a both the TIA with capacitive feedback [17] like the one designed in this work and the behavior of the well-known dependence shown for a Pierce-based topology amplifier.

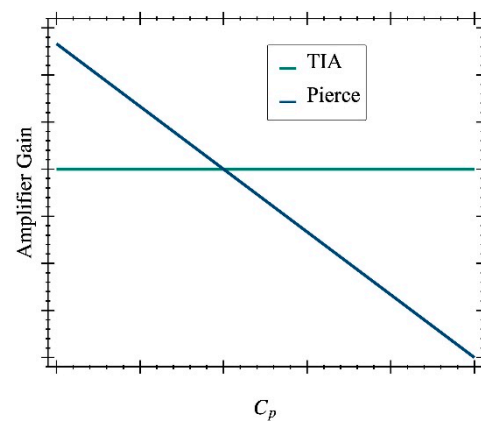


Figure 2. Open-loop gain from theoretical prediction for the two amplifier topologies as a function of the capacitance C_p .

In this work, we designed ad-hoc a commercial 0.35- μm 3.3 V CMOS technology TIA amplifier constituted by a first stage, based on the scheme from [16], and a second stage in which we added a control signal to tune the overall transimpedance gain as shown in Figure 3. The circuit behavior is closer to the ideal characteristic of Figure 2 in terms of sensitivity to the sense node parasitic capacitance.

In the first stage, C_p corresponds to the resonator capacitance (including the routing components). R_{G1} and R_{G2} ensure that transistors M_1 and M_2 are saturated by appropriately biasing the transistor gate; given their high nominal values (they are in the range of $G\Omega$), these devices have been implemented by two nMOS transistors, in anti-parallel configuration, working in their sub-threshold regions and consequently exhibiting an extremely high resistance [20]. In this design, we included a diode-connected pMOS transistor (M_4) with an equivalent small-signal resistance given by $R_D \approx 1/g_{m,M4}$. The transfer function can be written as

$$\frac{V_o(s)}{I_{sig}(s)} = \frac{I_{out}(s)}{I_{sig}(s)} R_D \approx \left(1 + \frac{C_1}{C_2}\right) R_D, \quad (2)$$

to obtain a gain close to $2.5 \times 10^6 \text{ V}\cdot\text{A}^{-1}$ with $R_D = 36 \text{ k}\Omega$, $C_2 = 6 \text{ pF}$ and $C_1 = 90 \text{ fF}$.

The second stage is a pMOS-based source follower with shunt-shunt feedback implemented through a nMOS device working in the linear region. The gate voltage is externally

controlled through $V_{control}$, which can take values between 0.5 and 2.5 V. This nMOS plays the role of variable resistance, providing tunable input resistance in terms of $V_{control}$. This variable input resistance affects the output resistance of the first stage and consequently its gain (Figure 3) [19].

Several simulation analyses were carried out to characterize the performance of the proposed circuit. Figure 4a shows the frequency response of the transimpedance gain (magnitude and phase). A maximum gain of $1.17 \cdot 10^6 \text{ V} \cdot \text{A}^{-1}$ (121 dB) was achieved over a bandwidth of 50 MHz. We notice that this value is lower than the $2.5 \cdot 10^6 \text{ V} \cdot \text{A}^{-1}$ obtained from Equation (2) given the moderate voltage gain for the first stage used in our design. Figure 4a also reports the dependence of the gain with $V_{control}$ (a very low impact has been observed in the phase plot in Figure 4b). The gain can be adjusted between 112 and 121 dB, varying $V_{control}$ between 0 and 3.3 V. Figure 5 shows the input-referred current noise, having a mean value of $192 \text{ fA} \cdot \text{Hz}^{-1/2}$ at frequencies around 10 MHz (equivalent to $225 \text{ nV} \cdot \text{Hz}^{-1/2}$ at the output). A low power consumption value of $930 \text{ } \mu\text{W}$ for a 3.3 V voltage supply was obtained.

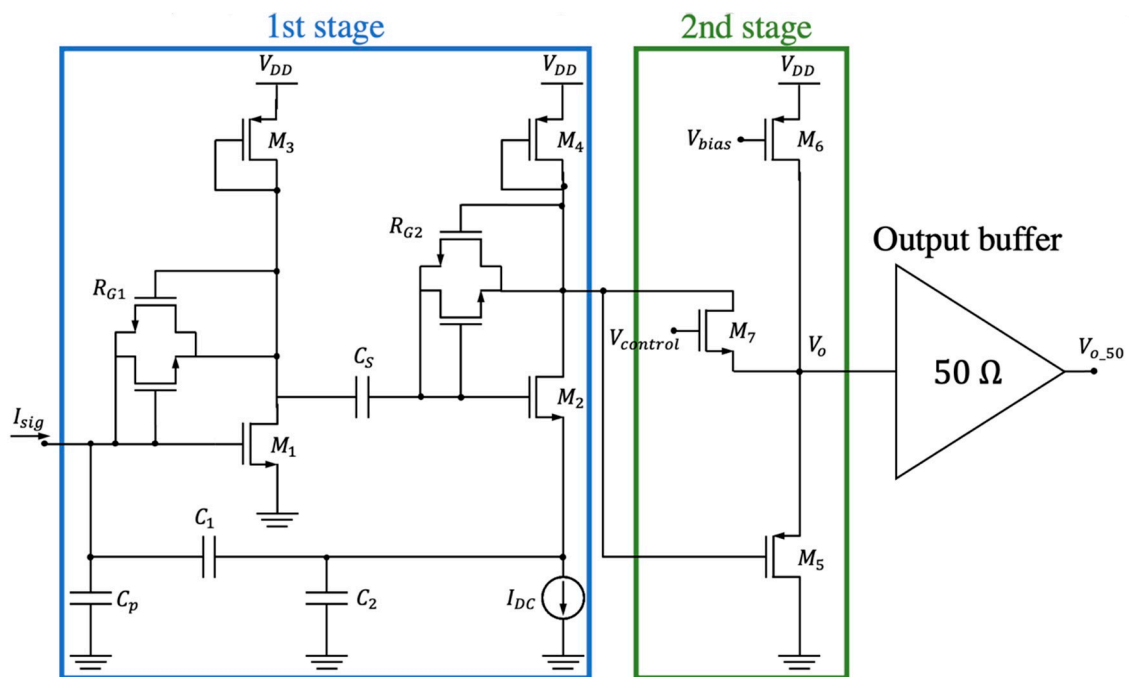


Figure 3. Schematic of the fabricated two-stage transimpedance amplifier (TIA) including an additional 50- Ω output buffer for testing purposes. The biasing resistors R_{G1} and R_{G2} have been implemented by two nMOS transistors in anti-parallel configuration.

Table 1 compares this TIA design to prior works [14,17,24–27]. As stated earlier, in addition to the gain insensitivity to C_p , a significant advantage of the proposed solution features a tunable-gain option. Finally, a Figure of Merit (FoM) is devised to compare the circuit design effort in series-resonant oscillators with various oscillating frequencies and resonator characteristics [14]:

$$FoM = \frac{k_B T BW^2 R_M^2}{V_{on}^2 P}, \quad (3)$$

where k_B is the Boltzmann constant, T is the absolute temperature, V_{on} is the output noise, BW is the TIA bandwidth, R_M is the TIA transimpedance gain, and P is the power consumption. The amplifier developed in this work exhibits an FoM value of $3.04 \cdot 10^{23}$, which is absolutely competitive with the reported state of the art as shown in Table 1. For comparison with the Pierce oscillator topology, an FoM value of $1.06 \cdot 10^{27}$ was achieved for a highly compact Pierce-based amplifier integrated together with a seesaw resonator

operating at frequencies below the 1-MHz range [21]. Despite the fact that it provides better performance compared to the present work, this would be rapidly degraded for higher operating frequencies and particularly for larger resonator parasitic capacitances. Similarly, in [23], a Pierce oscillator has been also demonstrated to achieve GSM noise requirements specifically oriented to phase noise optimization with a solution fabricated using the very same technological approach as this current work.

Table 1. Performance comparison with state-of-the-art reported works based on a TIA topology.

TIA	[24]	[14]	[25]	[17]	[26]	[27]	This Work
Bandwidth	280 MHz	20 MHz	60 MHz	1.8 MHz	1.2 MHz	90 MHz	50 MHz
Gain	25.0 kΩ– 89.0 kΩ	12.0 kΩ– 69.0 kΩ	316 kΩ	56.0 MΩ	7.94 MΩ	12.5 kΩ– 794 kΩ	330 kΩ– 1.17 MΩ
Output Voltage noise	-	-	790 μV/Hz ^{1/2}	3.64 μV/Hz ^{1/2}	199 nV/Hz ^{1/2}	3.18 μV/Hz ^{1/2}	225 nV/Hz ^{1/2}
Input-Referred Current Noise	-	-	-	-	-	-	192 fA/Hz ^{1/2}
CMOS Technology	0.18 μm	0.35 μm	0.18 μm	0.18 μm	0.35 μm	65 nm	0.35 μm
FoM	-	-	4.04·10 ¹⁴	7.28·10 ²¹	6.65·10 ²²	1.66·10 ²⁰	3.04·10 ²³
Power Consumption	1.57 mW	6.90 mW	5.90 mW	436 μW	150 μW	900 μW	930 μW

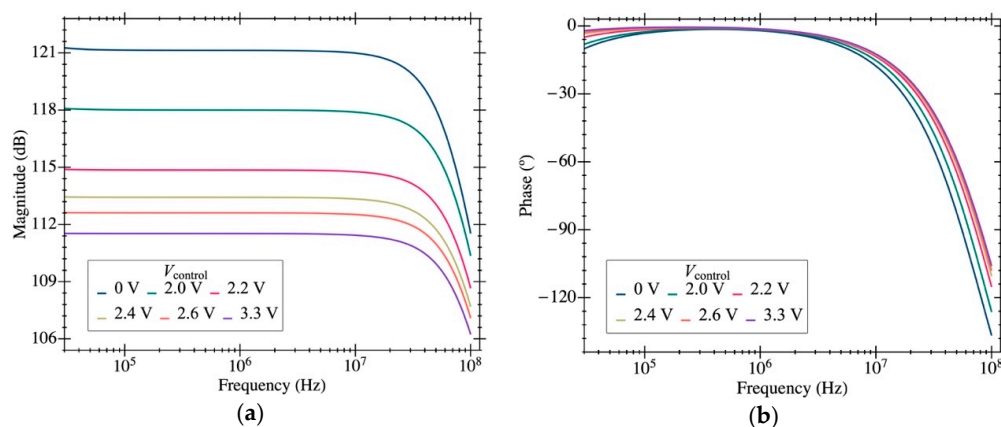


Figure 4. Bode plots of amplitude (a) and phase (b) of the proposed TIA at the V_o node. Results have been obtained under nominal biasing conditions with $C_p = 20$ fF.

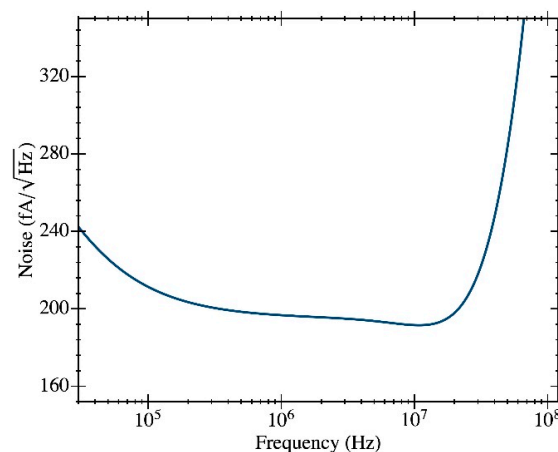


Figure 5. Simulation results for the input-referred current noise of the current TIA design.

3. Oscillator Electromechanical Model

The oscillator is constituted by the MEMS resonator, represented by its lumped equivalent RLC circuit and the feedthrough capacitance between the actuation and readout drivers [28], connected in series to the TIA as shown in Figure 6. In addition, an output buffer for testing purposes was also included in the integrated circuit scheme.

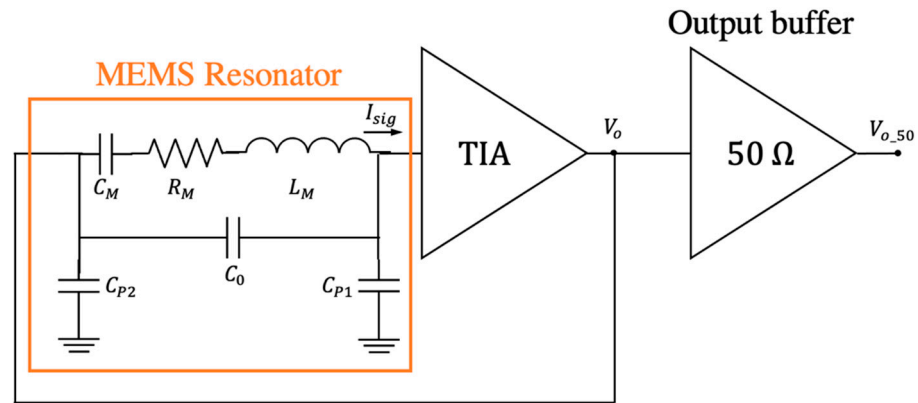


Figure 6. Oscillator schematic: MEMS resonator (represented by its lumped electrical equivalent model) and the transimpedance amplifier (TIA).

The equivalent admittance (Y_{eq}) in terms of the lumped elements is:

$$Y_{eq} = \left(j\omega L_M + \frac{1}{j\omega C_M} + R_M \right)^{-1} + j\omega C_0, \quad (4)$$

where the feedthrough capacitance (C_0) has also been included. The open-loop configuration amplifier output voltage is obtained from the equivalent admittance and the transconductance gain (G), which is accurately determined from the TIA amplifier post-layout simulations:

$$V_o = G Y_{eq}. \quad (5)$$

The main goal of this work is to determine these parameters for any specific resonator from an open-loop response by model fitting considering that the amplifier gain roughly depends on the resonator driver parasitic capacitance. From a practical point of view, it is advisable to use Q and ω_0 as fitting parameters, together with R_M , instead of C_M and L_M , which can be computed afterward. Therefore, using these definitions from the RLC branch,

$$Q = \frac{1}{\omega_0 R_M C_M}, \quad (6)$$

$$\omega_0 = \frac{1}{\sqrt{L_M C_M}}, \quad (7)$$

the output voltage is fitted from the open-loop response in terms of ω_0 , Q , C_0 , and R_M :

$$V_o = G \left(\frac{j \frac{\omega}{\omega_0} R_M Q}{1 - \left(\frac{\omega}{\omega_0} \right)^2 + j \frac{\omega}{\omega_0} Q} + j\omega C_0 \right) \quad (8)$$

Therefore, the resonator is fully characterized by first fitting the parameters in Equation (8) and subsequently computing the remaining parameters (C_M and L_M). The motional resistance represents the crucial parameter as it determines the amplifier gain constraints for a self-sustained oscillator.

4. MEMS Fabrication and Design

The mechanical resonators measured in this work were fabricated using a commercial CMOS 0.35- μm technology with an additional post-CMOS step consisting of a mask-less wet-etching performed at our laboratory. This additional step is aimed to release the resonators by removing the sacrificial oxide layer underneath, obtaining a fully integrated CMOS-MEMS solution [29]. The CMOS process used provides two polysilicon layers and a stack of four metal layers (TiN-Al-TiN) interconnected by Tungsten (W) vias. This fabrication approach based on a CMOS commercial technology provides a wide range of benefits as detailed in [9,10]. However, only the materials available in the manufacturing process can be considered as structural layers, and the manufacturer design rules must also be conformed to [10,12,30]. Thus, the resonator performance is constrained in some issues as a poor-quality factor (Q) compared to specific MEMS fabrication processes, reduced capacitive coupling between the resonator and the readout driver due to fixed layer thickness and minimum distance, and a relatively high device temperature sensitivity. Three design options, shown in Figure 7, were considered in this work, called Plate Resonator 1 (PR1), Plate Resonator 2 (PR2), and Plate Resonator 3 (PR3). All of them consist of an anchored plate resonator with a two-driver configuration with electrostatic actuation and capacitive readout to make it feasible to combine the MEMS with the readout circuitry in the same IC for a monolithic integration [31]. The large motional resistances exhibited by the resonators (as a consequence of the aforementioned relatively small capacitive coupling) is compensated by the high-gain, low-noise integrated TIA and a significant reduction of the parasitic contributions.

The MEMS resonators were designed by means of a two-layer strategy, similar to that in [32], so that the coupling capacitance became larger compared to single-layer geometries, i.e., decreased the motional resistance. The coupling can be improved by either reducing the resonator-driver gap or by increasing the composite material thickness. Therefore, the first two structures presented here exploit each one of these alternatives for design optimization. Additionally, a composite material in the form of metal–oxide–metal reduces its overall temperature sensitivity because the oxide relative stress when increasing the operating temperature changes opposite to that of the metal layer [33]. This fact is also a key aspect for MEMS resonators design when considering the final oscillator stability as an important figure of merit directly related to the sensor limit of detection. In this sense, the PR1 structure benefits from MET3-OX-MET4 and MET3-VIA-MET4 layers (see Figure 7a), while the PR2 was designed to have a MET-VIA stack as in Figure 7b. On behalf of PR3, it inherits most of the design strategy developed for PR2 shown in Figure 7c. It scales up its platform dimensions so as to provide a solution suitable for inkjet deposition; one of the possible applications for this resonator is to operate as a gravimetric gas sensor thanks to its outstanding distributed mass sensitivity [31] together with a proper functionalization process with a specific layer to capture the target molecules. A detailed discussion of each structure is presented next.

4.1. Plate Resonator 1

This design, shown in Figure 7a, consists of a four-anchored plate resonator composed of two materials: (i) the resonator main body is designed to be manufactured with a MET3-OX-MET4 (MOM) compound so that the overall effective mass growth is minimum compared to using the VIA layer required in the anchors and drivers for coupling requirements; (ii) the anchors combine the previous stack with a MET-VIA-MET (MVM) composite to get an increase in the readout coupling thanks to the larger thickness when including MET4. However, the minimum distance between two MET4-adjacent layers is 600 nm, worsening the overall coupling when compared to a gap of 500 nm available by design rules when using VIA or lower metal layers. To investigate this option, we created the second structure (Figure 7b), where the MV composite is not used in the whole beam to avoid an excessive increase of the whole resonator mass density [32].

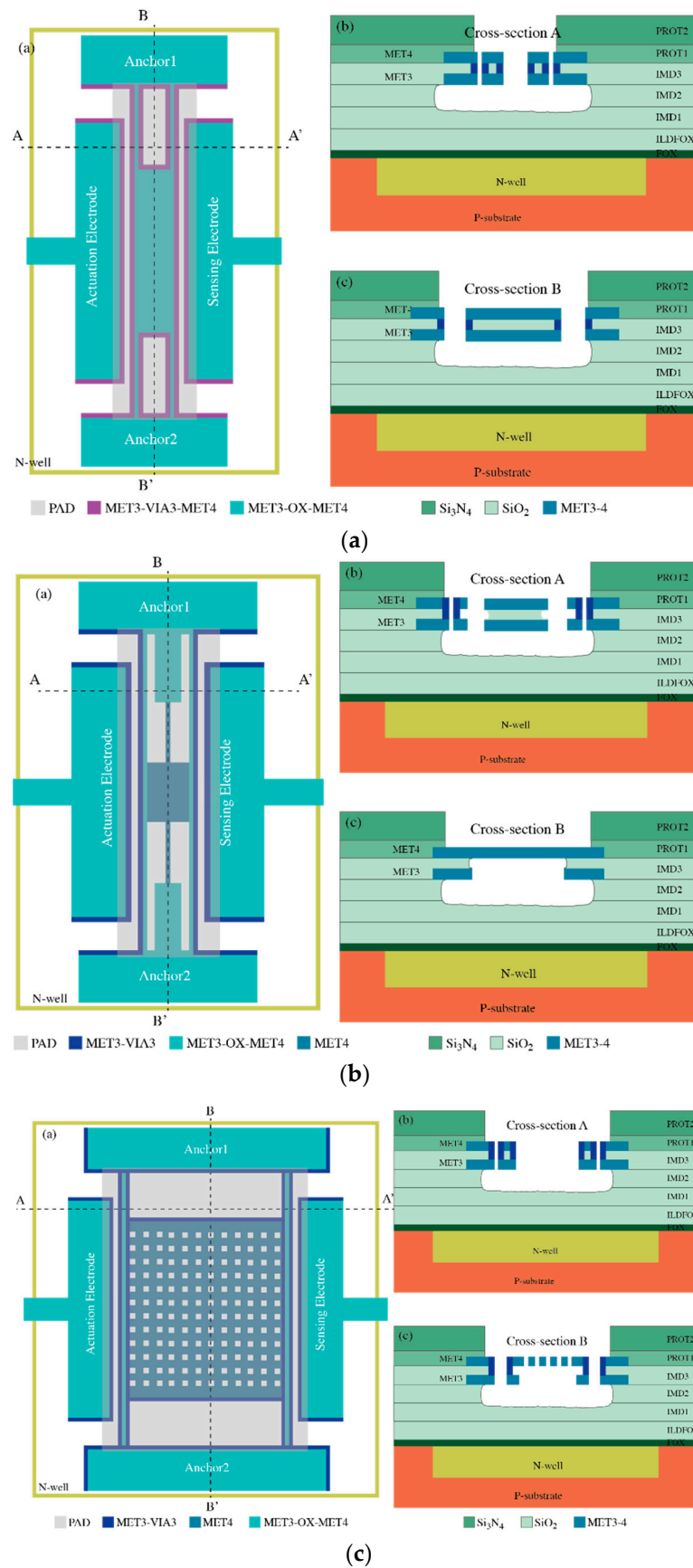


Figure 7. Schematic design of the fabricated MEMS resonators including the different layers that have been used: (a) PR1, (b) PR2 and (c) PR3.

4.2. Plate Resonator 2

The device shown in Figure 7b is a six-anchored plate resonator with the four outer anchors conceived to provide large coupling and vibration stability, while the two inner ones increase the overall stiffness to achieve higher oscillation frequency. Similarly to the previous design, it also combines various material aggregates: (i) the main body and the inner anchors were made of a single MET4 (M) layer as it does not play any role in the coupling capacitance—not requiring an increased thickness—while the overall mass is reduced, thus decreasing the motional resistance; (ii) the outer anchors merge the MOM composite with a MET3-VIA composite at the driver side to reduce the resonator-driver gap since MET3 and VIA layers can have a separation of only 500 nm. A reduction in the gap has a higher impact on the coupling than the overall thickness does. In any case, the coupling thickness of this structure will be smaller than the one of the previously described structure. Notice that, depending on the metal and via combinations, the thickness of each layer may vary [34].

The structure depicted in Figure 7c takes the design strategy from PR2 and implements some improvements in the pursuit of a large enough platform to enable inkjet deposition featuring droplets with diameter in the order of 70 μm . It combines the same material mixtures with a single metal layer approach: (i) the main body material is the MET4 layer to reduce the overall mass and, in consequence, the motional resistance, as well as to allow for regularly spaced holes for release purposes; (ii) the beams combine the MOM composite in the center for temperature insensitivity with the MV in both sides to increase the stiffness and improve the capacitive coupling; and (iii) the perimeter of the structure also features the MV composite to provide an increased stiffness to the overall platform and avoid vertical bending under self-loading effects. According to manufacturer fabrication parameters, the readout electrode parasitic capacitance featured for this structure is in the order of 80 fF; $8\times$ the value found for a minimum-size MEMS resonator fabricated with the same 0.35- μm technology [15]. Thus, one would expect for the Pierce topology alternative to have its open-loop gain reduced, similar to the possibility of failing to compensate for the motional resistance losses and, consequently, not being able to operate as a self-sustained oscillator. In such a case, it is the TIA alternative that provides a huge advantage, having an open-loop gain that does not diminish with increased input capacitance. Therefore, in this work, we will also provide electrical characterization for this structure obtaining a parameter extraction with an accuracy that, otherwise, would have been not feasible with a Pierce scheme-based amplifier.

5. Electrical Characterization

5.1. Transimpedance Amplifier

Figure 8 shows one of the CMOS-MEMS devices fabricated in the IC using a CMOS 0.35- μm commercial technology. First, the CMOS TIA circuit was characterized in terms of noise performance. A voltage noise at the V_{o_50} node of $110 \text{ nV}/\text{Hz}^{1/2}$ at 10 MHz was measured, providing a value that perfectly matches the simulation outcome (see Figure 9). For clarification, Figure 9 also depicts the simulated voltage noise at the V_o node (the output of the TIA 2nd stage), which is $225 \text{ nV}/\text{Hz}^{1/2}$ at 10 MHz (see Table 1). This node is the one used to drive the resonator excitation and closes the oscillator loop, but it cannot be experimentally tested since it was not designed to interface with the 50- Ω input laboratory benchtop equipment [20]. Notice that the noise at this node is higher than the one obtained at the tested node V_{o_50} because of the attenuation introduced by the output buffer.

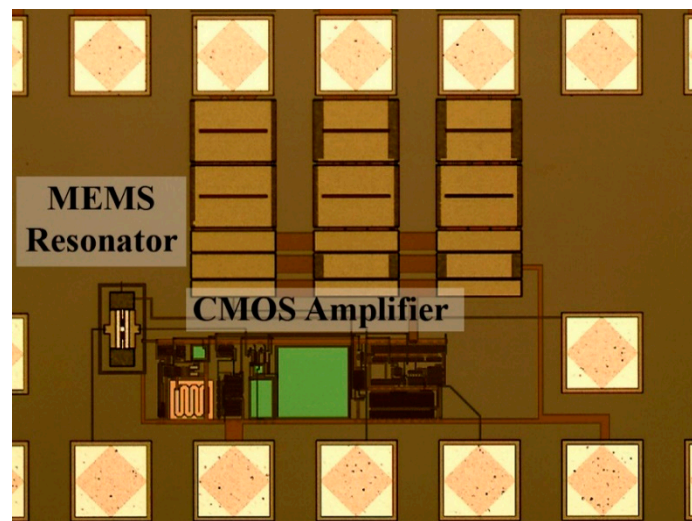


Figure 8. Optical image of the CMOS-MEMS oscillator IC fabricated in a CMOS 0.35- μm commercial technology.

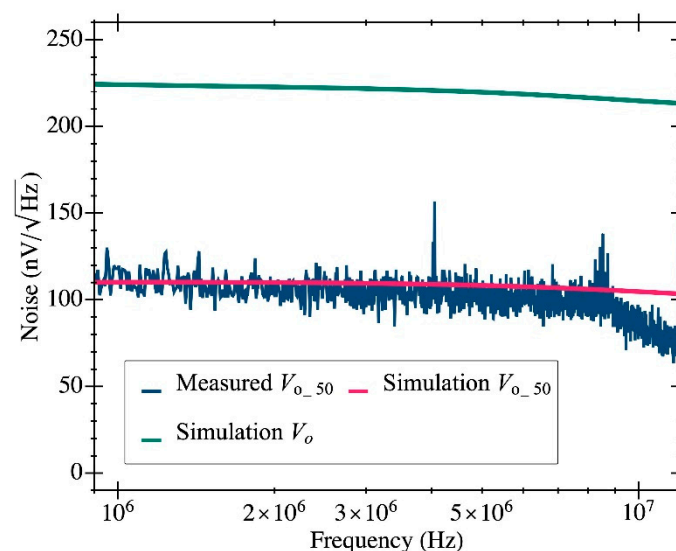


Figure 9. The measured output voltage noise (blue line) at V_{o_50} is compared to the simulation results at the same node (magenta line) to show that both values are in good agreement. Additionally, the simulated voltage noise at V_o is depicted with a solid green line to show how the output buffer attenuates the voltage signal.

5.2. Plate Resonator 1 and Plate Resonator 2

The CMOS-MEMS resonators were characterized in both open- and closed-loop configurations thanks to the capacitive readout scheme and the integrated amplifier. Figure 9 shows the measured electromechanical transmission coefficient (obtained with a *Keysight ENA E5061B* network analyzer) at low excitation power (-35 dBm) to keep the resonators' operation in the linear regime both for vacuum (below 10^{-3} mbar) and ambient pressure. Additionally, a sweep of the resonator DC biasing voltage from 10 V to 40 V was performed to obtain the motional resistance at various values and experimentally observe the relationship in which the resistance is inversely proportional to the squared DC voltage through the electromechanical coupling.

The experimental response shown in Figure 10 was fitted to the model in Section 3 to obtain the aforementioned parameters. The resulting resonance frequency is plotted in Figure 11 as a function of the biasing voltage and fitted as $f^2 = a - bV_{dc}^2$, from which the natural frequency was computed (resonant frequency at 0 V biasing). Figure 12 illustrates

an example of such fitting with the extracted values demonstrating high model accuracy, as it perfectly matches the measured transmission coefficient. Remarkably, this degree of precision in the parameter extraction procedure is only achievable thanks to having an amplifier open-loop gain that does not depend on the input capacitance and whose specific value was obtained from post-layout simulations. The parameters obtained for both resonators are listed in Table 2 for a biasing voltage of 25 V. We also obtained the motional resistance for all biasing voltages (plotted in Figure 13); the theoretical prediction is also included in solid lines as well as the linear fitting in logarithmic scale in dashed lines. Results show that the theoretical motional resistance prediction matches the experimental data with an error below 20% in the worst case; such a reliable calculation is also a direct consequence of the amplifier gain being accurately characterized. In any case, the remaining error could be attributed to the metal layers' degradation caused by the etching step that is intended to remove only the sacrificial oxide but in practice has an impact on the metal layers as well [35]. Such a metal degradation can reduce the overall resonator-driving coupling capacitance, resulting in experimental motional resistances larger than expected. Furthermore, the fabrication process itself, together with the post-CMOS etching step, has been shown to produce a 10% error in the measured resonant frequency, which goes in line with the error also observed for the motional resistance.

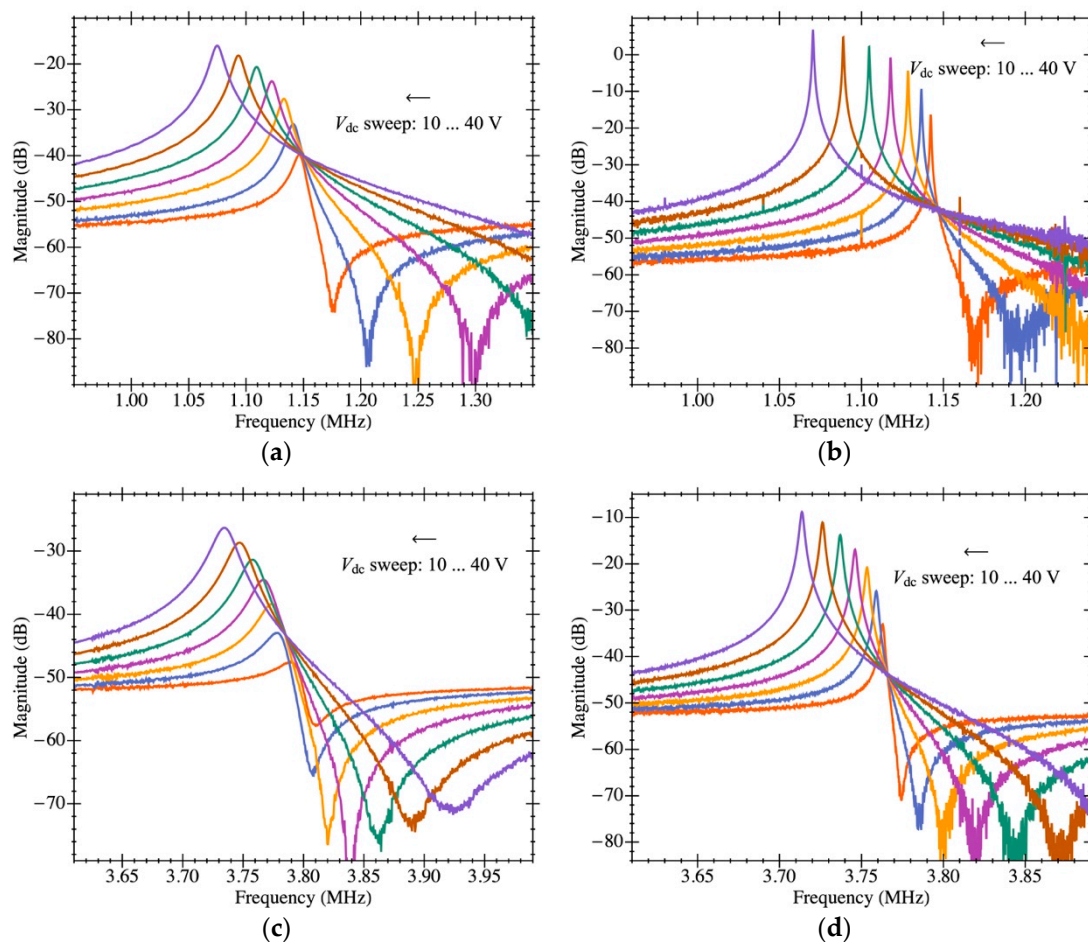


Figure 10. Electrical characterization of the MEMS resonator with on-chip readout circuit in open-loop configuration. Experimental magnitude of frequency response for various MEMS bias voltages (V_{dc}): (a) plate resonator PR1 in ambient pressure; (b) plate resonator PR1 in vacuum pressure; (c) plate resonator PR2 in ambient pressure; (d) plate resonator PR2 in vacuum pressure.

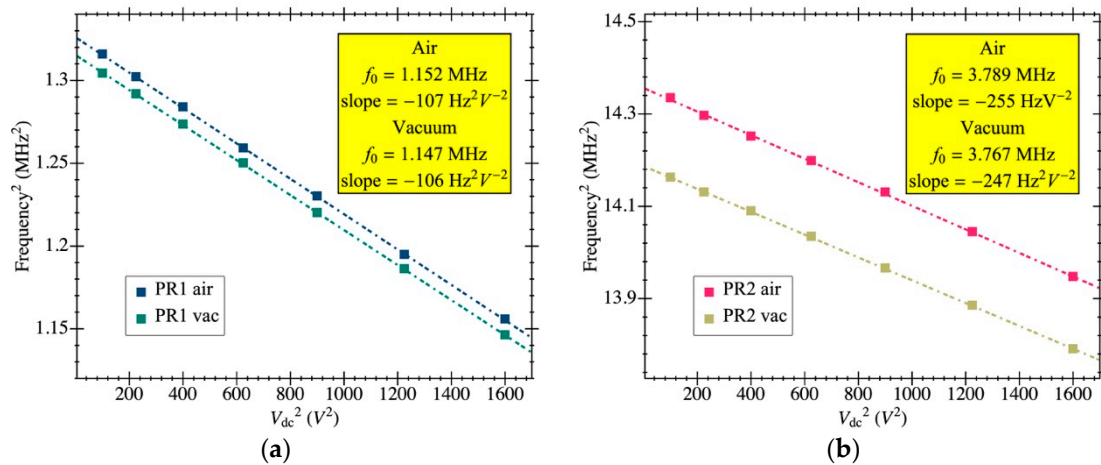


Figure 11. Resonance frequency dependence with the resonator bias voltage obtained from experimental open-loop response data fitting. The linear fit for the frequency values is also included (dashed lines) to obtain the natural frequency at 0 bias voltage for each case: (a) PR1; (b) PR2.

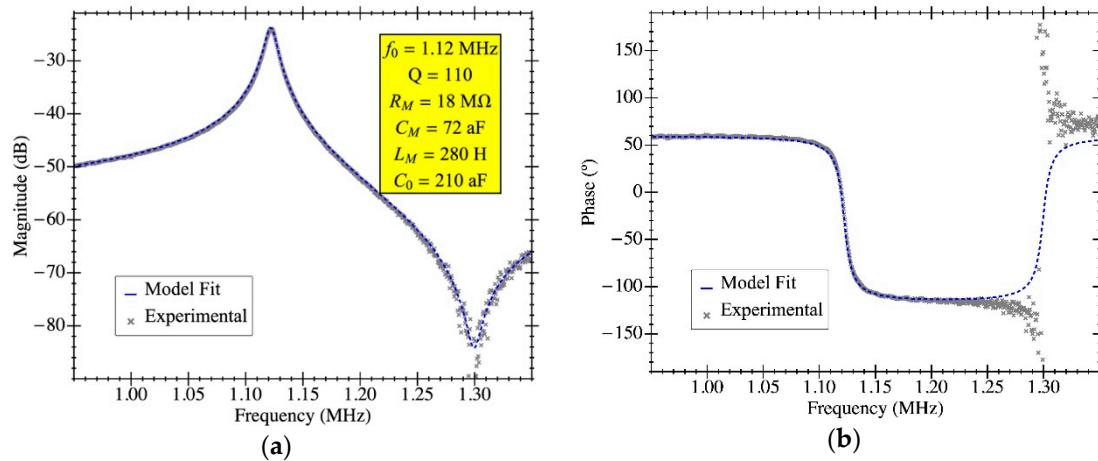


Figure 12. Electrical characterization of the MEMS resonator with on-chip readout circuit in open-loop configuration for RLC parameter extraction by means of model fitting. The experimental data corresponds to PR1 using a bias voltage of 25 V in air conditions: (a) magnitude and (b) phase.

Table 2. Extracted parameters from experimental open-loop response by model fitting for both resonators in air and vacuum conditions.

Resonator	f_0 (MHz)	Q	R_M (M Ω)	C_M (aF)	L_M (H)	C_0 (aF)
PR1 (air)	1.152	110	18 [†]	72 [†]	280 [†]	210
PR1 (vac)	1.147	2100	1.2 [†]	56 [†]	360 [†]	210
PR2 (air)	3.789	210	63 [†]	3.4 [†]	530 [†]	890
PR2 (vac)	3.767	1600	7.7 [†]	3.3 [†]	520 [†]	890
PR3 (air)	0.402	132	662 [§]	4.5 [§]	34,000 [§]	96

[†] These values refer to a biasing voltage of 25 V. [§] These values refer to a biasing voltage of 8 V.

The PR1 structure was also measured in closed-loop configuration to operate as an oscillator in self-excited mode in vacuum conditions obtaining the output voltage waveform shown in Figure 14a. The self-sustained oscillation started at a DC biasing voltage of 23 V, and at $V_{dc} = 25$ V, the oscillator exhibited a frequency of 1.120 MHz and a peak-to-peak voltage of 273 mV. The measured Allan deviation (obtained with the frequency counter Pendulum CNT-90) is also provided in Figure 14b for integration times ranging from $5 \cdot 10^{-5}$ s to 5 s, reaching a minimum value of 2 ppm for an integration time of 300 ms. The

experimental value for the oscillator stability is close to the one obtained in previous works using a Pierce topology for the oscillator circuit [36].

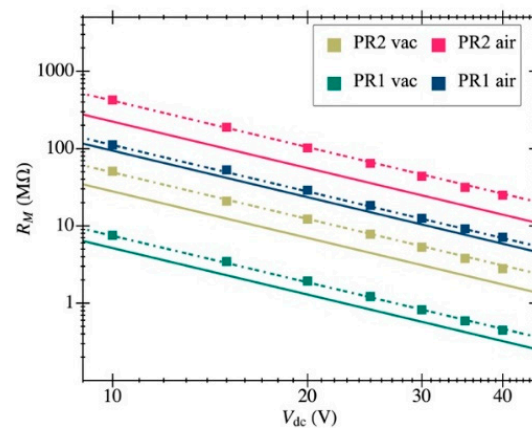


Figure 13. Motional resistance computed from experimental open-loop data by means of the proposed model fit: the value is inversely proportional to the square of the resonator biasing voltage. The obtained fit (dashed lines) matches the theoretical prediction (solid lines) for both structures in air and vacuum conditions.

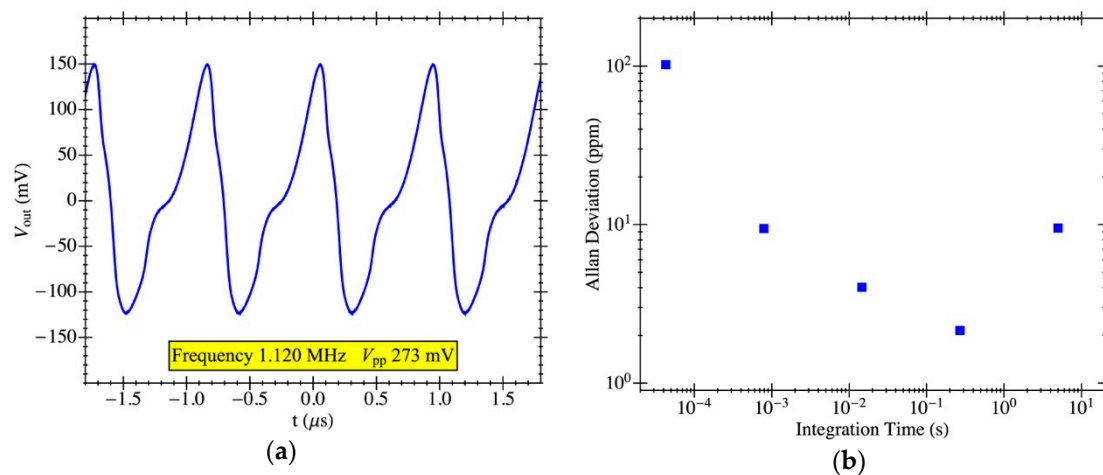


Figure 14. MEMS resonator electrical characterization with on-chip CMOS amplifier in a closed-loop configuration: (a) oscillator output voltage in the time domain for PR1 with a biasing voltage of 25V; (b) measured Allan deviation as a function of the integration time in ambient temperature and pressure.

5.3. Plate Resonator 3

In this section, the extraction of electromechanical parameters for PR3 are also obtained using the capabilities of the TIA amplifier addressed in this work. The plate resonator has a $150\ \mu\text{m} \times 150\ \mu\text{m}$ platform that features a parasitic capacitance due to the readout driver on the order of 80 fF estimated from manufacturer specifications. The open-loop response in air conditions is shown in Figure 15a for a biasing voltage that ranges from 4 V to 12 V. Additionally, the Bode plot corresponding to 8 V biasing is depicted in Figure 15b,c and fitted to the theoretical model presented. It is clearly shown that both the experimental curve and theoretical model are in good agreement thanks to having the open-loop gain of the on-chip amplifier perfectly characterized and not depending on the aforementioned parasitic capacitance. Interestingly, the feedthrough capacitance obtained for PR3 is $2\times$ smaller than the one featured by PR1 in spite of having a much larger platform size. Actually, this is directly related to the fact that, with a larger platform, the readout and driving electrodes are further dissociated and, in consequence, the parasitic capacitance

between them is smaller. Additionally, the obtained motional resistance for such a structure is well above the one presented for PR1—662 M Ω over 18 M Ω —as a consequence of the highly increased mass.

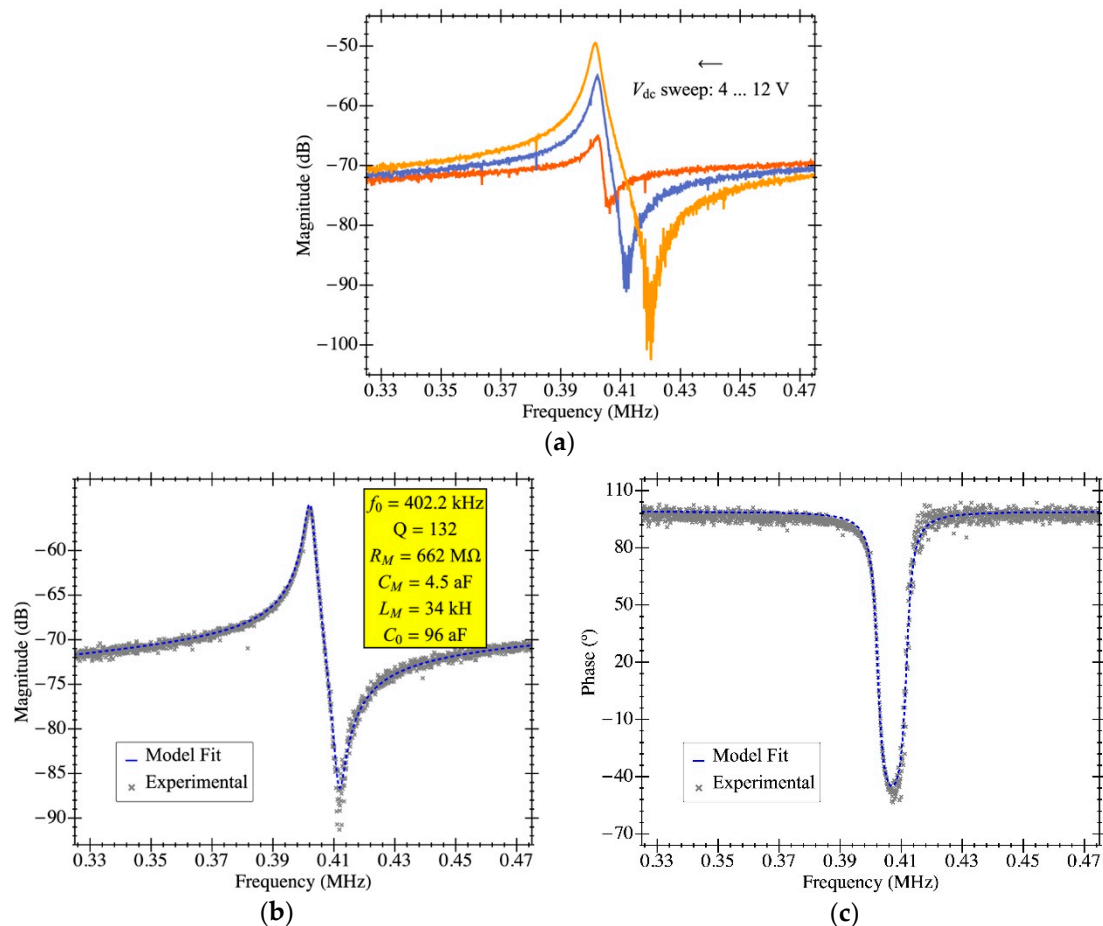


Figure 15. Electrical characterization of the MEMS resonator with on-chip readout circuit in open-loop configuration. (a) Experimental magnitude of frequency response for various MEMS bias voltages (V_{dc}) for the plate resonator PR3 in ambient pressure. RLC parameter extraction by means of model fitting; the experimental data corresponds to a bias voltage of 8 V in air conditions: (b) magnitude and (c) phase.

6. Conclusions

The design of capacitive readout circuits specifically oriented to CMOS-MEMS resonators that operate in the MHz-range is a demanding task if state-of-the-art outcomes are to be achieved due to moderate capacitive coupling and rather poor-quality factor of fabrication materials. In this work, we have provided experimental proof of a design that not only enables self-sustained oscillation but also provides a great characterization capability together with tunable gain so as to keep resonators operating in their linear regime that suits a wide range of resonator characteristics.

We developed a versatile transimpedance amplifier (TIA) designed in a commercial 0.35- μm 3.3 V CMOS technology specifically oriented to monolithic CMOS-MEMS resonators. The proposed design is clearly competitive with the state of the art, achieving low power, low noise, and a high gain that enables closed-loop oscillation of MEMS resonators that have been experimentally tested. Moreover, it offers tunable gain between 112 and 121 dB with a dramatically reduced dependence on the input parasitic capacitance compared to other common alternatives such as the Pierce topology commonly used in previous works [37].

The TIA was applied to accurately characterize three MEMS resonators monolithically fabricated into the same CMOS die. The extraction of their electromechanical parameters using the theoretical model presented offers an extremely precise fitting, thus being able to obtain a correct value for the motional resistance thanks to having a parasitic capacitance independent gain. This value represents a key parameter in MEMS resonator and sustaining amplifier co-design, being of great importance in the design stage for future fabrication iterations and system improvement.

Author Contributions: Conceptualization: R.P.-R., J.V., and J.S.; investigation: R.P.-R. and S.B.; methodology: R.P.-R., J.V., S.B. and J.S.; supervision: J.V. and J.S.; writing—review and editing: R.P.-R., J.V. and J.S. All authors have read and agreed to the published version of the manuscript.

Funding: This work has been supported by the Spanish Ministry of Economy and Competitiveness under project TEC2017-88635-R (AEI/FEDER, UE).

Acknowledgments: R. Perelló-Roig thanks his grant FPU-16/01758 from the Spanish Ministry of Education, Culture and Sport.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Nguyen, C.T.C. Integrated micromechanical radio front-ends. In Proceedings of the International Symposium on VLSI Technology, Systems, and Applications (VLSA-TSA) 2008, Hsinchu, Taiwan, 21–23 April 2008; pp. 3–4.
2. Nguyen, C.T.C.; Howe, R.T. CMOS micromechanical resonator oscillator. In Proceedings of the IEEE International Electron Devices Meeting, Washington, DC, USA, 5–8 December 1993; pp. 199–202.
3. Van Beek, J.T.M.; Puers, R. A review of MEMS oscillators for frequency reference and timing applications. *J. Micromech. Microeng.* **2012**, *22*, 013001. [[CrossRef](#)]
4. Pachkawade, V.; Li, M.H.; Li, C.S.; Li, S.S. A CMOS-MEMS resonator integrated system for oscillator application. *IEEE Sens. J.* **2013**, *13*, 2882–2889. [[CrossRef](#)]
5. Nguyen, C.T.C. MEMS technology for timing and frequency control. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2007**, *54*, 251–270. [[CrossRef](#)] [[PubMed](#)]
6. Verd, J.; Uranga, A.; Abadal, G.; Teva, J.L.; Torres, F.; López, J.; Pérez-Murano, F.; Esteve, J.; Barniol, N. Monolithic CMOS MEMS oscillator circuit for sensing in the attogram range. *IEEE Electron Device Lett.* **2008**, *29*, 146–148. [[CrossRef](#)]
7. Lo, C.C.; Chen, F.; Fedder, G.K. Integrated HF CMOS-MEMS square-frame resonators with on-chip electronics and electrothermal narrow gap mechanism. In Proceedings of the 13th International Conference on Solid-State Sensors, Actuators and Microsystems, 2005 Digest of Technical Papers TRANSDUCERS '05, Seoul, Korea, 5–9 June 2005; pp. 2074–2077.
8. Huang, W.L.; Ren, Z.; Lin, Y.W.; Chen, H.Y.; Lahann, J.; Nguyen, C.T.C. Fully monolithic CMOS nickel micromechanical resonator oscillator. In Proceedings of the 2008 IEEE 21st International Conference on Micro Electro Mechanical Systems (MEMS), Wuhan, China, 13–17 January 2008; pp. 10–13.
9. Brand, O. Microsensor integration into Systems-on-Chip. *Proc. IEEE* **2006**, *94*, 1160–1176. [[CrossRef](#)]
10. Uranga, A.; Verd, J.; Barniol, N. CMOS–MEMS resonators: From devices to applications. *Microelectron. Eng.* **2015**, *132*, 58–73. [[CrossRef](#)]
11. Chen, W.C.; Fang, W.; Li, S.S. A generalized CMOS-MEMS platform for micromechanical resonators monolithically integrated with circuits. *J. Micromech. Microeng.* **2011**, *21*, 065012. [[CrossRef](#)]
12. Fedder, G.K.; Howe, R.T.; Liu, T.J.K.; Quévy, E.P. Technologies for cofabricating MEMS and electronics. *Proc. IEEE* **2008**, *96*, 306–322. [[CrossRef](#)]
13. Xie, H.; Erdmann, L.; Zhu, X.; Gabriel, K.J.; Fedder, G.K. Post-CMOS processing for high-aspect-ratio integrated silicon microstructures. *J. Microelectromech. Syst.* **2002**, *11*, 93–101.
14. Seth, S.; Wang, S.; Kenny, T.; Murmann, B. A -131-dBc/Hz, 20-MHz MEMS oscillator with a 6.9-mW, 69-k Ω , gain-tunable CMOS TIA. In Proceedings of the ESSCIRC (ESSCIRC) 2012, Bordeaux, France, 17–21 September 2012; pp. 249–252.
15. Verd, J.; Uranga, A.; Abadal, G.; Teva, J.; Pérez-Murano, F.; Barniol, N. High-sensitivity capacitive sensing interfacing circuit for monolithic CMOS M/NEMS resonators. *Electron. Lett.* **2007**, *34*, 1274. [[CrossRef](#)]
16. Razavi, B. A 622 Mb/s 4.5 pA/ $\sqrt{\text{Hz}}$ CMOS transimpedance amplifier [for optical receiver front-end]. In Proceedings of the 2000 IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 9 February 2000; pp. 162–163.
17. Salvia, J.; Lajvardi, P.; Hekmat, M.; Murmann, B. A 56 M Ω CMOS TIA for MEMS applications. In Proceedings of the 2009 IEEE Custom Integrated Circuits Conference, Rome, Italy, 13–16 September 2009; pp. 199–202.
18. Lee, S.; Demirci, M.U.; Nguyen, C.T.C. A 10-MHz Micromechanical Resonator Pierce Reference Oscillator for Communications. In Proceedings of the 11th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XV) 2001, Berlin, Germany, 10–14 June 2001; pp. 1066–1069.

19. Sobreviela, G.; Uranga, A.; Barniol, N. Tunable transimpedance sustaining-amplifier for high impedance CMOS-MEMS resonators. In Proceedings of the 10th Conference on PhD Research in Microelectronics and Electronics (PRIME) 2014, Grenoble, France, 30 June–3 July 2014; pp. 1–4.
20. Verd, J.; Uranga, A.; Segura, J.; Barniol, N. A 3V CMOS-MEMS oscillator in 0.35 μm CMOS technology. In Proceedings of the 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII) 2013, Barcelona, Spain, 16–20 June 2013; pp. 806–809.
21. Riverola, M.; Sobreviela, G.; Torres, F.; Uranga, A.; Barniol, N. Single-resonator dual-frequency BEOL-embedded CMOS-MEMS oscillator with low-power and ultra-compact TIA core. *IEEE Electron Device Lett.* **2017**, *38*, 273–276. [[CrossRef](#)]
22. Roessig, T.A.; Howe, R.T.; Pisano, A.P.; Smith, J.H. Surface-micromachined 1 MHz oscillator with low-noise Pierce configuration. In Proceedings of the 1998 Solid State Sensor and Actuator Workshop, Hilton Head, SC, USA, 1 June 1998.
23. Naing, T.L.; Rocheleau, T.O.; Alon, E.; Nguyen, C.T.C. Low-power MEMS-based Pierce oscillator using a 61-MHz capacitive-gap disk resonator. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2020**, *67*, 1377–1391. [[CrossRef](#)] [[PubMed](#)]
24. Li, M.H.; Li, C.S.; Hou, L.J.; Liu, Y.C.; Li, S.S. A 1.57 mW 99 dB CMOS transimpedance amplifier for VHF micromechanical reference oscillators. In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS) 2012, Seoul, Korea, 20–23 May 2012; pp. 209–212.
25. Chen, T.T.; Huang, J.C.; Peng, Y.C.; Chu, C.H.; Lin, C.H.; Cheng, C.W.; Li, C.-S.; Li, S.-S. A 17.6-MHz 2.5V ultra-low polarization voltage MEMS oscillator using an innovative high gain-bandwidth fully differential trans-impedance voltage amplifier. In Proceedings of the IEEE 26th International Conference on Micro Electro Mechanical Systems (MEMS) 2013, Taipei, Taiwan, 20–24 January 2013; pp. 741–744.
26. Li, M.H.; Chen, C.Y.; Liu, C.Y.; Li, S.S. A sub-150- μW BEOL-embedded CMOS-MEMS oscillator with a 138-dB ultra-low-noise TIA. *IEEE Electron Device Lett.* **2016**, *37*, 648–651. [[CrossRef](#)]
27. Bouchami, A.; Elsayed, M.Y.; Nabki, F. A Sub-mW 18-MHz MEMS Oscillator Based on a 98-dB Ω Adjustable Bandwidth Transimpedance Amplifier and a Lamé-Mode Resonator. *Sensors* **2019**, *19*, 2680. [[CrossRef](#)] [[PubMed](#)]
28. Senturia, S.D. *Microsystem Design*; Springer: New York, NY, USA, 2001.
29. Verd, J.; Uranga, A.; Teva, J.; López, J.; Torres, F.; Esteve, J.; Abadal, G.; Pérez-Murano, F.; Barniol, N. Integrated CMOS MEMS with on-chip readout electronics for high-frequency applications. *IEEE Electron Device Lett.* **2006**, *27*, 495–597. [[CrossRef](#)]
30. Fang, W.; Li, S.S.; Cheng, C.L.; Chang, C.I.; Chen, W.C.; Liu, Y.C.; Tsai, M.-H.; Sun, C. CMOS MEMS: A key technology towards the “More than Moore” era. In Proceedings of the 2013 Transducers & Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII), Barcelona, Spain, 16–20 June 2013; pp. 2513–2518.
31. Perelló-Roig, R.; Verd, J.; Barceló, J.; Bota, S.; Segura, J. A 0.35- μm CMOS-MEMS oscillator for high-resolution distributed mass detection. *Micromachines* **2018**, *9*, 484. [[CrossRef](#)] [[PubMed](#)]
32. Vidal-Álvarez, G.; Marigó, E.; Torres, F.; Barniol, N. Fabrication and measurement of a suspended nanochannel microbridge resonator monolithically integrated with CMOS readout circuitry. *Micromachines* **2016**, *7*, 40. [[CrossRef](#)] [[PubMed](#)]
33. Liu, Y.C.; Tsai, M.H.; Chen, W.C.; Li, M.H.; Li, S.S.; Fang, W. Temperature-compensated CMOS-MEMS oxide resonators. *J. Microelectromech. Syst.* **2013**, *22*, 1054–1065. [[CrossRef](#)]
34. Riverola, M.; Vidal-Álvarez, G.; Torres, F.; Barniol, N. CMOS-NEM relay based on tungsten VIA layer. In Proceedings of the IEEE Sensors 2014, Valencia, Spain, 2–5 November 2014; pp. 162–165.
35. Michalik, P.; Fernández, D.; Wietstruck, M.; Kaynak, M.; Madrenas, J. Experiments on MEMS integration in 0.25 μm CMOS process. *Sensors* **2018**, *18*, 2111. [[CrossRef](#)] [[PubMed](#)]
36. Perelló-Roig, R.; Verd, J.; Bota, S.; Segura, J. Frequency Fluctuations in CMOS-MEMS Oscillators: Towards the Thermomechanical Limit. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 27–30 May 2018; pp. 1–5.
37. Melero, A.; Verd, J.; Uranga, A.; Segura, J.; Barniol, N. A 24-MHz differential oscillator circuit for 5-M Ω CMOS-MEMS resonator. In Proceedings of the XXI Conference on Design of Circuits and Integrated Systems (DCIS) 2011, Albufeira, Portugal, 16–18 November 2011.