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Supplementary information

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Nanofluidic logic with mechano–ionic memristive switches

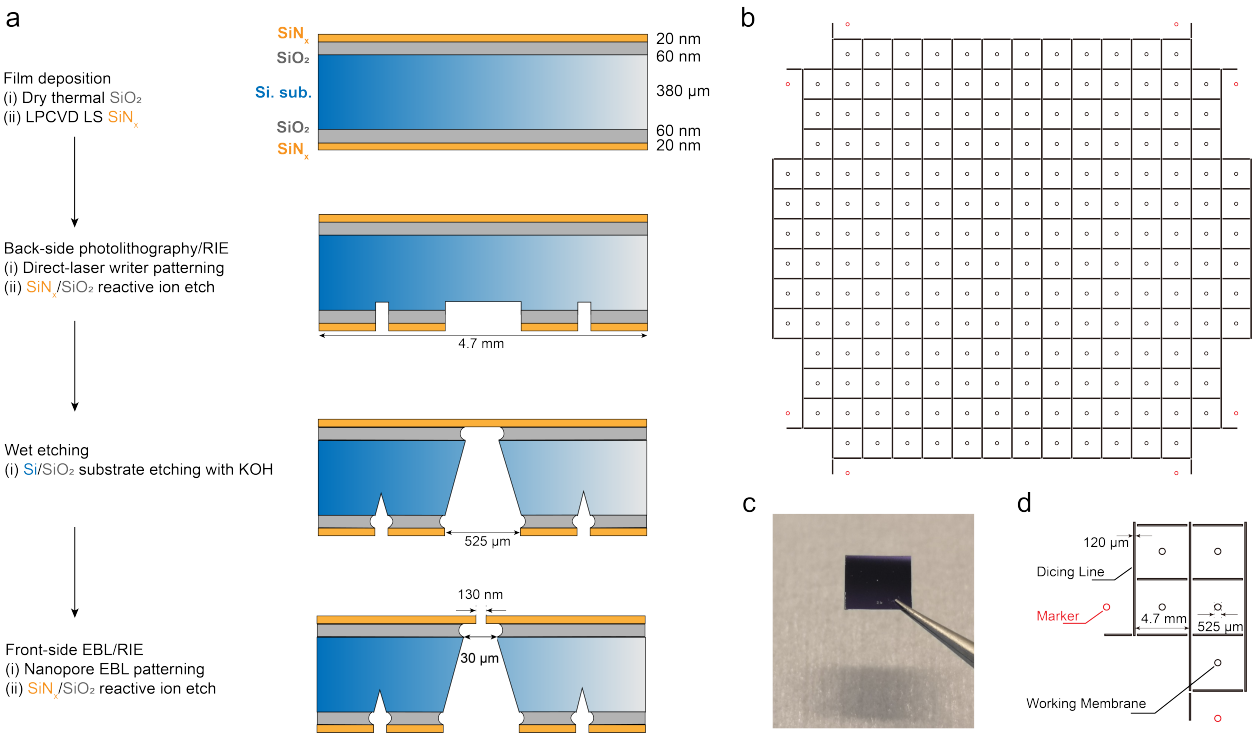
In the format provided by the authors and unedited

Contents

1 Nanofabrication

1.1 Step 0: Wafer-scale fabrication of silicon nitride aperture

Silicon nitride (SiN) windows, as the basis and the starting point of our HAC nanofluidic devices, are fabricated in a state of art cleanroom facility with a technical route of reactive ion etching (Supplementary Figure 1.a)[1;2]. Here, we start from a 4-inch double side polished silicon wafer with a 60 nm SiO_2 and a 20 nm low stress silicon nitride at both sides from Center of Micro-NanoTechnology in EPFL. The first step is the back-side patterning. Direct-laser pattering and reactive ion etching will result in a back-side design on the silicon nitride and silicon oxide layer (Supplementary Figure 1.b), which includes working membrane positions, contrast markers and dicing lines (supplementary Figure 1.d). Then, the KOH wet etching will release the freestanding silicon nitride membrane according to the pattern from the previous step. In the end, we pattern the front side design and silicon nitride apertures with electron beam lithography and reactive ion etching. With several cleaning procedures and physical dicing, we can produce these silicon nitride nanopore chips (Supplementary Figure 1.c) in a wafer-scale fabrication process flow.

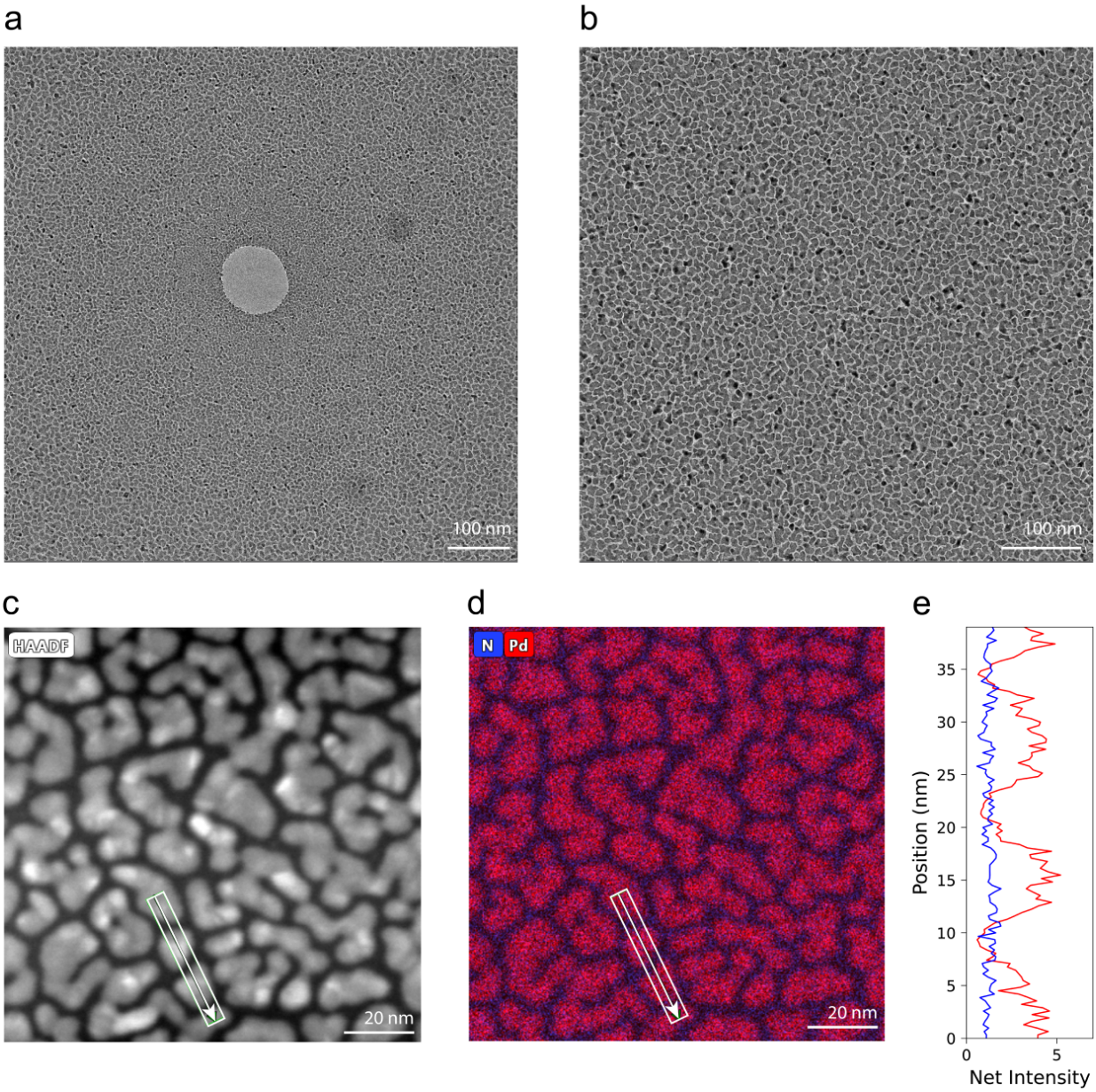


Supplementary Figure 1: **Wafer-scale fabrication of silicon nitride aperture. a,** A fabrication process flow based on the reactive ion etching to realize pattern transfer from PMMA photoresist to silicon nitride membrane. **b,** Pattern design on the backside of the wafer. **c**, Optical image of a single chip. **d,** The detailed dimensions of pattern design in **b**.

1.2 Step 1: Palladium deposition and characterization

Electron beam deposition is usually used to introduce metallic materials with a well controllable deposition rate. Due to the mechanism of electron beam vapor deposition, the landing of metal atoms on the surface of the target can also be taken as a condensation of atomic vapor. Thus, for depositing the metal that is not very adhesive on the silicon nitride surface, the usual process consists of depositing first an adhesive layer such as Ti or Cr. However, the direct deposition will cause a non-continuous and non-uniform layer of metal on the silicon nitride surface (supplementary Figure 2).[3]

For instance, here is the result that we deposited a very thin layer (2 nm) of palladium directly on the surface of silicon nitride aperture. Due to the condensation effect during metallic layer formation and the poor adhesive property of Pd on silicon-based surface, a non-continuous layer of Pd is formed with isolated island geometry (Supplementary Figure 2.a). This non-uniform morphology of Pd layer is due to the adhesive relation between metal and targeted substrate. Therefore, this

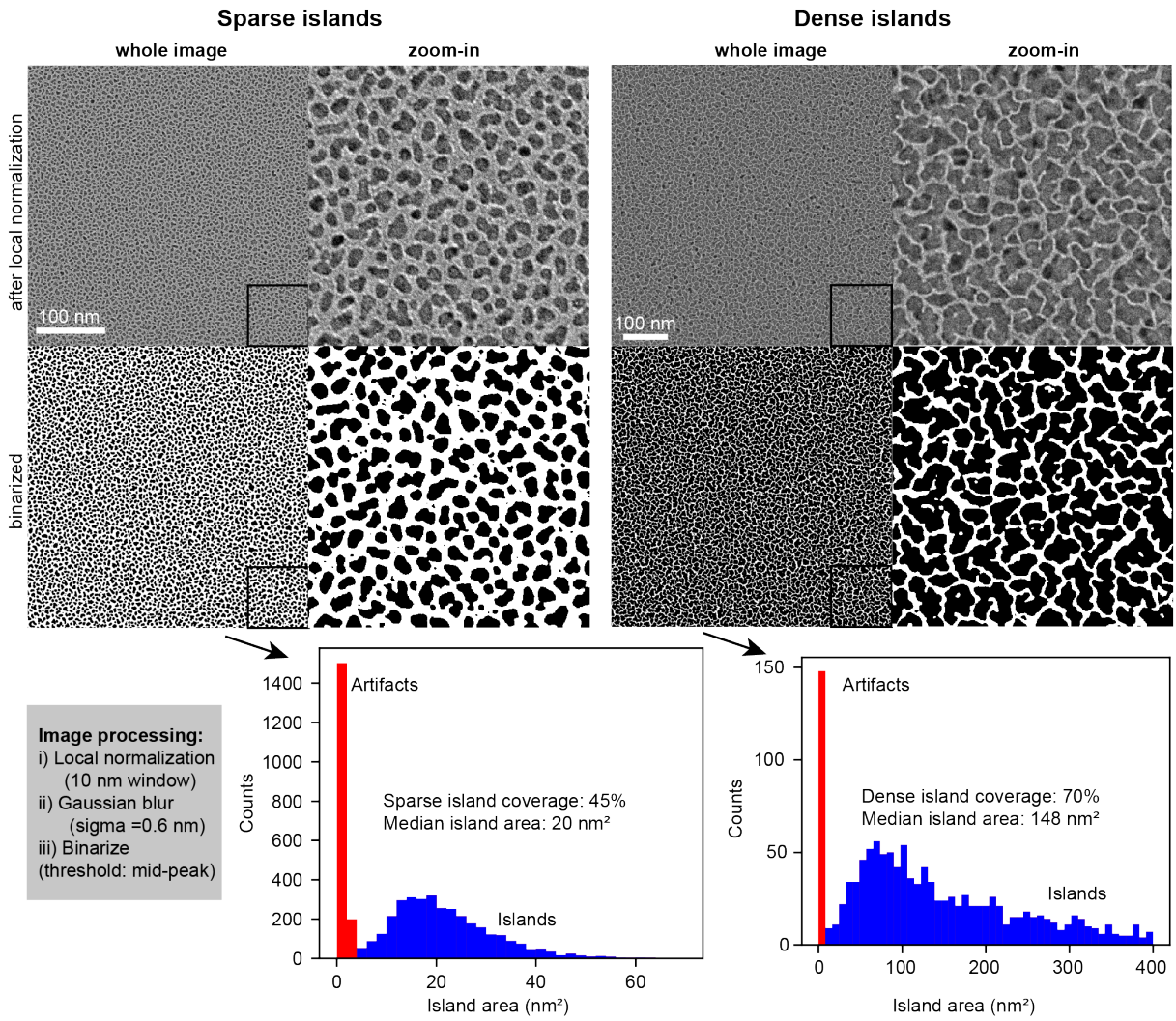


Supplementary Figure 2: **Transmitted electron microcopy analysis of non-continuous and non-uniform palladium layer on free-standing silicon nitride membrane** This non-continuous and non-uniform morphology is consistent on the surface of silicon nitride membrane around the aperture **(a)** or far from the aperture**(b)**. With the scanning transmitted electron microscope, the high angle annular dark field (HAADF) image **(c)** and EDX mapping **(d)** are provided to support the non-uniform distribution of Pd on the uniform substrate of silicon nitride. **(e)** is an extracted line analysis of Pd and N net intensity.

effect is consistent on the surface of silicon nitride membrane, the specific geometric feature, Pd island, could be observed both around (Supplementary Figure 2.a) and far from the silicon nitride aperture (Supplementary Figure 2.b). Furthermore, the EDX mapping (Supplementary Figure 2.d) is also provided to support the localization of Pd from the contrast in the STEM image (Supple-

mentary Figure 2.c). The net count signal of Pd and N on the write line also follows a similar geometric pattern. The alternative appearance of Pd along with a consistence N signal indicates the gap between island structure that would be the path for ions flux in the design of nanofluidic systems.

As shown in Supplementary Figure 3, we analyzed the TEM images to determine percentage of space occupied by the palladium islands for two devices with low and high island density, denoted as 'sparse islands' and 'dense islands' (the latter correspond to the device in Supplementary Figure 2). For dense islands, the coverage was found to be 70%, whereas the coverage was only 45% for the sparse islands. The image analysis pipeline consisted in local normalization[4], followed by Gaussian blur and finally binarization at the mid-peak point of the bimodally distributed image. The images were acquired slightly away from the silicon nitride aperture which ensures a continuous distribution of the palladium island.

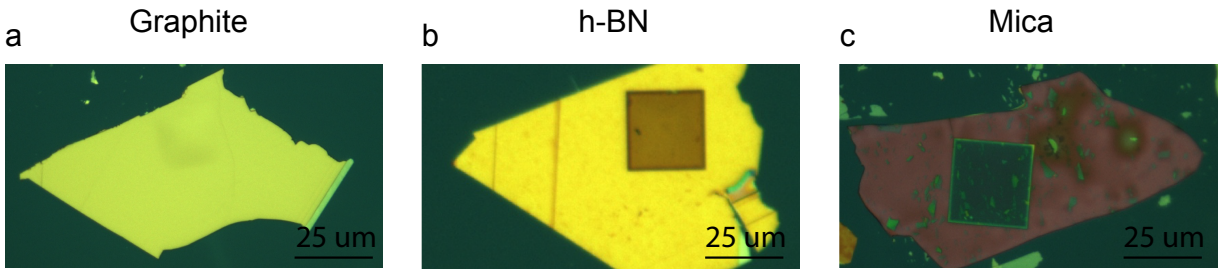


Supplementary Figure 3: **Quantification of the palladium island coverage for two different islands density**. Starting from the locally normalized TEM images above, we obtain the binary images at the bottom left following the protocol described on the top right. *ImageJ* was used for image processing, and local normalization was performed using the plugin Sage & Unser[4]. Following binarization, we obtain the island area distribution at the bottom right. The left peak (red, area < 4nm^2) corresponds to false positives in the detection of islands due to the imperfect binarization on noisy TEM images. We discard these small islands and count the island coverage by dividing the total area occupied by larger islands (blue, area > 4 nm2) by the image area, yielding a coverage of 45%. However, for the dense island device, such as (Supplementary Figure 2), the coverage is up to 70%.

1.3 Step 2: 2D material transfer

The chosen materials are exfoliated on Si wafer with a nitride layer of 200 nm thickness. A flat crystal with an area of minimum 20x20 microns is then selected. It is transferred using standard dry-transfer technique as detailed in methods section. The thin SiN window at the center of the chip with the hole in its middle constitutes the target. The only requirement here is that the hole

in the center has to be covered. The devices are then cleaned with acetone and isopropanol prior to the measurements. supplementary Figure 4 shows images of finished devices with different top layer materials.



Supplementary Figure 4: **Optical microscopy images of finished devices (a-c)**The Window can be observed in h-BN and Mica crystals which are transparent.

2 List of results per device

Supplementary table 1 report all experimental results in this work. For each device, the corresponding available experiments are listed as well as correspond figures. We also provide On-state, Off-state, and conductance ration under sinusoidal periodic operation for the experimental conditions presented.

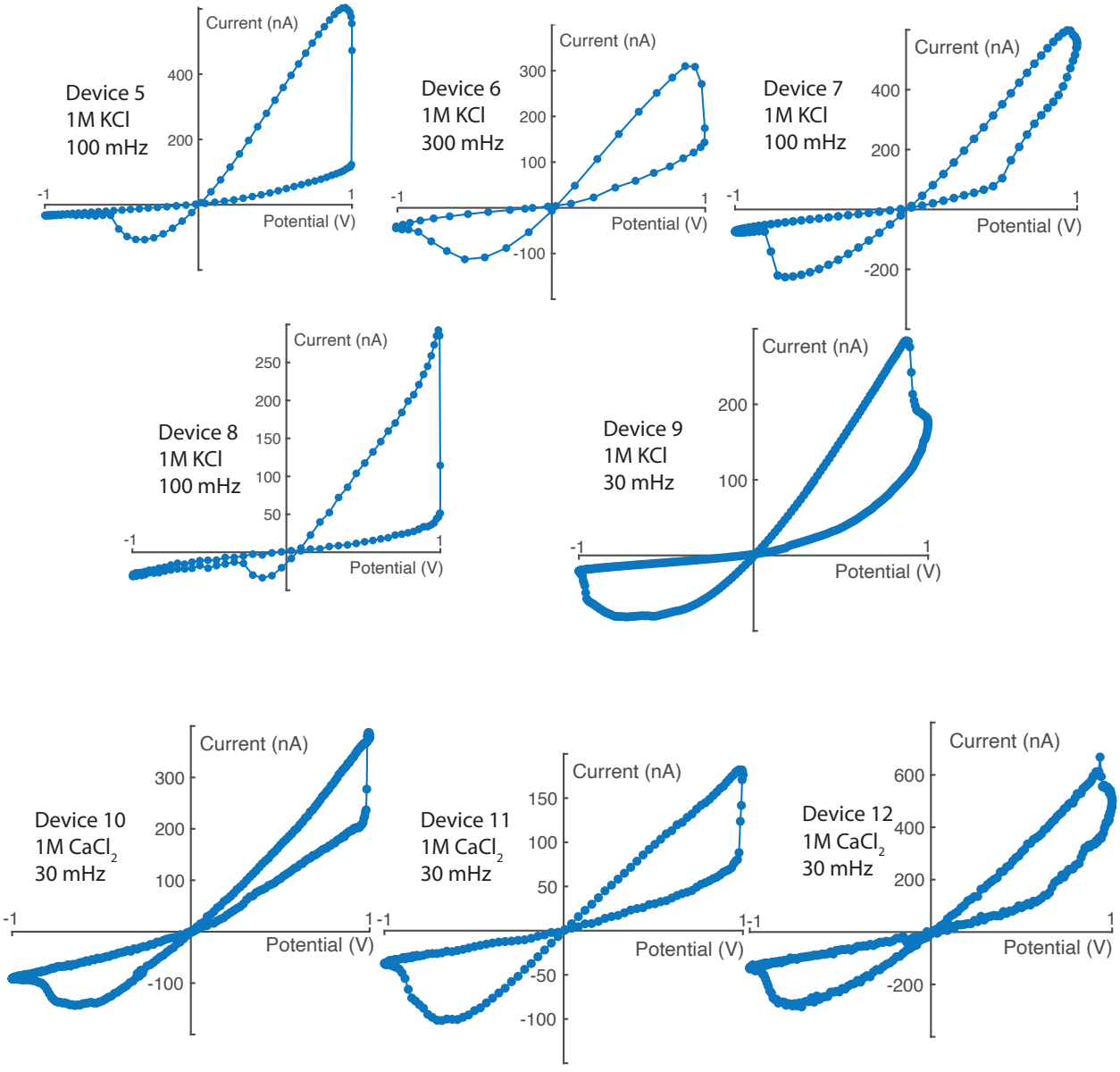
	Experiment (Figure or video)	Concentration	Species	Materials	G_{on} (nS)	G_{off} (nS)	$\frac{G_{on}}{G_{off}}$
Device 1	IV(F1), amplitudes(F2), charge(F2), pulses(SF7), frequencies (SF10)	1M	KCl	Graphite	120	6	20
Device 2	Optics(F3 and video 1)	1M	KCl	Graphite	224	6	37
Device 3	Logic(F4)	1M	KCl	Graphite	-	-	-
Device 4	Logic(F4)	1M	KCl	Graphite	-	-	-
Device 5	IV(SF5), pulses (SF6 and SF)	1M	KCl	Graphite	660	31	22
Device 6	IV(SF5), pulses (SF6 and SF17), stability (SF18)	1M	KCl	Graphite	370	23	16
Device 7	IV(SF5), frequencies(SF10), concentration(SF14)	1mM-1M	KCl	Graphite	596	62	10
Device 8	IV(SF5), frequencies(SF10), species(SF13)	1M	KCL, $CaCl_2$, $AlCl_3$	Graphite	276	17	16
Device 9	IV(SF5)	1M	KCl	Graphite	282	22	13
Device 10	IV(SF5)	1M	$CaCl_2$	Graphite	350	96	4
Device 11	IV(SF5), amplitudes(SF8)	1mM-1M (SF9)	$CaCl_2$	Graphite	187	33	6
Device 12	IV(SF5), amplitudes(SF8), pulses (SF7 and SF12)	1M	$CaCl_2$	Graphite	643	125	5
Device 13	amplitudes and waveform (SF9), stability (SF18)	1M	KCl	Graphite	606	64	9
Device 14	frequencies(SF10)	1M	KCl	Graphite	900	84	11
Device 15	pulses(SF12)	1M	KCl	Graphite	-	-	-
Device 16	concentration (SF14)	3mM-300mM	KCl	Graphite	422	15	26
Device 17	IV(SF15)	1M	KCl	h-BN	154	23	7
Device 18	IV(SF15)	1M	KCl	mica	300	125	2
Device 19	IV(SF15)	1M	KCl	mica	155	115	1
Device 20	pressure (SF16)	1M	KCl	Graphite	-	-	-
Device 21	pressure (SF16)	1M	KCl	Graphite	-	-	-
Device 22	concentration gradient (SF16)	1M	KCl	Graphite	-	-	-
Device 23	Optics (SF20 and video 2)	1M	KCl	Graphite	550	17	33
Device 24	Optics (video 3)	1M	KCl	Graphite	595	10	60
Device 25	Optics (video 4)	1M	KCl	Graphite	500	13	38
Device 26	Optics-LTP (video 5)	1M	KCl	Graphite	-	-	-
Device 27	Optics (video 6)	1M	KCl	mica	220	200	1
Device 28	Optics (video 7)	1M	KCl	mica	160	80	2
Device 29	logic (SF26)	1M	KCl	Graphite	-	-	-
Device 30	logic (SF27)	1M	KCl	Graphite	-	-	-
Device 31	logic (SF27)	1M	KCl	Graphite	-	-	-
Device 32	logic (SF28)	1M	KCl	Graphite	-	-	-

Supplementary table 1: **List of devices with corresponding experiments.** F is for Figure and SF is for Supplementary Figure.

3 Nanofluidic measurements with a single device

3.1 IV sweeps

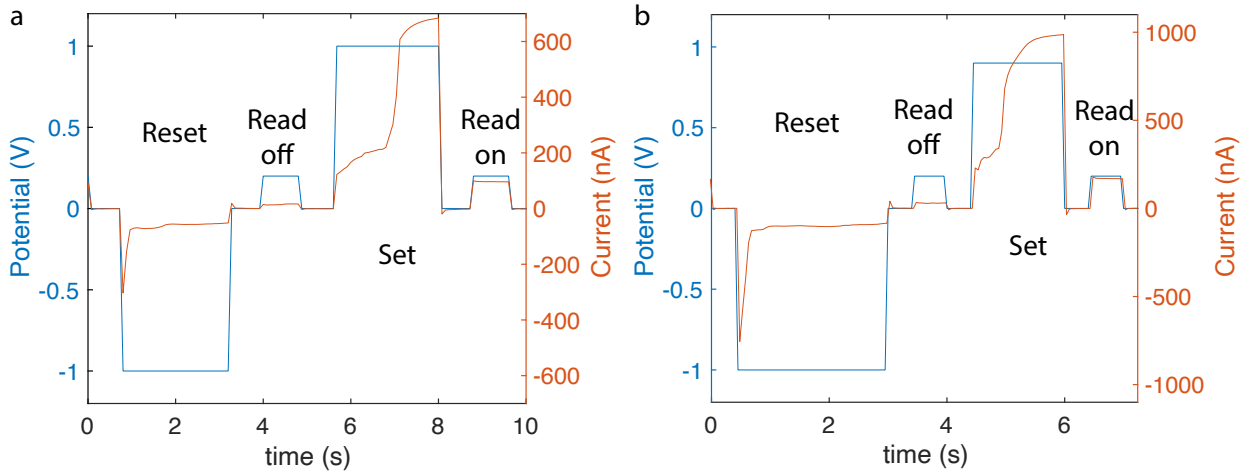
To demonstrate HACs' reproducibility and robustness we show IV sweeps on 8 different devices (Supplementary Figure 5) in addition the the one presented in the main text. It can already be noticed that the memory effect is stronger with KCl than $CaCl_2$. This is quantified in section 3.9.



Supplementary Figure 5: **IV sweeps.** Each graph is obtained with a different device. The frequency and salt is indicated for each device. For all devices the salt concentration is 1M and the top layer material is graphite.

3.2 Pulse programming

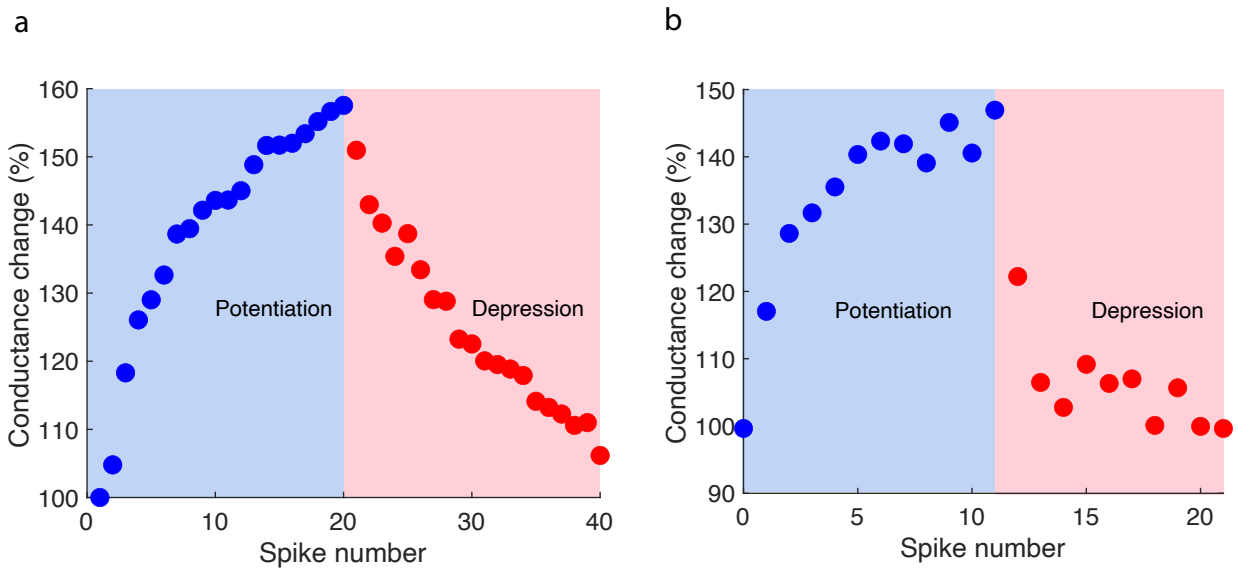
To check HACs' ability for neuromorphic computing we perform basic pulse programming operation (Supplementary Figure 6). The device is reset with a high amplitude negative programing pulse and set with a high amplitude positive pulse. The conductance can be measured with a low amplitude positive read pulse. The device can be reset or set with 2s programming pulse and read pulse in ON state is around five times larger than read pulse in OFF states.



Supplementary Figure 6: **Programing pulses. a,** Device 6. **b,** Device 5. The salt used is KCl at a concentration of 1M.

3.3 Setting at intermediate levels of conductance

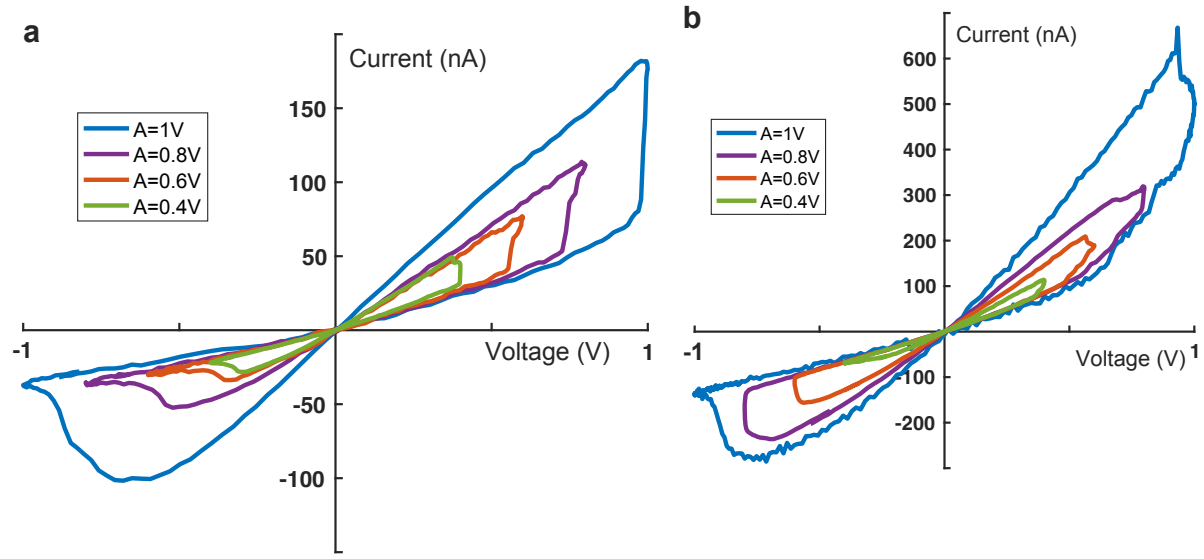
We check that HACs can be set to intermediate level of conductance by applying successive short voltage pulses (0.5-1s). Device are then reset progressively with negative voltage pulses of same duration. We observe that it is indeed possible to achieve intermediate level of conductances as shown in Supplementary Figure 7 thereby mimicking progressive synaptic potentiation and depression. This allow in principle the implementation of in-memory computing algorithm emulating more complex synaptic behavior like spike-timing dependent plasticity (STDP).



Supplementary Figure 7: **progressive potentiation and depression of HACs through intermediate conductance levels. a**, (Device 1-1M KCl). The conductance is increased (decreased) with programming pulses of +1V (-1V) with duration of 0.5s. Between each pulse it is accessed with non intrusive read pulses of 1s and 100mV. (Device 12-1M CaCl2). The conductance is increased (decreased) with programming pulses of +1V (-1V) with duration of 1s. Between each pulse it is accessed with non intrusive read pulses of 5s and 100mV. **b**, (Device 12-1M CaCl2). The conductance is increased (decreased) with programming pulses of +1V (-1V) with duration of 1s. Between each pulse it is accessed with non-intrusive read pulses of 5s and 100mV.

3.4 Additional data for sweeps at with different amplitudes

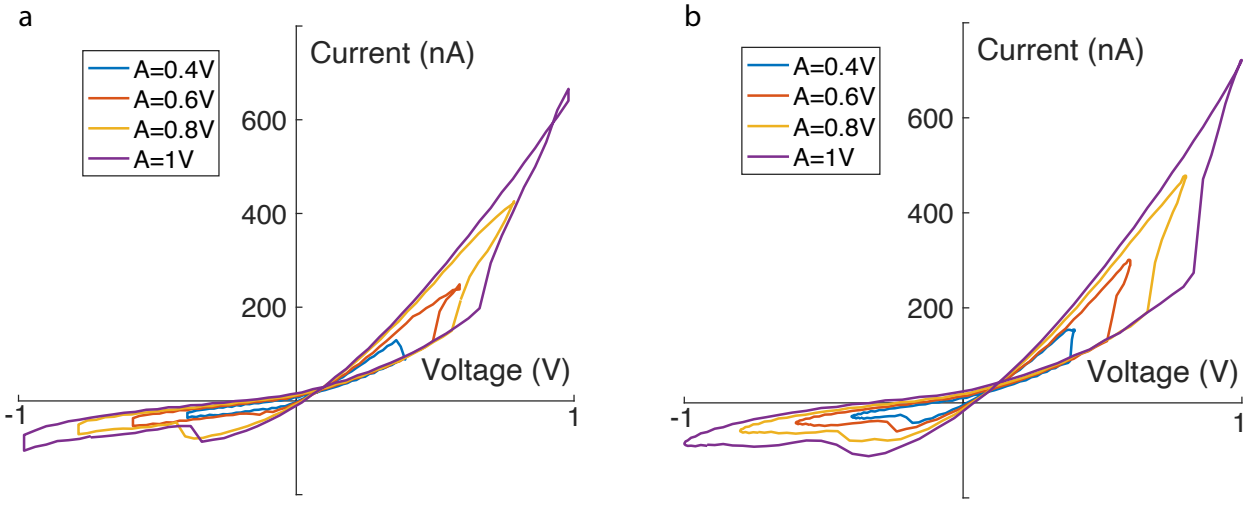
We provide in Supplementary Figure 8 additional data with applied sinusoidal bias of varying amplitude. We can notice, as for device A in Figure 2, that the voltage at which the switching occurs is dependent on the bias amplitude.



Supplementary Figure 8: **Sweeps with different amplitudes for two supplementary devices a,** Device 11, **b,** Device 12. The salt used is $CaCl_2$ at 1M and the frequency is 30 mHz.

3.5 Data for sweeps with different voltage waveform

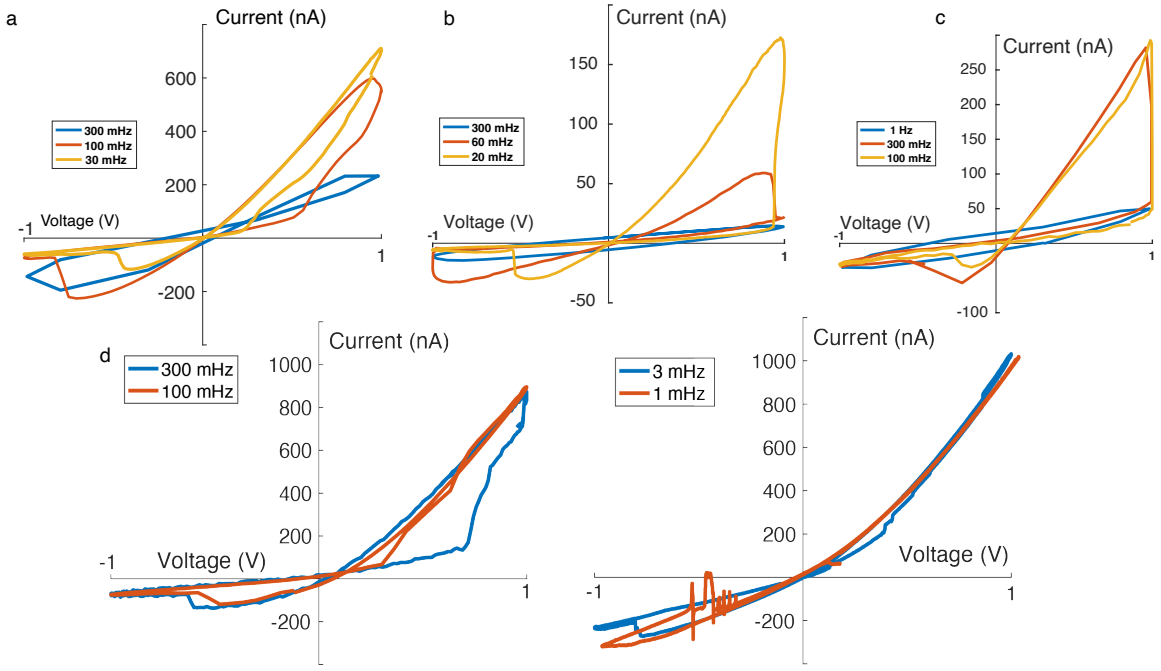
To verify if the effect had a strong dependance on the applied waveform shape, we compare in Supplementary Figure 9 sweeps at different amplitude using triangular and sinusoidal wave. While sinusoidal wave result in a slightly larger hysteresis as more time is spent at large voltage, we find that the waveform shape has little effect on the threshold.



Supplementary Figure 9: **Current-voltage (IV) curves at different amplitudes using triangular waves. (a) and sinusoidal waves (b).** Device 13 at 1M KCl. 100 mHz.

3.6 Additional data for sweeps at different frequencies

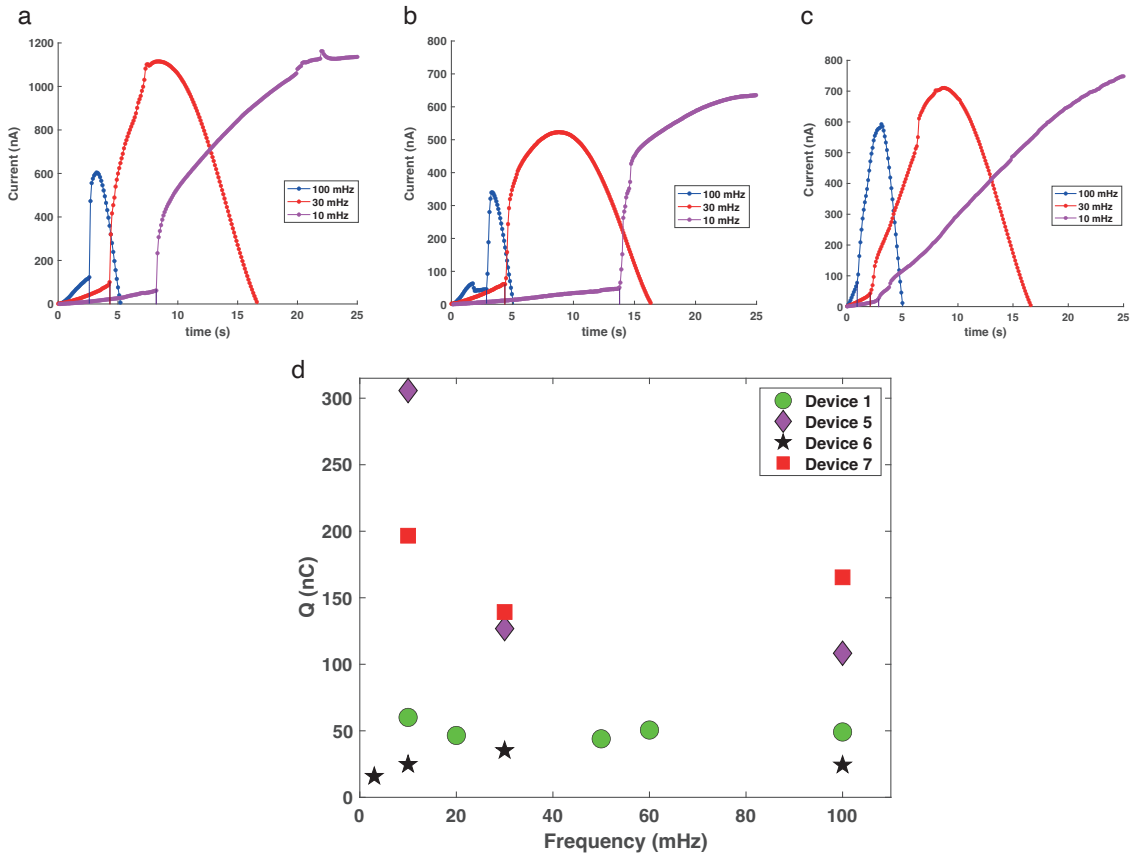
We provide in Supplementary Figure 10 additional data with applied sinusoidal bias of varying frequencies. At highest frequencies, the memristive effect disappears, leading to a ohmic behavior. Small ellipsoid can be observed because of capacitive effects. At lowest frequencies, the IV characteristic is diode-like (Supplementary Figure.10-d). We notice that slowing at low frequencies (below 10 mHz) seems to damage the device as recovering the OFF-state is not possible. Thus, application of high voltage for prolonged time should be avoided. This is however not required as memristors are expected to operate as fast as possible.



Supplementary Figure 10: **Sweeps with different amplitudes for two supplementary devices. a,** Device 7, **b,** Device 1, **c,** Device 8. **d**, Device 14. The salt used is KCl at 1M.

3.7 Additional data for the charge threshold

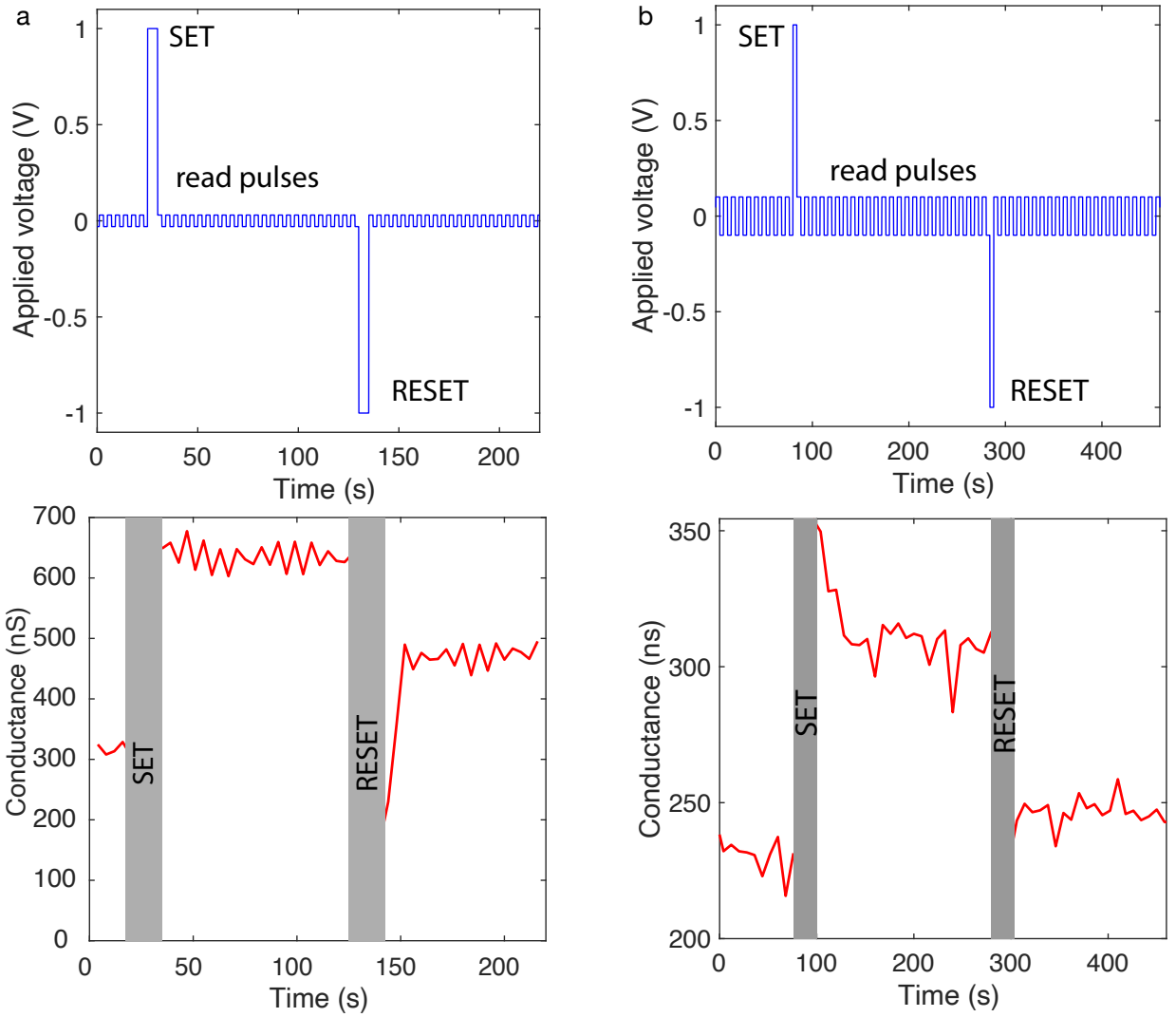
Following the same procedure as in main text Figure 2.b-c, we reported the charge threshold for three additional devices (Supplementary Figure 11.a-d). We find that the charge threshold varies by maximum three for a given device and is comprised in the 30-300 nC range for the four studied devices.



Supplementary Figure 11: **Additional data for charge threshold (1M KCl). a-c,** Setting of the device with sinusoidal potential of various frequencies for devices 5-7 respectively. The vertical dashed lines indicate the threshold time for each frequency. **d,** Charge threshold, Q, for various frequencies and devices. Device 1 is presented in the main text.

3.8 Memory retention

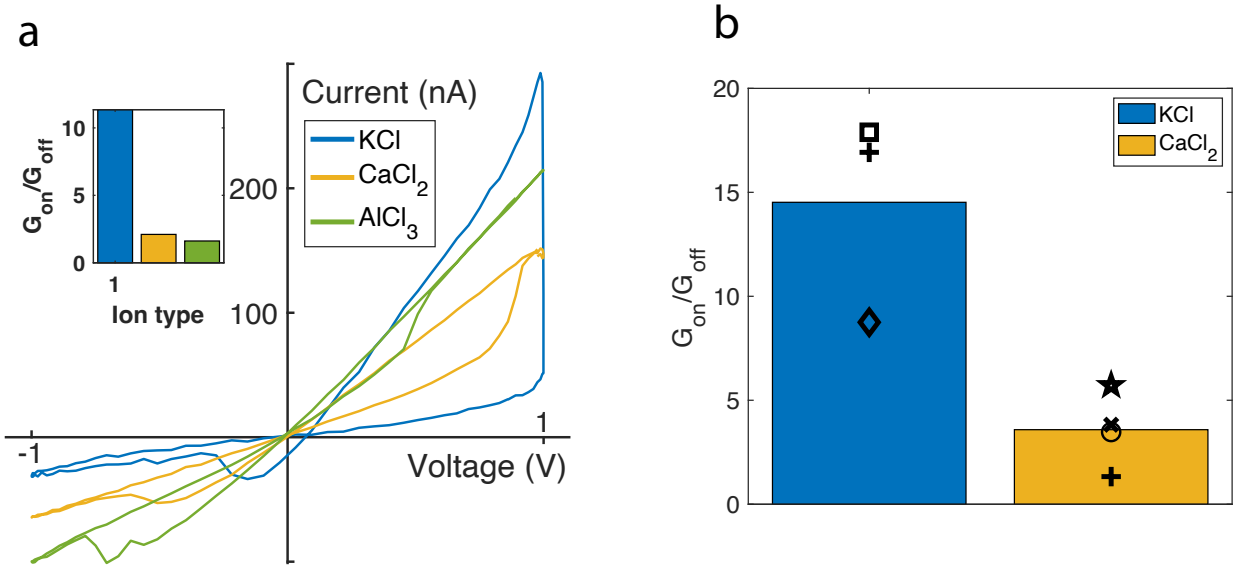
We check how the conductance evolve after setting/resetting in Supplementary figure 12. To do so we set/reset the device with positive/negative voltage pulses and access the conductance state with a weakly disturbing voltage pulse train of low amplitude oscillating around 0. We find that even if the conductance can experience an overshoot after setting/resetting (short-term potentiation) it does stabilize at a level higher (lower in case of reset) than its pre-pulse level. HACs thus indeed exhibit long-term potentiation. We repeat this experiment with optical feedback in section 4.



Supplementary Figure 12: **Implementation of long term potentiation with two devices. a**, Electrokinetic data (Device 15-1M KCl). The applied voltage is displayed on the top and the extracted conductance is shown on the bottom. The conductance is measured with voltage pulse train oscillating between $\pm$ 30 mV. The device is set/reset with a single positive voltage pulse of +/-1V and a duration of 5 seconds. **b**, Electrokinetic data (Device 12-1M $CaCl_2$). The applied voltage is displayed on the top and the extracted conductance is shown on the bottom. The conductance is measured with voltage pulse train oscillating between $\pm$ 100 mV. The device is set/reset with a single voltage pulse of $\pm$1V and a duration of 5 seconds.

3.9 Dependency with ionic species

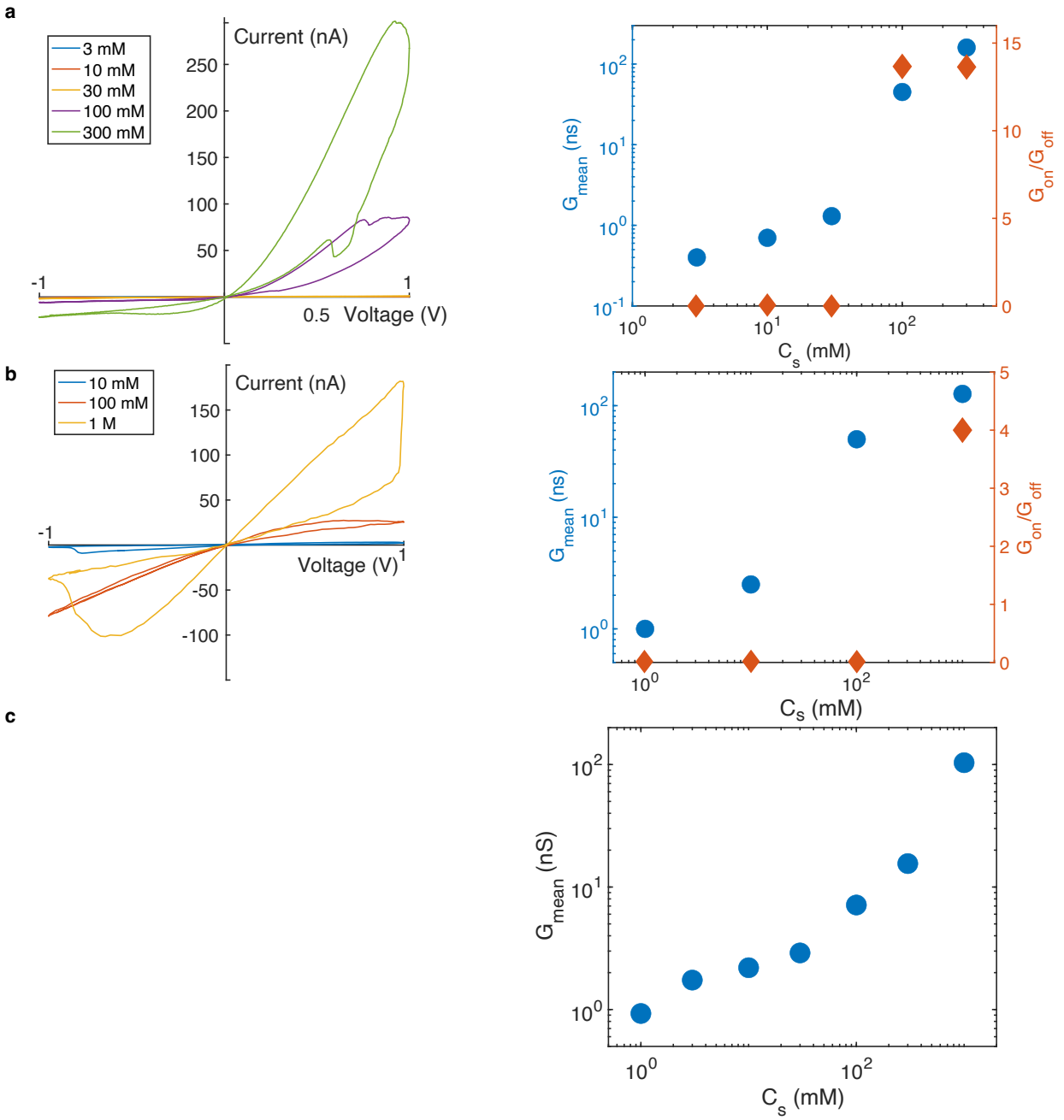
The memory effects increases with decreasing ionic valence and is maximum for KCl (Supplementary Figure 13.a-b).



Supplementary Figure 13: **Dependency of the effect with ion type (at a concentration of 1M). a,** IV characteristics with different salts for device 8. The frequency is 100 mHz. Inset: Extracted conductance ratio for the three salts. **b,** Comparison of conductance ratios between monovalent and divalent salts with 6 different devices. Each symbol represents a device. The frequency is 30 mHz.

3.10 Dependency with the salt concentration

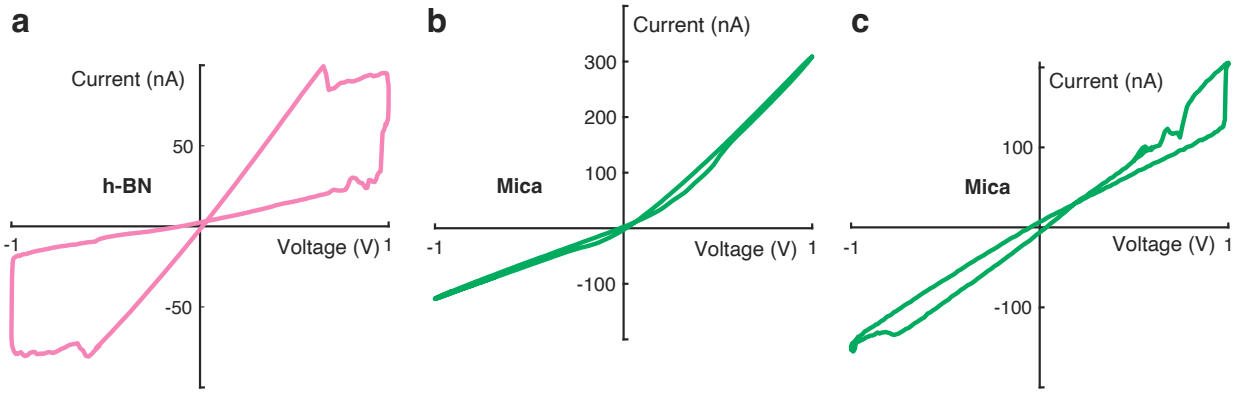
The memristor effect can be observed in HACs at concentrations higher than 100mM (Supplementary Figure 14.a-b). It can be noted that HACs are weakly conductive at concentration below 30-100mM (Supplementary Figure 14.a-c). Therefore the conductive, high-concentration regime, is where the memory can be observed.



Supplementary Figure 14: **HAC's conductance and conductance ratio with the salt concentration. a,** Device 16-KCl. Left: IV characteristics for different salt concentrations at 10mHz. Right: quasi-static mean conductance (Blue points) and conductance ratio measured at 10 mHz (red diamonds) at different salt concentration. If the memristive effect cannot be observed, the conductance ratio is defined as 0. **b,** Device 11-$CaCl_2$. Same panels and legend as **a**. **c,** Quasi-static mean conductance vs concentration for device 7-KCl.

3.11 Dependency with type of 2D material

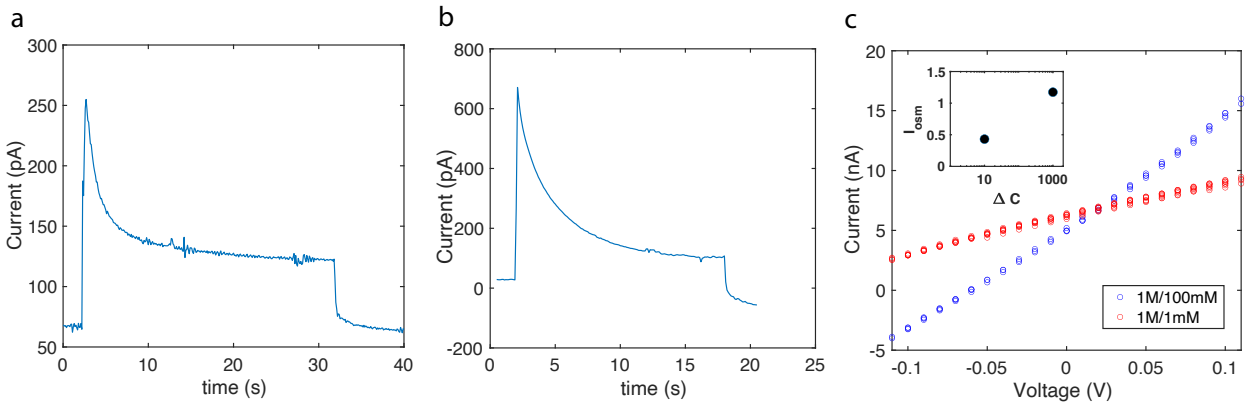
We changed the top layer material to further characterize the memory effect in HACs. We find that while the effect can still clearly be observed with a top layer made of h-BN, the IV characteristics with a mica top is quasi-linear (Supplementary Figure 15). This indicates that the effect is controlled by the surface charge coming from the top layer as mica bears a weaker surface charge relative to h-BN or graphite.



Supplementary Figure 15: **Dependency of the top material. (1M KCl-30 mHz) a,** IV sweep for a device with h-BN cap (Device 17) **b-c,** Device sweeps for two devices with mica cap (Devices 18 and 19).

3.12 Selectivity: streaming measurements

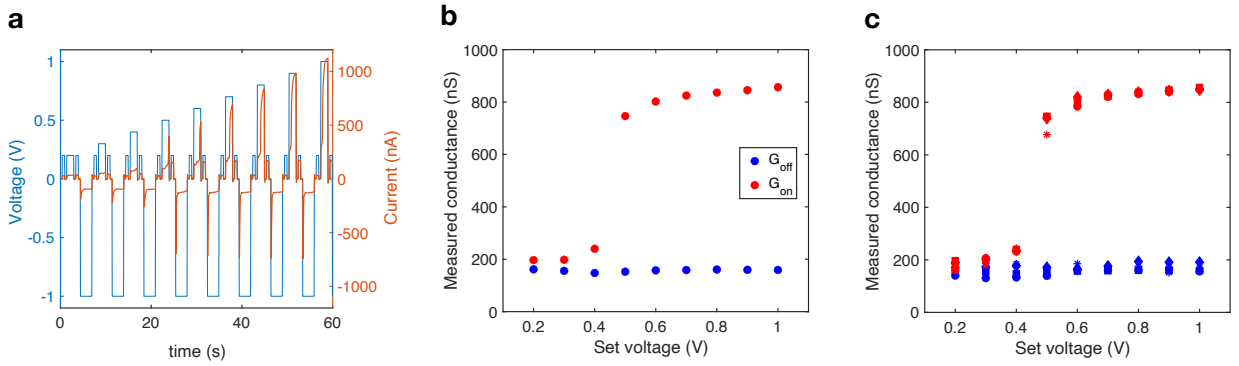
To verify that our device are indeed selective, we performed pressure-driven streaming currents measurements as well as osmotic currents measurements under salinity gradients (Supplementary figure 16). Under the application of pressure, ions are moved by advection generated by fluid-flow. While bulk-ions do not contribute to the current as cations and anions compensate for each other, excess counter-ions generate an ionic "streaming" current. Thus measuring a streaming current shows channel selectivity and its sign is related to the sign of the net surface charge. In our case, we measure positive currents while applying pressure at the working electrode reservoir which is the one where the 2D crystal and large entrance are. This is consistent with the measured osmotic currents under salinity gradients. Altogether, these results point to positive counter-ions (K^+) screening a negative net surface charge.



Supplementary Figure 16: **Selectivity control with pressure-driven ionic transport. a,** Device 20, 1M KCl. The applied pressure is 500 mbar. **b,** Device 21, 1M KCl. The applied pressure is 500 mbar. **c**, IV curve of HAC at two different concentration gradients (Device 22). Inset: extracted osmotic currents. The osmotic currents are calculated as in Emmerich et al.[6] by subtracting the Nernst current to the current at V=0.

3.13 Setting with pulses of different magnitude and voltage pulses endurance tests

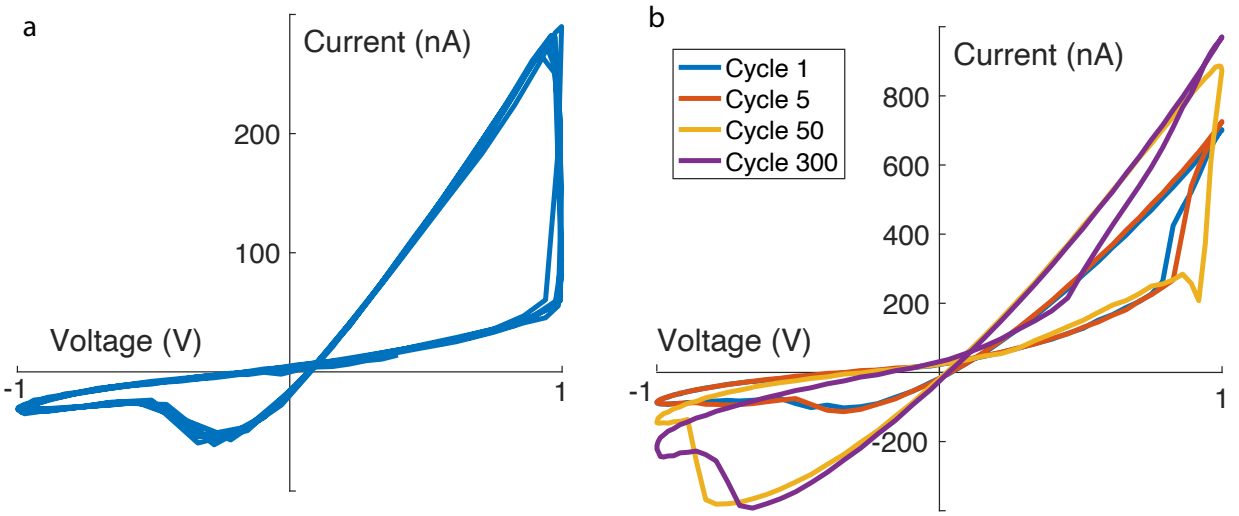
The IMP logic requires a switching threshold to be achieved correctly. In term of pulse programming, a setting threshold means that if a pulse is not high or long enough to reach the charge threshold, the conductance is weakly affected (V_Q^β in the IMP logic). On the other hand, If the pulse is sufficient to reach the charge threshold, the conductance will be strongly affected (V_Q^α in the IMP logic). Thus, even a small different of setting voltage can result in a large difference in output conductance. To verify that HACs indeed behave this way, we apply different setting voltages and monitor the change in conductance (supplementary Figure 17.a). We find that HACs are setted only for a voltage higher than a given value, as expected given the threshold dynamic and as required for IMP logic (supplementary Figure 17.a-b). We repeat this process four times and notice little variation (supplementary Figure 17.c). This demonstrates the stability of our devices which is also required to perform IMP logic where 8 setting/operation pulses are applied on each HAC.



Supplementary Figure 17: **Dependance on the magnitude of the programming pulse and stability-Device 5, 1M KCl. a,** Applied potential and resulting current (raw data). The conductance is measured with read pulses of 0.2 V and 0.5 s before and after the programming pulses. The programming pulses have a duration of 1.5s. Current during programming pulses exhibit an abrupt increase when the charge threshold is reached for programming pulses of voltages of 0.5V and higher like in the α-case of Figure 4.d. **b,** Conductance measured with read pulses before and after each programming pulses, extracted from **a**. This device is set for programming pulses larger thane 0.4V. **c**, Repetition of **a-b** four times. Each symbol represents an iteration.

3.14 Endurance tests under sinusoidal potential

We checked the endurance of HACs using multiple applied sinusoidal voltage cycles We observe excellent stability over 7 cycles (Supplementary Figure 18.a). For a larger number of cycles, the IV curves can drift. Yet we could observe up to 300 cycles (supplementary Figure 18.b).



Supplementary Figure 18: **Endurance test with sinusoidal applied bias. a,** IV-characteristics for 7 consecutive cycles. Device 5, 1M KCl-300 mHz. **b**, A few extracted individual cycles among 300 repetitions. Device 13, 1M KCl-100 mHz.

4 In operando optical measurements

4.1 Setup

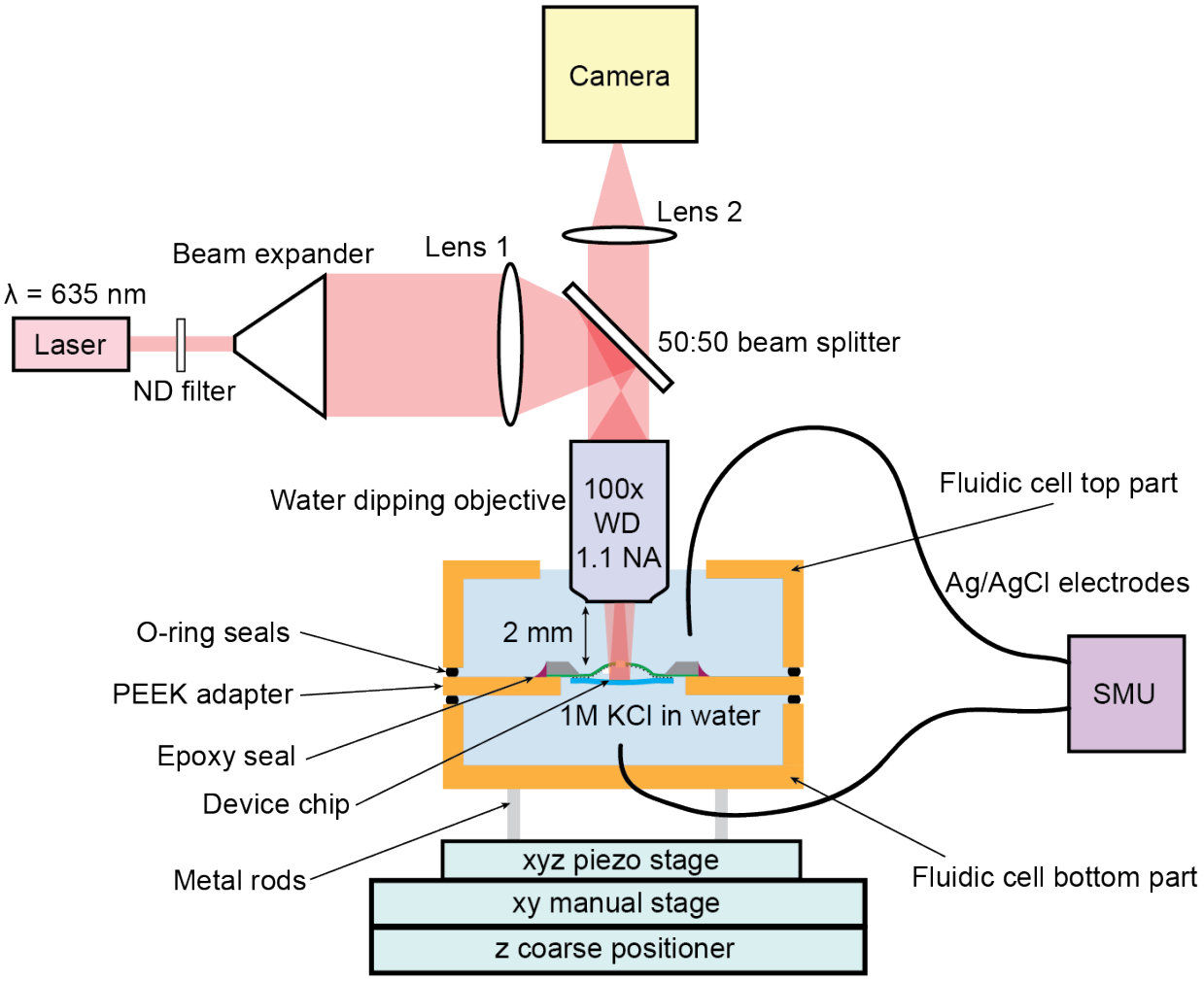
We performed in-operando observations using the setup sketched in supplementary Figure 19, where a water-dipping objective is used to image the device in a custom fluidic cell. As nanofluidic chips are smaller than the water-dipping objective, we designed a PEEK adapter (square with a 1 mm aperture) on which the chip was glued using epoxy resin (Araldite standard). We placed the chip upside down (graphite was facing down) to image inside the channels through the SiN window of the chip. This adapter was sandwiched between the two parts of the PEEK fluidic cell, held together by threads not shown on the sketch and sealed with O-rings. The bottom cell chamber had a leak-proof opening for the bottom electrode. The top cell chamber is open and has both the objective and the top electrode immersed. The objective used (Nikon CFI Plan 100XC W) has a working distance of 2.5 mm. The objective-sample distance was adjusted first coarsely using a z-positioner (conoptics M102A), and the sample was scanned using first a manual xy translation stage (Newport M-401). The optimal focus was found using finer motion control with a 3-axis piezoelectric stage (Thorlabs NanoMax 300).

4.1.1 Microscope details

The illumination light source was a 635nm continuous wave laser (Thorlabs HLS635). Its *som*1mW output was attenuated with ND filters (Thorlabs, E03/E04) to fill reach adequate illumination power densities. The gaussian beam size was enlarged in two steps: first through coupling the fiber output with a parabolic mirror (Thorlabs RC08FC-P01, 8 mm beam size output) and then by passing through a 2X adjustable beam expander (Thorlabs GBE02-A). Light was focused onto the back focal plane of the objective with an achromatic doublet lens (Thorlabs AC254-125-A-ML, 125 mm focal length). The objective was mounted at the bottom of a filter cube mount (Thorlabs DFM1L) which contained a 50/50 non-polarizing beam splitter (Thorlabs BS033), which directed 50% of the illumination light towards the sample and let through 50% of the light reflected at the sample towards the camera path. The image was formed on the camera (Hamamatsu ORCA Flash 4.0) using an achromatic doublet lens with a 200 mm focal length (Thorlabs AC254-200-A-ML).

4.1.2 Image acquisition and post-processing

The camera was controlled using Micro-Manager. The exposure time was set to 100ms to match the sampling rate of the electrokinetic measurements. The light intensity was adjusted to fill the camera dynamic range. The pixel size of 6.5 μm yielded a size of 65nm on the object plane, and a 4x4 binning was used in the acquisition to compress the images ($\sim$260 nm pixel size on the final image). Digital image rotation was applied when needed, and to remove laser speckle effects, images were denoised with a second-order low-pass Butterworth filter of cutoff frequency 0.05. Image processing was done using the Python library scikit-image.



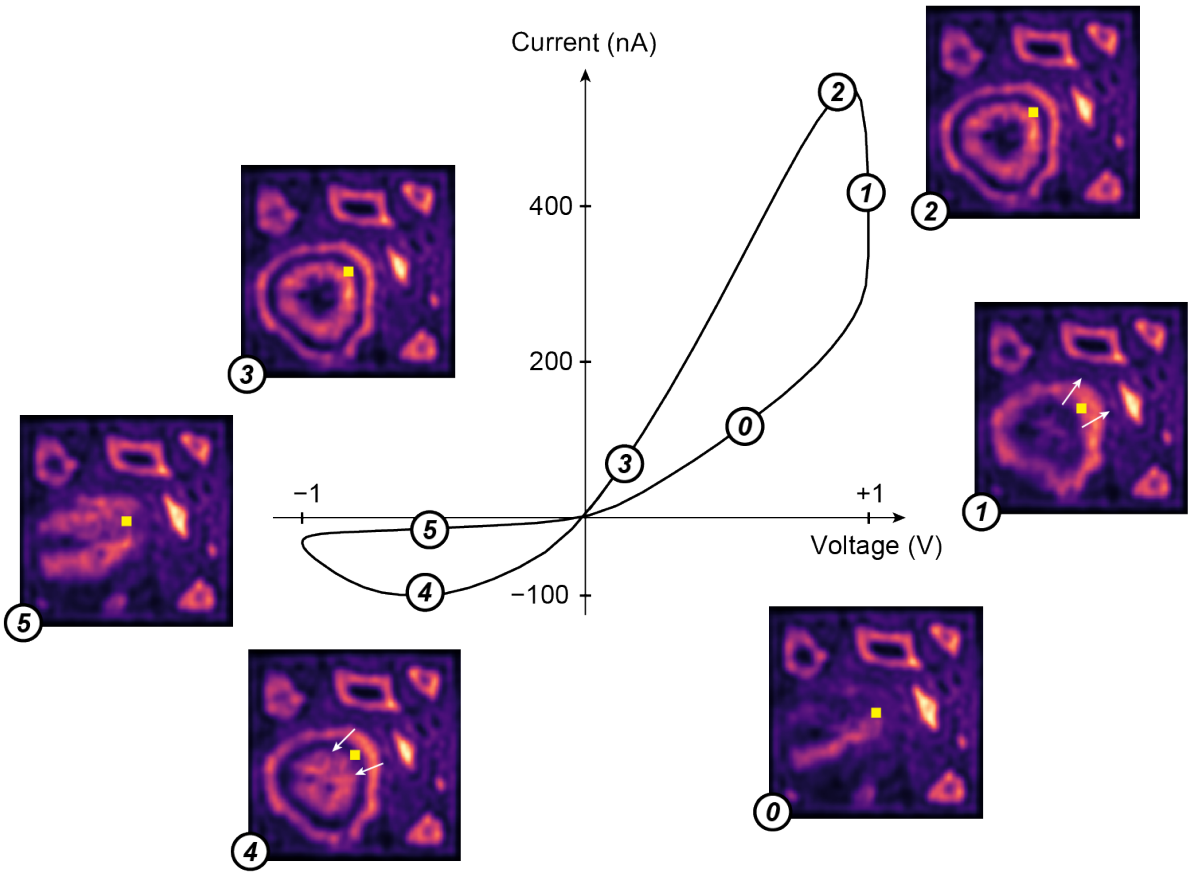
Supplementary Figure 19: **Setup for *in operando* optical measurements**

4.2 Additional Devices

In addition to the device presented in Figure 3 (Supplementary Movie 1) of the main text, we have measured six supplementary devices. Four are made with a graphite top layer (Supplementary Movie 2-5) and two are controls using a mica top layer (Supplementary Movie 6-7). One graphite device shows threshold mechanism similar as the one presented in main (Device 23). For the two other graphite devices (Devices 24 and 25), the blister forms directly at the pore location and the threshold is therefore attributed at some abrupt dynamic taking place outside of the SiN window and therefore the field of view.

4.3 Memory retention *in operando*

We performed *in-operando* memory retention experiment as was done in section 3. We find that the diminution of the conductance and its stabilization after setting is consistent with the evolution of the blister (Supplementary Figure 21 and Supplementary Movie 5). This demonstrates that the

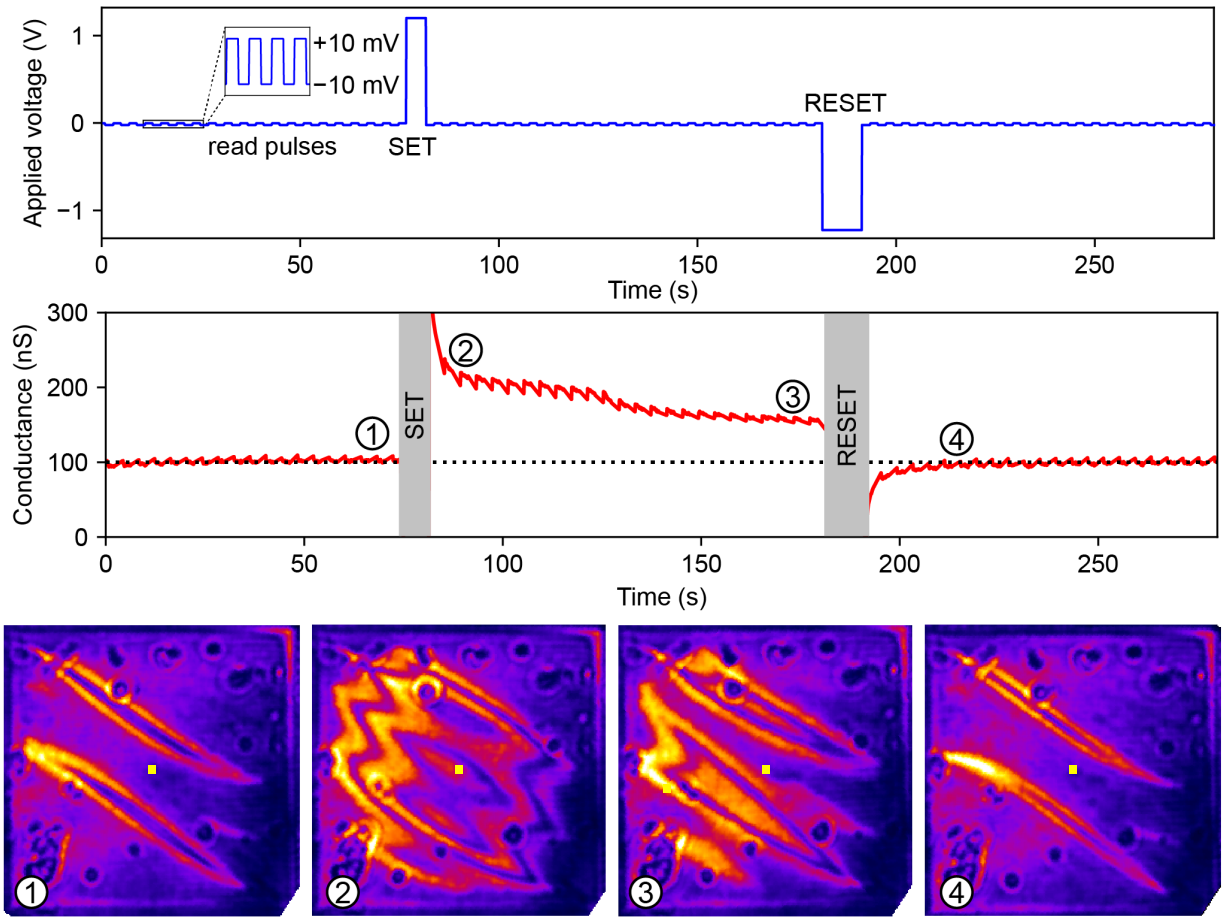


Supplementary Figure 20: **IV characteristic at (1V, 300 mHz, device 23) with optical images of the SiNx window at different time points marked by white dots and numbers.** White arrows illustrate blister motion and yellow squares mark the pore region.

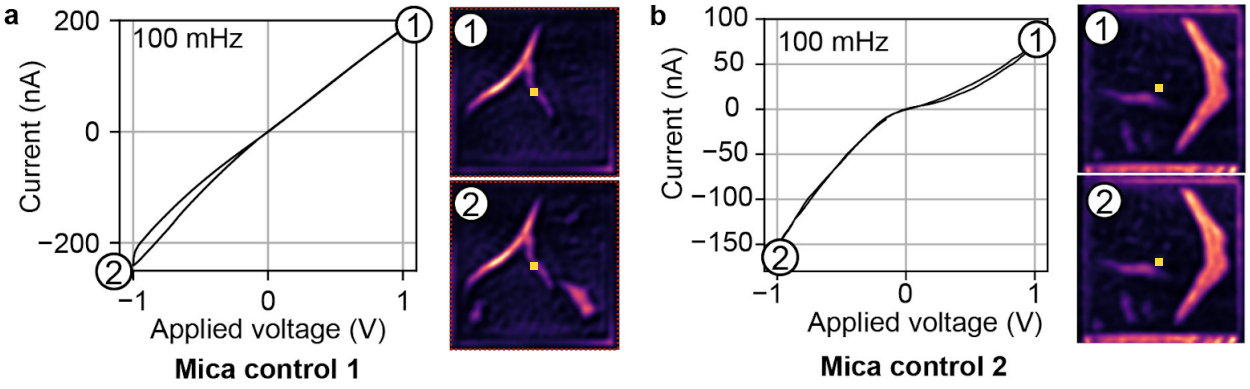
ability to mimic long-term potentiation exhibited by HACs is related to their blister dynamics.

4.4 Mica controls *in operando*

To confirm our hypothesis regarding the combined role of surface charge and adhesion of graphite to drive the memristive mechanism, we performed *in-operando* optical observations with two mica controls. As can be noticed in supplementary figure 22, there are some blisters in the vicinity of the SiN aperture. The main difference with graphite here is that the application of voltage has a very limited impact on the dynamics of these blisters. Interestingly, the limited blister formation observed for mica devices consistently appeared at negative voltages (outward pointing electric field), which seems to imply that these devices respond to anion motion rather than cation. We attribute this difference to a lower Σ^2/Γ of mica resulting in marginal mechanical deformations (Supplementary videos 6-7). Thus, mica-caped devices remain in an intermediate state of conductance with limited variation of their conductance. This intermediate level of conductance was observed consistently on four devices.



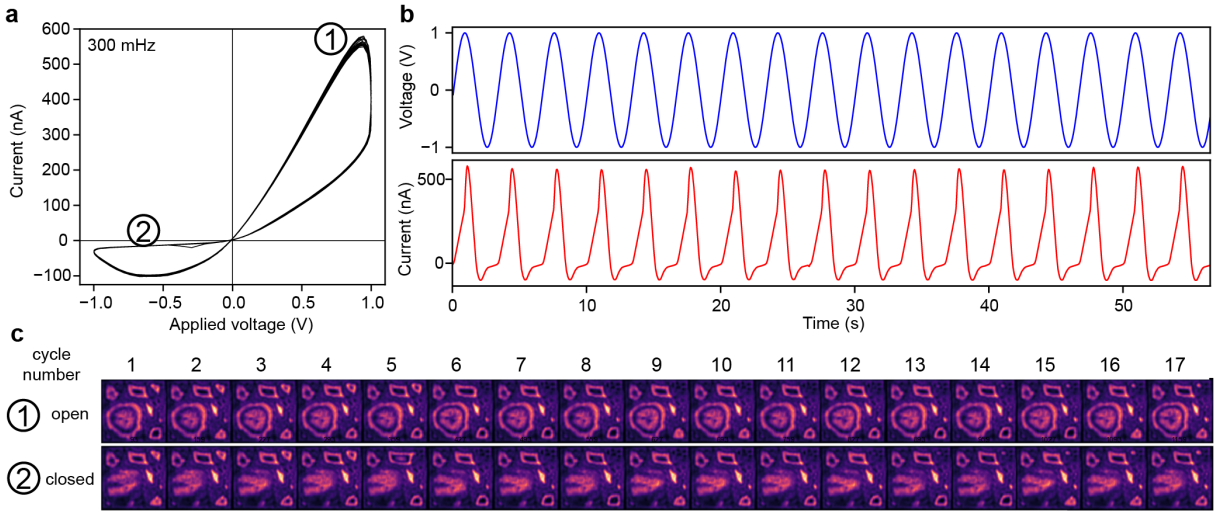
Supplementary Figure 21: **Memory retention experiment with optical feedback (Device 26-1MKCl)**. Applied voltage (top), resulting conductance (middle) and snapshots taken at times indicated in conductance panel (bottom). After setting, the blister recedes before stabilizing in agreement with the ON-state conductance. The reset pulse results in the blister shrinking and thus the return of the conductivity to the OFF-state value. The yellow square indicates the pore region.



Supplementary Figure 22: **Optical and electrokinetic results for two mica-caped devices under applied sinusoidal bias**. 1M-KCl-100 mHz. Yellow squares represent pore region. Device 27 (**a**) and 28 (**b**).

4.5 Endurance tests under sinusoidal potential *in-operando*

We observed optically the endurance of HACs *in-operando* using multiple applied sinusoidal voltage cycles. We find excellent stability of the memristive hysteresis as well as blister dynamics over 17 cycles (supplementary Figure 23).



Supplementary Figure 23: **In-operando measurements of 17 cycles-Device 23, 1M KCl. a,** IV characteristics of the 17 cycles. **b**, Applied voltage and resulting current in time for the 17 cycles. **c**, Snapshot extracted for each cycles corresponding to points in **a**.

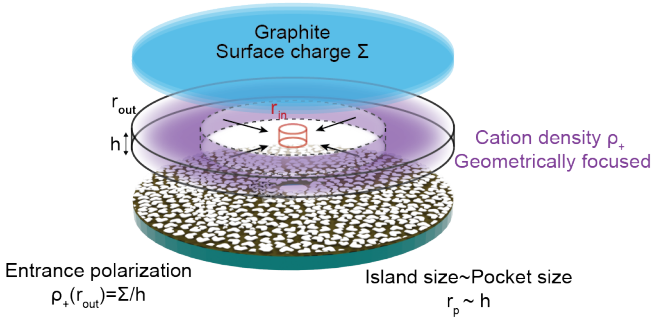
5 Theoretical analysis

Introduction

Nanofluidic devices with palladium islands combine asymmetry and confinement, resulting in distinctive physics, reflected in the very high rectification and abrupt threshold. Specifically, under sinusoidal excitation, they display a strongly nonlinear behavior, with a charge threshold followed by a rapid shift to a highly conductive state. We observed experimentally that this threshold is explained by mechanical deformations of the device, in which a liquid-filled blister reversibly forms. This blister responds to applied voltages and causes large conductance changes, including the abrupt threshold observed. We attempt here to rationalize (1) the device behavior in the OFF state, and (2) the ON/OFF conductance modulation through the blister dynamics. Then, we provide a plausible mechanism for the blister formation which involves (3) excess cation focusing to produce large net charge densities and (4) Coulomb repulsion overcoming the graphite/palladium adhesion.

5.1 The OFF-state conductance

We model the device in the OFF-state (in the absence of blister) as a hollow cylindrical slab of inner radius $r_{\text{in}} \sim 50$ nm, outer radius $r_{\text{out}} \sim 25$ μm and height $h \approx 5$ nm (Supplementary Figure 24), following typical device dimensions extracted from TEM images as shown in Supplementary Figures 2-3. We define the aspect ratio of the device as $a = r_{\text{out}}/r_{\text{in}} = 500$. The channel entrances exhibit a non-zero surface charge $\Sigma = 100$ mC/m^2 in accordance with previous reports for concentration-regulated surface charge on graphite[5;6]. A bias is applied to the device such that the electrostatic potential's value at the inner entrance is ΔV and its value at the outer entrance is 0.



Supplementary Figure 24: Key ingredients of the OFF-state model. The top graphite wall is charged and the entrance surface charge regulation ensures a net cation excess which is geometrically focused under the application of an inward electric field.

We first compute the OFF state conductance of the device, before moving to the mechanism for an increased conductance. We obtain this conductance through writing the following equations:

1. $E(r) = -\nabla V(r)$

2. $j(r) = \sigma E(r)$

3. $\nabla \cdot j(r) = 0 = \frac{1}{r}\partial_r\big(r j(r)\big)$

Where $E(r), V(r), j(r)$ are the electric field, the potential and current density, respectively. σ is the bulk conductivity of the electrolyte. For KCl at 1M, $\sigma = 10 S/m$.

We have $I = 2\pi r h j(r) =$ constant, therefore $E(r) = I/(2\pi r h \sigma)$. The potential thus reads $V(r) = \int_r^{r_{\text{out}}} E(r)dr = I/(2\pi\sigma h)\ln(r/r_{\text{out}})$. Using the boundary condition $V(r_{\text{in}}) = \Delta V$, we obtain the value of the device conductance:

$$G_{\text{OFF}} = I/\Delta V = 2\pi\sigma h/\ln a \tag{1}$$

Where $\ln(a) \approx 4.6$. As the conductance of a nanochannel with height h, width w and length L is $G_{\text{channel}} = wh/L \times \sigma$, we can note that the Pd island device conductance is equivalent to that of a nanochannel with dimensions h, $w = 2\pi r_{\text{in}}$, $L = r_{\text{in}} \ln a \approx 500$ nm. That is, **the conductance level of the device is governed by the inner entrance region**.

Evaluating this expression for reasonable parameters gives a conductance level close to the experimental OFF state. Therefore, the over-conducting ON is obtained with a modified geometry effectively leading to a partial short-circuit of the channel considered above.

Moreover, we obtained the full spatial distribution of the electric field:

$$E(r) = \frac{\Delta V}{r \ln a} \tag{2}$$

We observe that the electric field developed close to the inner wall is $\Delta V/(r_{\text{in}} \ln a)$ which is much larger than the field in a nanochannel with length r_{out}, by a field enhancement factor $a/\ln a \approx 80$.

5.2 ON/OFF conductance modulations and threshold due to blister displacement

The blisters observed experimentally give rise to thin film interference patterns with several fringes, indicating that the optical path difference between the light reflected above (SiN window) and below the blister (2D crystal) is on the order of a few wavelengths. Therefore, we observe micron-scale deformations. Ionic transport within the dynamical micro-channel formed by the blister is therefore unconfined and can be considered as a zero-resistance path. In other words, the blister short-circuits the nanofluidic circuit formed by the nanochannel network in between Pd islands. Depending on where the blister forms, it can have different effects on the device conductance. If it forms close to the pore, it will reduce the pore entrance and rescale the OFF-state conductance (as shown in section 5.1). Although a memristive response is expected in this picture, it does not explain the threshold as the blister can form gradually around the pore region. When the blister forms off-center, pronounced thresholds were observed and correlated experimentally with the blister crossing the pore region (threshold scenario 1, Supplementary Videos 1 and 2). We have observed another scenario leading to a threshold uncorrelated with the pore region crossing

(scenario 2), which we attribute to a blister extension outside of the window region (threshold scenario 2, Supplementary Videos 3 and 4)

For the devices exhibiting OFF-state conductance values compatible with the above description, we observed that the shift to the ON-state conductance matches the passage of the blister over the pore entrance region (threshold scenario 1). We can then rationalize the ON-state conductance in a simplified geometry as proposed in Figure 3d. When a small, off-centered blister of size negligible compared with the window size is present, it hardly affects the device conductance, and the conductance is very close to its OFF-state value $G_{\mathrm{OFF}} = 2\pi\sigma h/\ln(r_{\mathrm{out}}/r_{\mathrm{in}})$. When a blister with radius r_{blister} forms, it forms a short circuit such that the conductance is given by the remaining adhered channel network outside the blister, which reads:

$$G_{\mathrm{ON}} = 2\pi\sigma h/\ln(r_{\mathrm{out}}/r_{\mathrm{blister}}) \tag{3}$$

We can therefore note that the loss of resistance is simply given by the resistance of the formed blister: $R_{\mathrm{OFF}} - R_{\mathrm{ON}} = \ln(r_{\mathrm{blister}}/r_{\mathrm{in}})/2\pi\sigma h$ In this picture, the conductance ratio is given by:

$$G_{\mathrm{ON}}/G_{\mathrm{OFF}} = \frac{\ln(r_{\mathrm{out}}/r_{\mathrm{in}})}{\ln(r_{\mathrm{out}}/r_{\mathrm{blister}})} \tag{4}$$

This mechanism explains both the ON and OFF state, and the steepness of the switching threshold between these states is specific to the blister dynamics and position, which may vary from device to device. After these phenomenological considerations driven by *in-operando* imaging, we now rationalize the blister formation.

5.3 Blister formation: focusing charges to overcome adhesion

We propose that the observed blisters arise from electrostatic repulsion overcoming the adhesion force between the palladium islands and the 2D crystal. In the following sections, we show analytically that in the presence of a strong surface charge and confinement, it is possible to focus excess counter-ions geometrically. Then, we demonstrate that the obtained charge densities may be large enough to overcome adhesion.

5.3.1 Charge focusing enabled by the radially converging geometry

We show that the entrance counter-ions balancing the outer entrance surface charge can be focused geometrically by radially converging electric fields to higher concentrations inside the channels, which may lead to the breakdown of electroneutrality in the channels. This is reminiscent of the so-called 'spatially charged zone' asymmetric nanocapillaries[7]. The non-zero (negative) surface charge $-\Sigma$ of outer walls brings the local electroneutrality balance at $r = r_{\mathrm{out}}$:

$$-\Sigma + \rho^{o}_{+,D}\lambda_D = 0 \tag{5}$$

Which means there is a non-zero (positive) counter-ion density $\rho^{o}_{+,D} = Fc^{o}_{+}$ within the Debye layer close to the outer walls. Upon drifting towards the device center, we assume that ions will no longer be located within the Debye layer of thickness λ_D close to the wall, but rather dispersed over the whole height of the channel, leading to an overall decrease of the height-averaged concentration

$\rho_+^o = \rho_{+,D}^o \times \lambda_D/h$. In other words, for simplicity, we neglect out-of-plane concentration variations in the device driven away from electroneutrality, and simply write the boundary condition:

$$\rho_+(r_{\text{out}}) = \Sigma/h = \rho_+^o \tag{6}$$

We assumed here that at the outer entrance of the device, the diffuse counter-ion layer reaches equilibrium very quickly as it is in contact with the solution, ensuring the boundary condition equation 6 is verified at any time. However, the excess charge within the device is out of surface charge regulation equilibrium as it is not in contact with the reservoir. The exact fate of the excess charge distribution $\rho_+(r,t)$ under sinusoidal voltage cannot be easily computed, but we derive the result for the DC bias case below, showing that this charge can indeed be focused to higher densities geometrically.

5.4 Radially converging drift-diffusion DC model

5.4.1 Drift-diffusion in cylindrical coordinates

The full drift-diffusion equation in cylindrical coordinates reads:

$$\partial_t \rho_+ + v(r)\partial_r \rho_+ = D\big(\partial_{rr}\rho_+ + \frac{1}{r}\partial_r \rho_+\big) \tag{7}$$

Treating the excess charge density as a perturbation without back-action on the electric field distribution, the charge velocity field reads: $v(r) = \mu E(r) = \mu\Delta V/(r\ln a) := U/r$. The constant $U = \mu\Delta V/\ln a$ is negative for a positive bias applied, as we have inward motion of the excess cations.

5.4.2 Analytical solution

Cahn and Jackson[8] obtained an analytical expression for an ion distribution undergoing inwards radial drift-diffusion. The analytical solution of the problem for a δ point source reads:

$$\rho_+^0(\vec{r},s) = \frac{1}{\sigma_\parallel(s)\sqrt{2\pi}} e^{\frac{-\left(r\cos\theta - r_o(s)\right)^2}{2\sigma_\parallel^2(s)}} \times \frac{1}{\sigma_\perp(s)\sqrt{2\pi}} e^{\frac{-r^2\sin^2\theta}{2\sigma_\perp^2(s)}} \tag{8}$$

Where $\vec{r} \equiv (r,\theta)$ in polar coordinates, $s = t/T$, T is the electrophoretic time $T = R_{\text{out}}^2 \ln\alpha/2\mu\Delta V$, $r_o(s) = r_{\text{out}}\sqrt{1-s}$, $\sigma_\parallel = \sqrt{\frac{2DTs}{1+g_\parallel(s)}}$, $\sigma_\perp = \sqrt{\frac{2DTs}{1+g_\perp(s)}}$, $g_\parallel(s) = \frac{1+s}{2+s}$, $g_\perp(s) = -1 + \frac{s}{(1+s)\ln(1+s)}$, as derived by Cahn and Jackson[8].

More generally, the solution for a δ source at time 0 and position $(r_{\text{out}}\cos\phi, r_{\text{out}}\sin\phi)$ in Cartesian coordinates reads:

$$\rho_+^\phi(\vec{r},s) = \frac{1}{\sigma_\parallel(s)\sqrt{2\pi}} e^{\frac{-\left(r\cos(\theta-\phi) - r_o(s)\right)^2}{2\sigma_\parallel^2(s)}} \times \frac{1}{\sigma_\perp(s)\sqrt{2\pi}} e^{\frac{-r^2\sin^2(\theta-\phi)}{2\sigma_\perp^2(s)}} \tag{9}$$

As sketched in Supplementary Figure 25.a, we obtain the circle source solution by integrating over

the angle ϕ:

$$\rho_+^C(r,t) \sim \int_0^{2\pi} \rho_+^{\phi}(\vec{r},t)d\phi \tag{10}$$

Where the integration over ϕ suppressed the dependency over θ, granting the distribution radial symmetry. To obtain the solution with a constant flux of ions, this solution can be integrated with respect to time, yielding the constant flux source solution:

$$\rho_+^{CF}(r,t) \sim \int_0^t \rho_+^C(r,t')dt' \tag{11}$$

We evaluated ρ_+^C and ρ_+^{CF} numerically, to check whether the converging geometry enables charge focusing. Our analytical results demonstrate the possibility of geometrically focusing the outer entrance charge with the radially converging geometry, in such a way that the center region has an unbalanced charge density $\rho_+^{CF} - \rho_+^o$ where $\rho_+^o = \rho_+(r_{\text{out}}) = \Sigma/h$ is the part of the net charge that counters the wall surface charge Σ. As shown in Figure 25c and 25e, we obtain charge densities in the central region well above the outer wall surface charge, which open the door for unscreened Coulomb repulsion in the channels.

5.4.3 Blister formation at large charge densities

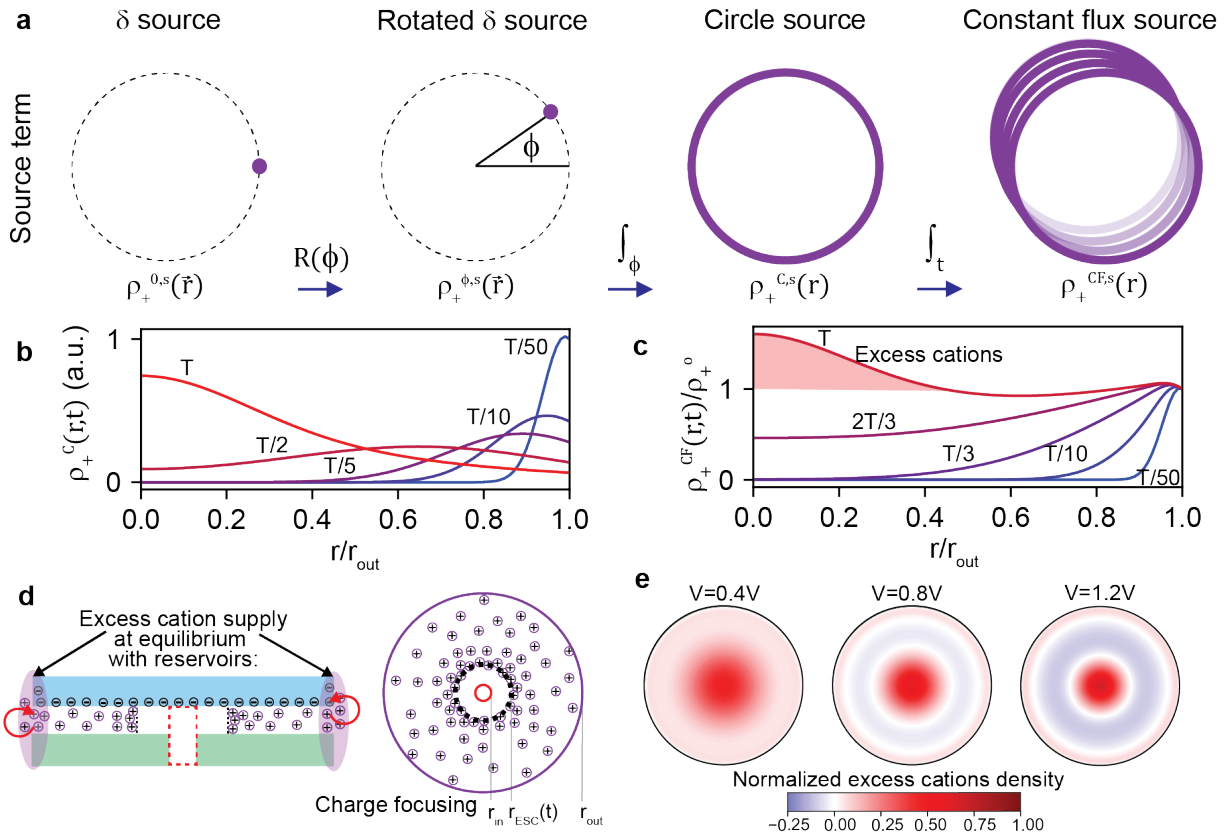
We demonstrated that we can up-concentrate counter ions in highly asymmetric channels with a radial geometry. We propose that the experimentally observed mechanical deformations arise from an out-of-equilibrium net charge density in the channels induces an electrostatic pressure which can overcome the van der Waals adhesion between the graphite and the Pd islands. The diversity of observations is largely modulated by the silicon nitride membrane strain distribution, which can provide yield points different that the center of the radially converging flow of counter-ions.

Inside a spherical pocket with radius $r_p = 5$ nm (size between the Pd islands) we have an excess counter-ion concentration c_+ and a net charge density $\rho_+ = Fc_+$ where F is the Faraday constant. Summing Coulomb repulsion energies over all ions within the pocket, we obtain a total energy of:

$$E_+ = K\frac{\rho_+^2\ r_p^5}{\varepsilon_o\ \varepsilon_r} \tag{12}$$

where the prefactor K is equal to $2\pi/15$ in a spherical pocket geometry. The volumetric energy corresponds roughly to an equivalent pressure of $P_+ \sim K\frac{\rho_+^2\ r_p^2}{\varepsilon_o\ \varepsilon_r}$. Metal islands are expected to screen any longer-range interaction between charges, making the interstitial pocket size the relevant dimension here. To get an order of magnitude of the magnitude of the effect, we can examine the expected pressures that should build up in the system with counter-ions concentrations accessible by the system. We expect an outer entrance outer surface charge $\Sigma = 100$ mC/m^2 for graphite in 1M KCl (value extrapolated from Emmerich et al[6]). This translates into a concentration $c_+^o = \Sigma/Fr_p \approx 300$ mM.

We write the electrostatic pressure as a function of the concentration of unscreened cations $P_+ \sim K\frac{F^2r_p^2}{\varepsilon_o\varepsilon_r}c_+^2$ and derive the proportionality coefficient between the pressure in bars and the counter-ion concentration in mM. This coefficient is equal to $10^{-5} \times 10^6 \times K\frac{F^2r_p^2}{\varepsilon_o\varepsilon_r} \sim 1$ mbar/mM^2.



Supplementary Figure 25: **DC model for geometry-induced cation focusing in HACs. a**, Construction of the constant flux source by superposition of δ sources. **b**, Time evolution of the circle source at t=T/2 and t=T (DC breakthrough time). **c**, Time evolution of the constant flux source, with the red highlighted part at t=T illustrating the excess cations exceeding the surface charge equilibrium. **d**, Sketch of the charge focusing, with a source at the outer entrance supplied by surface charge regulation at equilibrium with reservoirs. **e**, Radial profile of the excess charge charge distribution at t=T for different voltages V=0.4, 0.8 and 1.2V, normalized by the outer wall surface charge.

Therefore, while modest concentrations of 10 mM cause little electrostatic pressure (100 mbar), the quadratic dependency on the cation concentration can bring large pressure increases with an expected value of 10 MPa for 300 mM cation concentration. This is comparable with pressures estimated in 2D materials blisters[9]. We consider the appearance of a small blister of surface dS, small enough to consider that c_+ and thus P_+ are uniform, but large enough to consider that once the blister is formed, the excess charge is highly diluted and thus negligible. This should correspond to the 1-micrometer scale. We consider the energy change which reads:

$$dE = +\Gamma \times dS - K\frac{\rho_+^2 r_p^2}{\varepsilon_o\, \varepsilon_r} \times r_p\, dS \tag{13}$$

where the first surface term corresponds to the adhesion energy increase and the second volumetric term corresponds to the Coulombic energy decrease.

The blister formation becomes favorable when $dE/dS < 0$, that is the system can reduce its energy by forming the blister. The concentration threshold to obtain the blister formation reads:

$$\rho_+^* = \sqrt{\frac{\Gamma \varepsilon_o \, \varepsilon_r}{K r_p^3}} \tag{14}$$

Using an adhesion energy $\Gamma = 20$ mJ/m^2 in the range of 10% of measured (dry) graphite-metal adhesion energies[10], we obtain a critical blister formation concentration in the range of 0.5M, which should be attainable by a 2-fold concentration of the surface charge due to the radially converging flow.

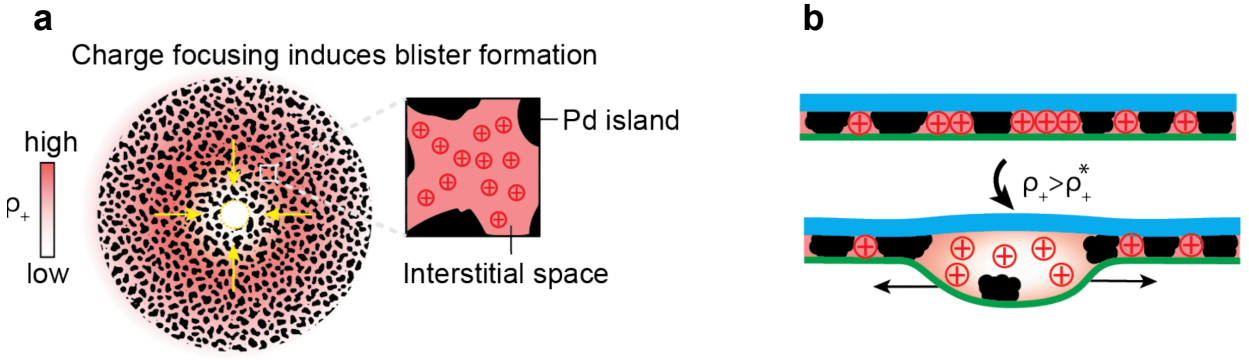
Merging the radial charge focusing picture with this instability reasoning for blister formation, we can group the adhesion and surface considerations as follows. The maximum charge density that builds up in the device is $\rho_+^{\max} = \Phi \rho_+^o = \Phi \Sigma / h$. Therefore, the criterion $\rho_+^{\max} > \rho_+^*$ for blister formation becomes:

$$\Phi \Sigma / h > \sqrt{\frac{\Gamma \varepsilon_o \, \varepsilon_r}{K r_p^3}} \tag{15}$$

We assimilate the device height h and the pocket size r_p and obtain the following dimensionless criterion:

$$K \Phi^2 \times \Sigma^2 h / \Gamma \varepsilon_o \varepsilon_r > 1 \tag{16}$$

Therefore, blister formation in the device is essentially governed by Σ^2/Γ, which should be large enough to enable the blister formation. This seems to be the case for graphite devices but not for mica ones. The other parameters depend on the device geometry and channel network properties (K, Φ, h). While we assumed for simplicity that the dielectric constant of water was its bulk value $\varepsilon_r = 80$, it may be reduced for the case of interfacial water[11], which would further enhance the predicted effects.



Supplementary Figure 26: **Charge focusing induces blister formation. a**, The blister formation occurs through the excess positive charge focusing in the radially converging channel network, yielding an increased cation density in the interstitial spaces between palladium islands. **b**, When this density exceeds a critical value, a blister forms to relax the electrostatic energy. Nanoscale blisters as pictured in **a** results in micron-scale blisters under sustained positivebiases, yielding features spanning the whole SiNx window.

These predictions are in line with the experimental observation that large KCl concentration

were required to obtain the memristive behavior of the devices (Supplementary Figure 14), as KCl is expected to regulate the surface charge of the 2D crystals. For time-dependent AC measurements, we rationalize the charge threshold reported in Figure 2 as follows: the blister formation criterion eq. (16) occurs fast at positive voltages and the charge threshold relates mostly to the blister dynamics where enough charges need to be brought to enlarge the blister past the pore. The threshold corresponds to flushing all ions and a possible delay for the blister dynamics, both of which are governed by the amount of excess charge focused into the device.

Where the blister forms

While the maximum concentration is expected to happen at the narrowest constriction - the pore entrance – we do not systematically observe that the blister forms precisely there. This observation can be rationalized as the radially convergent excess counter-ion up-concentration mechanism allows for parts of the device to reach the concentration threshold before the cation front reaches the pore. Moreover, as the actual geometry is not perfectly radial, the focusing might happen at pre-determined positions. An additional effect not taken into account so far is the possibility for the silicon nitride membrane to be pre-strained due to growth[12]. The pre-strain energy could assist in peeling the blister, thereby locally lowering the concentration threshold for blistering derived above. This pre-strain could not be controlled in our experiments and may explain variations in our devices regarding the location of the blistering and the abruptness of the threshold. However, it represents an avenue for further optimization of the devices in a controlled manner.

Second threshold mechanism: For devices presented in Supplementary movies 3 and 4, the threshold does not correlate with the blister passing over the pore, but rather with an abrupt volumetric change of the blister. The blister edge displacement accompanying the threshold is then located close the window edge. In this scenario, we attribute the conductance change to a blister extension close to the top flake edge rather than close to the pore center. This second mechanism yielding similar IV characteristics (with however a higher G_{OFF} as the blister is over the conductance-limiting region close to the pore) points to the importance of *in-operando* observations, and that of optimizing devices to control the blister motion which governs the memristor performance.

5.5 Elelctro-osmotic flow

We consider the electric field distribution as computed from the electrostatic picture:
$E(r) = \Delta V/(r\ln(a))$ where a is the aspect ratio of the device $a = r_{out}/r_{in}$, such that $\ln(a) \sim 5$. The electro-osmotic mobility $\mu_{EO} = -\varepsilon\zeta/\eta$ of carbon surfaces was reported to be in the range of $\mu_{EO} = 80.10^{-11} \times 50.10^{-3}/10^{-3} = 4.10^{-8}\ m^2/Vs$ from measurements of streaming currents (Emmerich Nat Mat 2022, using the formula $\mu_{EO} = -\varepsilon\zeta/\eta$ with the reported values of $\zeta \sim -50mV$ for pristine graphite in 1M KCl).

This gives rise to an electro-osmotic flow given by:

$$v(r) = \mu_{EO}\, E(r) \tag{17}$$

We now write Stokes equation that relates this flow to a pressure buildup:

$$\nabla P(r) = \eta \nabla^2\, v(r) \tag{18}$$

$$\partial_r P(r) = \eta\mu_{EO}\nabla^2 E(r) = \eta\mu_{EO}\Delta V/\ln(a) \times \nabla^2(1/r) \tag{19}$$

With $\nabla^2\ (1/r) = 1/r\ \partial_r\ (r\ \partial_r\ (1/r)) = 1/r\ \partial_r\ (-1/r) = 1/r^3$

Integrating, we obtain:

$$\Delta P = \frac{\eta\mu_{EO}\Delta V}{2\ln(a)}(1/r_{in}^2 - 1/r_{out}^2) \tag{20}$$

As $r_{in} \ll r_{out}$ this can be calculated as:

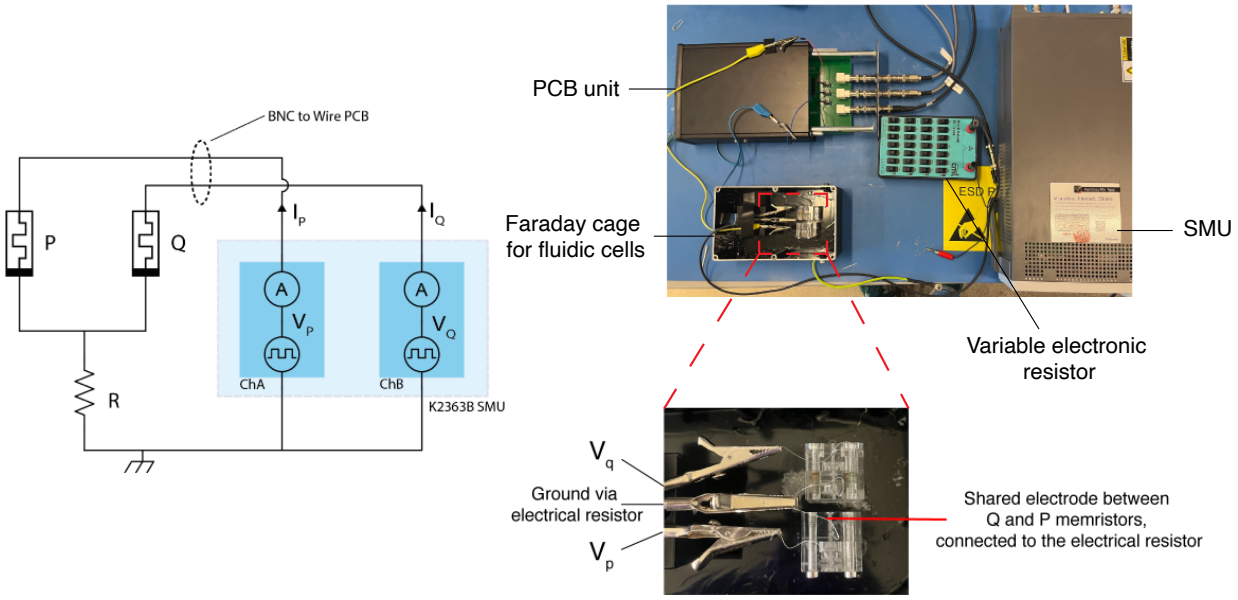
$$\Delta P/\Delta V = (\eta\mu_E O)/(2\ln(a)\ r_{in}^2\ ) = \frac{10^{-3} \times 4.10^{-8}}{2 \times 5 \times (5.10^{-8})^2} = 1600\ Pa/V = 40mbar/V \tag{21}$$

This pressure may enlarge pre-existing micron-scale blisters, modulating their size for as long as the voltage is applied. The memory retention would then be governed by the release of this pressure and possibly adhesion hysteresis.

6 Nanofluidics logic

6.1 Setup

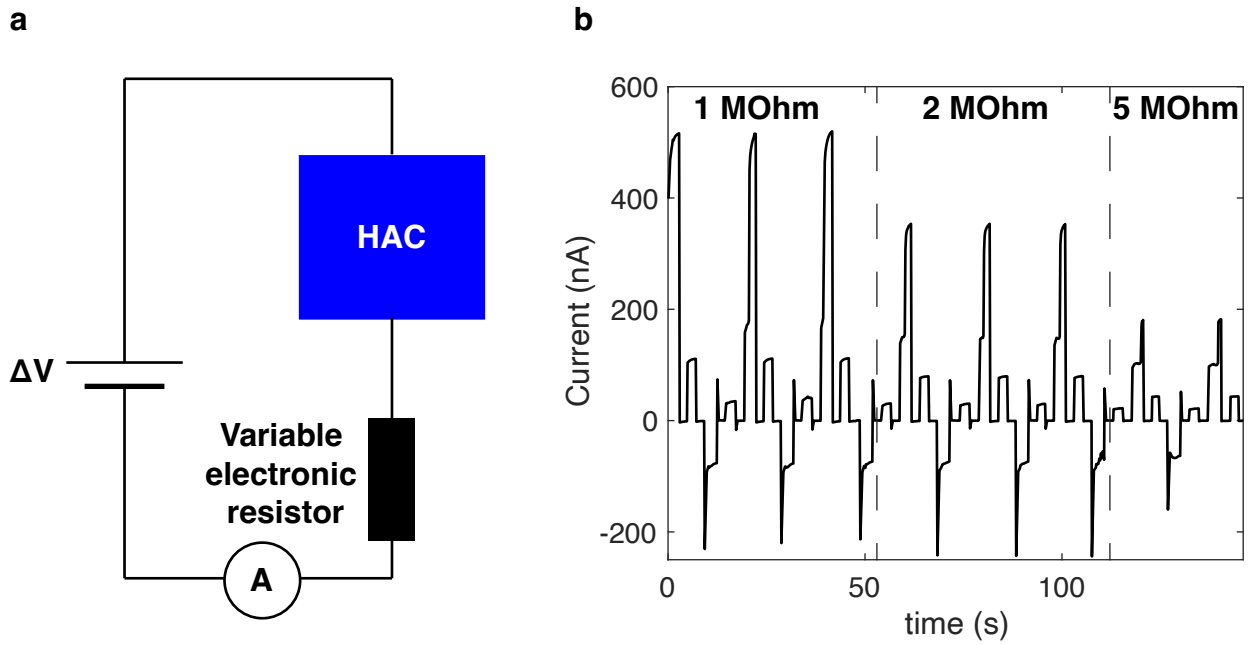
The details of the memristive logic circuit for the IMP gate implementation are shown in supplementary Figure 26. A source measurement unit (SMU, Keithley 2636B) provides the voltage imputs V_{q} and V_{p} for the two Q and P memristors involved in the IMP operation. In particular, all terminals belonging to the ionic cells consist of chlorinated tips connected by metal clips to the rest of the circuit. The metal clips are connected by wires to a printet circuit board (PCB) with header pins and BNC connectors. The BNCs are connected to the SMU, providing the Q and P terminals, as well as the ground. The common terminal shared between P and Q is connected to a variable electronic resistor. The other terminal of the variable resistor is connected to the instrument ground. The SMU allows us to force V_{q} and V_{p} while simultaneously reading I_{q} and I_{p}, thus retrieving the data presented in Figure 4 of the main text.



Supplementary Figure 27: **Setup for ionic logic. Left:** Details schematic of the circuit. P and Q represent both HAC channels. The electronic resistor is drawn in black. **Right:** Photography of the complete setup with a zoom on fluidic cells below.

6.2 One HAC with a resistor in series

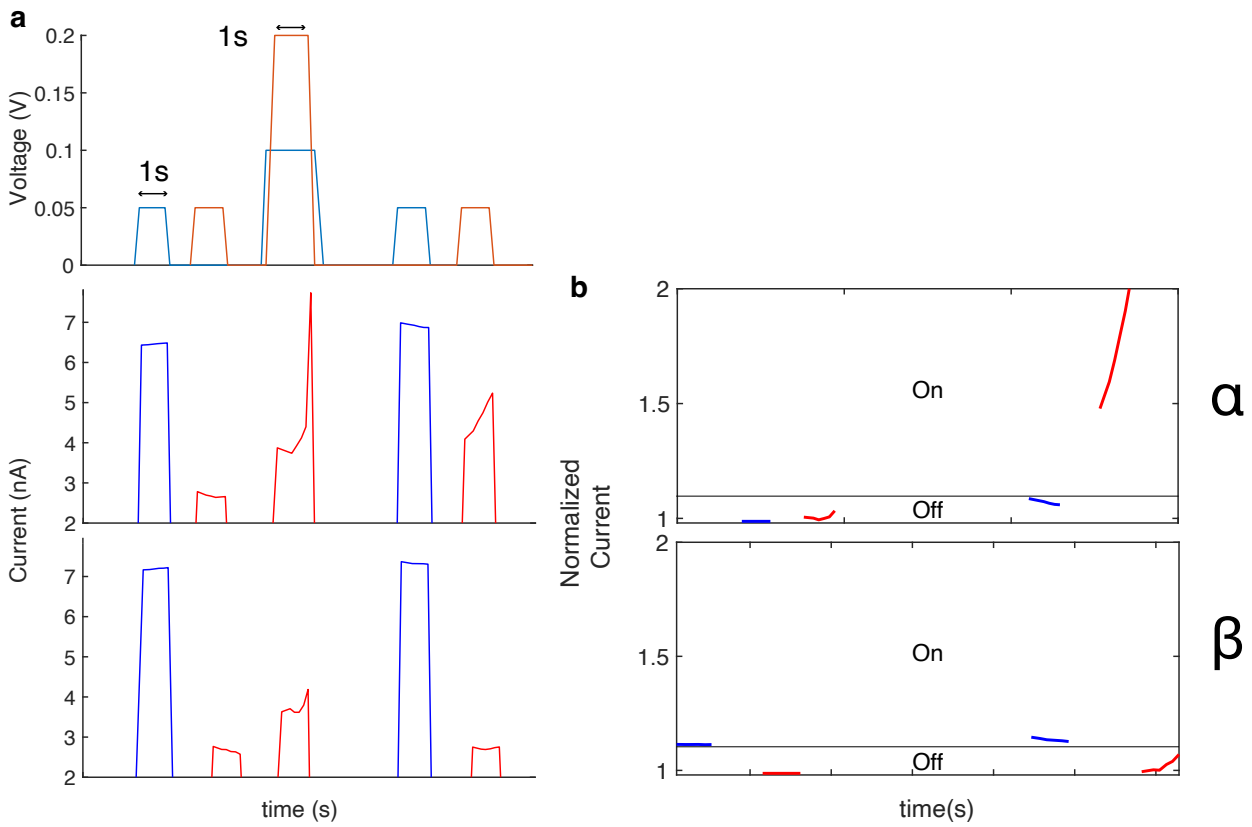
In the logic circuit drawn in Figure 4.a, HACs are connected in series with a variable resistor set to a few megaohms. As stated in the main text, a resistor placed in series with a memristive device will have a lower conductance ratio than the memristor alone. Upon the application of voltage, the memristor's conductance and thus the current will increase. This has the effect of increasing the voltage drop across the resistor hence decreasing the one on the memristor. We therefore connected a HAC in series with a variable electronic resistor in order to verify that the combination of these two component still behave as a memristor (Supplementary Figure 27.a). We used the same equipment as for the logic circuit (presented in the previous section) but plugged only one memristor. We find that HACs in series are still able to operate in this configuration, yet at the costs of a decrease in conductance ratio, which enables performing the IMP logic gate (Supplementary Figure 27.b).



Supplementary Figure 28: **HAC with a resistor in serie (Device 29-1M KCl). a,** Schematic of the circuit. **b,** Pulse-programing performances for different settings of the variable electronic resistor. Voltage pulse programming similar as in supplementary Figure 6 are applied repeatedly. The value of the electronic resistor is manually changed during the experiment.

6.3 Additional data with two HACs

For Robustness regarding ionic logic, we repeated the experiment presented in main text Figure.4, focusing only on the non-trivial cases. The results are presented in Supplementary Figure 28. For this pair of the device, the charge threshold was of lower value than the ones presented in the main text. This imposed working with pulses of lower amplitude and duration. In this experiment, the resistor was set to 4 MOhm.



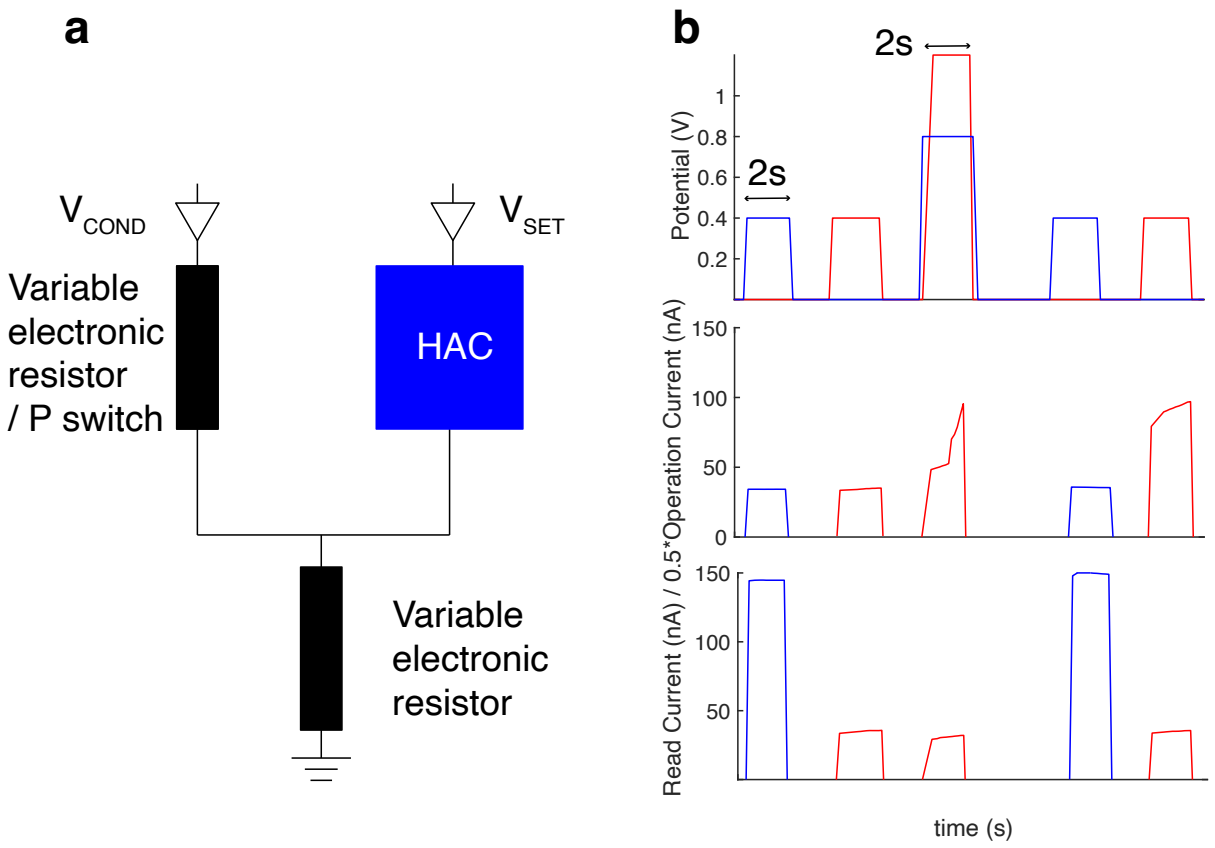
Supplementary Figure 29: **Supplementary data for ionic logic with two HACs (Devices 30 and 31-1M KCl). a,** Up: Applied potential for the P-memristor (in blue) and Q-memristor (in red). Middle: raw current data for the α case (P=0, Q switch). Down: Raw current data for the β case (P=1, Q does not switch). **c,** Normalized current data for the two cases presented in **b**. Each memristor's current pulses is normalized by its minimum value. The limit between ON and OFF states is placed at 10% of relative variation.

6.4 Additional data with one HAC and one tunable electronic resistor

For robustness regarding ionic logic, we also performed experiments with one HAC and two variable electronic resistors, as shown is supplementary Figure 29.a. The first electronic resistor plays the role of the P-switch and its conductance is manually changed during the experiment depending on the targeted state. Here we used 1 MOhm as ON state conductance and 10 Mohm as OFF state conductance which matches HACs. The second electronic resistor is set to 2 MOhm and remains fixed as for experiments with two HACs. One HAC is used as Q-switch. We find that we are indeed able to perform both non-trivial cases of IMP logic (supplementary Figure 29.b).

6.5 Numerical simulation

In this section, we reproduce the 'stateful' logic operation with a numerical simulation method under a similar condition that we have with ionic memristors. This simulation is based on the *Matlab, Simulink*, and *Simscape* packages.



Supplementary Figure 30: **Supplementary data for ionic logic with one HAC as the Q-switch and one programmable resistor as the P-switch (Device 32-1M KCl). a,** Schematic of the circuit. **b,** Raw data for IMP logic with applied potentials (up) and measured current for α case (middle) and β case (down).

6.5.1 Numerical model of the switching-threshold memristive device.

A classical numerical model of memristor in *Simscape* package is an ideal memristor with a nonlinear dopant drift approach[13]. Here we modify the model to achieve a charge-threshold dynamics. The state of the device will switch only when the total charge is beyond threshold value. The mathematic expression of charge-threshold memristive element can be written as following equations:

$$V = I \cdot M \tag{22}$$

$$M = \varepsilon \cdot R_A + (1-\varepsilon) \cdot R_B \tag{23}$$

$$q = \int I dt \tag{24}$$

$$\frac{d\varepsilon}{dt} = \begin{cases} 0, & \text{if } q < Q \\ \frac{I}{Q_s} F_p(\varepsilon) & \text{if } q \geq Q \end{cases} \tag{25}$$

$$F_p(\varepsilon) = 1 - (2\varepsilon - 1)^{2p} \tag{26}$$

Where, V is the voltage across the memristor, M is the dynamic resistor value of the memristive element, I is the current go through this device, R_A is the high conductive state resistance, R_B is the

low conductive state resistance, ε is the fraction of the memristor in state A, t is the time, q is the total charge that flux through the devices, Q is the charge-threshold to be overcome for initializing the state transition, Q_s is the total charge required to make the memristor transition from one state to another (when the state transition starts), $F_p(\varepsilon)$ is a 'window' function, which keeps ε between 1 and 0, and realize the zero drift at the boundaries of the device, and p is positive integer to control the exponential scale of state switch.

Compared with our modified model with ideal memristor accessible in *Simscape* Package, the devices conduct the stateful transition with the exact tendency but delayed with a consistence value of charge threshold, thus there are only limited influence on the reliability of the model. To be noticed that the definition of Q_s has been modified. Now in our modified model, Q_s and $F_p(\varepsilon)$ are used to controlled the shape of the transition curve, whereas the total charged required to the memristor transition from being fully in one state to being fully in the other state can be expressed as $Q_s + Q$.

6.5.2 Numerical simulation of 'stateful' logic operation circuit.

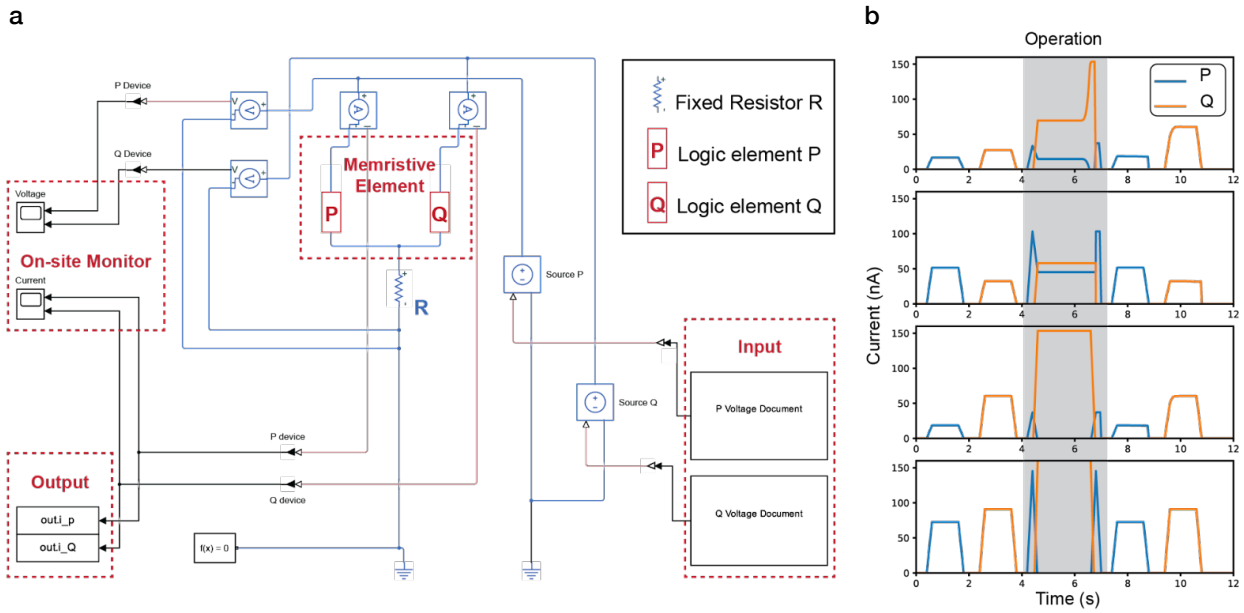
Based on this charge-threshold memristive model, we connect two of these devices in the following simulated circuit built in *Simulink*. With this simulated circuit, we can direct input the same voltage documents used in experimental section of 'stateful' logic operation (Figure 4) to run the simulation. By applying similar performance of real nanofluidic memristors that we have in experimental section (supplementary table 2), we could reproduce a similar circuit with a numerical model (supplementary Figure 30.a). Here, the threshold is several tens of nC and the transition ratio is 10. Different from real experimental situation, in which devices need to be set by prior voltage pulses, the conductance state can be manually set by defining the value of initial State A fraction ε_0, which '0' corresponding to low conductance state and '1' corresponding to the high conductance state. Here the fraction of State A $\varepsilon_(t_1)$ at alternative time t_1 is defined as following in the simulation:

$$\varepsilon_{t_1} = \varepsilon_0 + \int_0^{t_1} \frac{d\varepsilon}{dt} dt \tag{27}$$

Compared with Figure 4, Supplementary Figure 30 reproduce its result within a numerical simulated system. This result could support that, from the objective of simulation, the 'stateful' logic operation could be achieve with memristive switches displaying a conductance ratio of 5.

Component P	Values	Component Q	Values	Component R	Value
R_A	4 MOhm	R_A	2 MOhm	Resistance, R	6 MOhm
R_B	20 MOhm	R_B	10 MOhm		
Q_s	20 nC	Q_s	20 nC		
Q	130 nC	Q	130 nC		
P	2	P	P		

Supplementary table 2: **Detailed parameter of resistor and memristive elements in numerical simulated circuit model (Supplementary Figure 29).**



Supplementary Figure 31: **The 'stateful' logic operation circuit model and simulated current trace. a,** Artificial circuit model to simulate 'stateful' logic operation, including input section that capable to directly run voltage documents in Figure 4, on-site monitor, and output for current analysis. **b,** Simulated current of logic operations.

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