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Coexistence of high performance resistance and capacitance memory based on multilayered metal-oxide structures

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The Au/$DyMnO_3$/Nb:$SrTiO_3$/Au stack was demonstrated to be not only a high performance memristor but also a good memcapacitor. The switching time is below 10 ns, the retention is longer than 10^5 s, and the change ratio of resistance (or capacitance) is larger than 100 over the 10^8 switching cycles. Moreover, this stack has a broad range of intermediate states that are tunable by the operating voltages. It is indicated that the memory effects originate from the Nb:$SrTiO_3$/Au junction where the barrier profile is electrically modulated. The serial connected Au/$DyMnO_3$/Nb:$SrTiO_3$ stack behaves as a high nonlinear resistor paralleling with a capacitor, which raises the capacitance change ratio and enhances the memory stability of the device.

Metal-oxide junction is an ideal platform for investigating the fundamental physics of carrier transport across heterojunction, and is one of the most basic building blocks for practical electronic devices[1–3]. Generally, a Schottky barrier is formed at the metal-oxide interface due to the difference between the metal work function and the oxide electron affinity[1]. Electrical transport across the Schottky interface is well described by thermionic emission theory for lightly doped semiconductors, while it is dominated by quantum mechanical tunneling mechanism for heavily doped semiconductors[2,3]. Such Schottky junction usually displays the rectifying but non-hysteretic current-voltage (I-V) behavior as the core physics for Schottky diode[4].

Recently, however, remarkable hysteretic behaviors are also observed in many specially-engineered Schottky junctions, and the nonvolatile memory based on metal-oxide junction has been attracting increasing attentions due to their potentials for next-generation nonvolatile memory devices[5–11]. Under a pulsed voltage of different polarity, the junction demonstrates a reversible switching between nonvolatile high resistance state (HRS) and low resistance state (LRS)[11]. Many investigations indicate that this nonvolatile resistance switching can have different mechanisms[8,12–15]. One is the filamentary model, in which the junction barrier is locally destroyed (not simply modulated) and the conductive filament is formed while at other regions the Schottky barrier remains nearly unchanged[14]. It is frequently reported that, depending on the different concrete metal-oxide junctions, the conductive filaments across the junction are possibly formed/ruptured by redox process[14], migration of oxygen vacancies[11], or diffusion of atoms/ions of electrode metal such as Ag and Cu[16]. For this kind filamentary memory device, the switching between different resistance states is usually abrupt, and the random formation of filaments usually makes large fluctuations of both the resistance states and the operating voltages, which greatly weakens the reliability of memory devices[17].

The other one is the field-induced uniform or non-uniform modulation of Schottky barrier profile. It is well accepted that the interface state seriously affects the formation of the Schottky barrier, and the field-induced metastable modification of the interface state contributes to the memory effect[18]. For example, a metal-ferroelectric Schottky junction allows the charge redistribution at the junction interface due to the polarization reversion and as a result modulates the interfacial states as well as the interface barrier, inducing the nonvolatile resistance switching[10,19]. Ferroelectrics usually have very large resistivity due to the large band gap[20], while a large resistance of ferroelectric film would reduce or even conceal the differences between the HRS and LRS of whole metal-ferroelectric structure. Hence, for real applications, the challenge may be fabricating ferroelectric film with an intermediate band gap (~1.0–2.0 eV) or an ultrathin thickness (typically below 10 nm)[12].

In fact, for many specially-engineered metal-oxide Schottky junctions in which interfacial states as defect- and metal-induced gap states near the interface exist, the field-induced migration of oxygen vacancies or the carrier trapping/detrapping can also uniformly or locally modulate the interface barrier profile and results in the nonvolatile resistance switching[6,9,13,21]. A broad choice of oxides and well-developed technologies of doping and surface treatments provide a good platform for investigating the high performance memory on such junctions. In the carrier-trapping/detrapping-type memory junction, the variation of the Schottky barrier is continuous and remnant, and is well determined by the voltage pulse[22], which gives rise to the controllably multiple resistance states. In such junctions, however, the LRS is observed to be relaxing and its stability depends on the trap-depth and the reading voltage as well[23,24]. This issue remains to be overcome and substantial effort is still needed. Moreover, the field-induced variation of the Schottky barrier is usually accompanied with the change in the depletion-width[1], which would possibly bring out the nonvolatile capacitance switching effect[25], but rare related investigations have been reported.

In this study, we demonstrate the coexistence of resistance and capacitance memory based on a multilayer stack of Au/$DyMnO_3$/Nb:$SrTiO_3$/Au (Au/DMO/NSTO/Au). The memory effect comes from the NSTO/Au junction where the barrier profile is electrically modulated. The serial connection of Au/DMO/NSTO, which can be equivalent to a parallel of a high nonlinear resistor with a capacitor, greatly raises the change ratio of capacitance and enhances the memory stability of the device.

Results

Memory performance. Polycrystalline DMO thin films were grown on (111) NSTO substrates with 0.7 wt% Nb by pulsed laser deposition. The Au electrodes were fabricated by ion sputtering at room temperature. The schematic drawings of the fabricated Au(100 nm)/DMO(300 nm)/NSTO/Au(100 nm) stack memory cell and the measurement configuration are depicted in Figure 1(a). The virgin resistance state of the cell is at the HRS ($\sim 10^{10}$ Ω at 0.1 V). Figure 1(b) shows the pulsed write-voltage (V_{write}) dependent resistance measured at an electrical bias of 0.1 V after each different V_{write} (pulse width is fixed at 100 μs hereafter). It clearly shows a counterclockwise hysteretic curve between low ($R_L \sim 6.1 \times 10^6$ Ω) and high ($R_H \sim 7.8 \times 10^9$ Ω) resistance states, with a R_H/R_L ratio $> 10^3$ when V_{write} is swept in the $0 \to -10$ V $\to$ 10 V $\to$ 0 sequence (Figure 1(b), blue curve). The switching between the two states is not abrupt. The minor R-V_{write} loops in Figure 1(b) indicate a broad range of intermediate resistance states. These intermediate resistance states can be well tuned by the V_{write} pulse magnitude and pulse number. Figure 1(c) shows the pulse number dependent resistance switching from the LRS. It clearly demonstrates that a V_{write} pulse train with larger magnitude and larger pulse number switches the device from the LRS to an intermediate resistance state with a larger resistance.

Interestingly, the Au/DMO/NSTO/Au stack is also a good memcapacitive system[25]. In synchronizing with the resistance switching, the nonvolatile capacitive switching is also observed. With the same measuring protocol, a clockwise equivalent parallel capacitance (C_p) hysteresis between low capacitance state (LCS) ($C_L \sim 0.7$ pf) and high capacitance state (HCS) ($C_H \sim 1$ nf) is shown in Figure 1(d). The C_H/C_L ratio is also ~ 1000. The opposite rotating directions of the hysteretic curves in Figure 1(b) and 1(d) indicate that the HRS corresponds to the LCS and the LRS corresponds to the HCS. That is, the positive voltage pulse switches the memory stack to the HRS and LCS, while the negative pulse switches it to the LRS and HCS on the contrary.

For characterizing the cell memory performances, the resistance retention and write speed are measured, as shown in Figure 1(e) and (f) respectively. The retention of the HRS and LRS is obviously much longer than 10^5 s, and the width of the bipolar voltage pulses that switch the stack between the HRS and LRS can be shorter than 10 ns under $V_{write} = \pm 9.6$ V, which is real-time monitored and shown in the inset of Figure 1(f). Besides, the endurance over 10^8 switching cycles is also displayed in Figure 1(g), in which the resistance is readout at 0.5 V and the switching is operated by the ± 10 V pulses. Although the HRS has a weak linear dependence on the switching

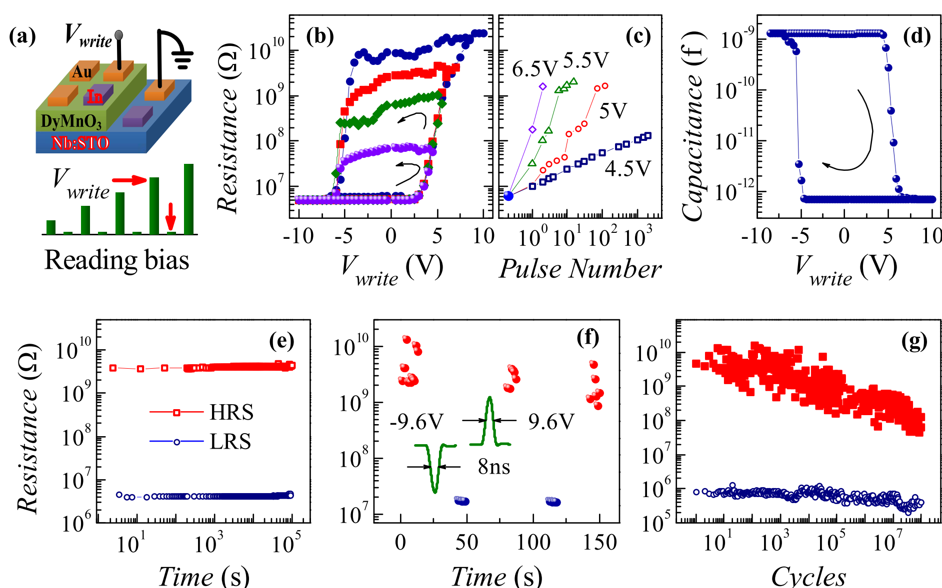

Figure 1 | Resistance and Capacitance switching performances of the Au/DMO/NSTO/Au stack at room temperature. (a) Upper panel: Schematic of the stack and the measurement configuration. Lower panel: Schematic of the measuring method for the resistive hysteresis. (b) V_{write}-dependent resistive hysteresis, with V_{write}: $0 \to -10$ V $\to V_{max} \to 0$ [V_{max} = 4.5, 5.5, 7, and 10 (V) respectively] and readout at 0.1 V. (c) V_{write} pulse number dependent resistive switching from the LRS, with fixed pulse width of 20 μs and V_{write} = 4.5, 5, 5.5, and 6.5 (V) respectively, readout at 0.1 V. (d) V_{write}-dependent capacitive hysteresis between −10 V and 10 V, readout at 50 kHz and 50 mv AC voltage. (e) Retention data of the HRS and the LRS respectively, readout at 0.1 V. (f) Time dependent resistance before and after the stressing of ± 9.6 V pulses with width of ∼ 8 ns, readout at 0.1 V. (g) Endurance data for 10^8 consecutive switching cycles, operated by ± 10 V pulses (100 μs-width, compliance current: 10 mA) and readout at 0.5 V.

cycles in the *log-log* scales, the LRS is stable and the R_H/R_L ratio is still larger than 100 times even over the 10^8 switching cycles. The close correlation of the HRS (LRS) with the LCS (HCS) allows us to infer the similar memory performances for the memcapacitive applications.

The memory switching at Au/NSTO interface. To clarify the core physical ingredient for the memory effect, the *I-V* behaviors of various stack cells including the Au/DMO/NSTO/Au, Au/DMO/NSTO/In, In/NSTO/Au, and In/NSTO/In, are measured under the identical sweep of 0 → 10 V → −10 V → 0 with a current compliance of 10 mA. Figure 2(a) indicates that for the Au/DMO/NSTO/Au and In/NSTO/Au stacks the hysteretic *I-V* behaviors are clearly displayed in the positive voltage region, while for the Au/DMO/NSTO/In and In/NSTO/In stacks no any hysteretic *I-V* characteristics are demonstrated, noting that the *I-V* plot without hysteretic characteristic means no memory effect. In these structures, the contact between Indium and NSTO is Ohmic with a low contact resistance of ~ 6 Ω, as evaluated from the linear *I-V* curve of In/NSTO/In stack. With the same measuring protocol as that in Figure 1(b), the significant V_{write}-dependent resistance hysteresis of the Au/DMO/NSTO/Au and In/NSTO/Au stacks is shown in Figure 2(b), while no variation of resistance in the Au/DMO/NSTO/In and In/NSTO/In stacks is detected (no shown here). By comparing the electrical behaviors of these four stacks, one can easily find that the hysteresis behavior (i.e. memory effect) can be observed only in the stack with the NSTO/Au junction interface, i.e. the nonvolatile memory switching takes place at the NSTO/Au interface instead of others.

Nevertheless, considering that the In/NSTO contact resistance is very low, the *dc* resistance of the Au/DMO/NSTO/Au stack can be recognized as the serial connection of the Au/DMO/NSTO/In stack with the memristive In/NSTO/Au stack. When a voltage (V_{write}) is applied onto this serially connected device, the voltage drop (V_m) on memristive In/NSTO/Au stack can be calculated according to the *I-V* data of the three stacks shown in Figure 2(a). Consequently, the function $V_m(V_{write})$ is obtained. Then, combining with the data of the V_{write}-dependent resistance of the In/NSTO/Au stack [shown in Figure 2(b), readout at 0.5 V and denoted as $R_m(V_{write}, 0.5\ \text{V})$], the V_{write}-dependent resistance of the serially connected device can be calculated by $R(V_{write}, 0.5\ \text{V}) = R_m(V_m(V_{write}), 0.5\ \text{V}) + R_n(0.5\ \text{V})$. Here $R_n(0.5\ \text{V})$ is the resistance of Au/DMO/NSTO/In stack measured at 0.5 V. The red curve in Figure 2(b) is the calculated result, which agrees well with the experimental data of Au/DMO/NSTO/Au stack. This result further confirms that the memristive effect takes place at the NSTO/Au interface, and the Au/DMO/NSTO part plays a role as a nonlinear resistor during the *dc* resistance measuring on Au/DMO/NSTO/Au stack.

Besides, to investigate the origin of capacitance change of the device, we also carry out the V_{write}-dependent C_p measurement on the Au/DMO/NSTO/In and the In/NSTO/Au stacks respectively. It is noted that the resistance of the In/NSTO contact (~6 Ω) in these stacks is much less than that of the Au/DMO/NSTO (R_n ~ 710 kΩ) and NSTO/Au (>5 kΩ) parts, which assures the negligible impact of the In/NSTO junction capacitance on the measured capacitance. As shown in Figure 2(c), an obvious C_p hysteresis is observed both in the In/NSTO/Au and Au/DMO/NSTO/Au stacks but absented from the Au/DMO/NSTO/In stack. Similarly, the C_p hysteresis is only observed in the stacks with the NSTO/Au junction. This result indicates that the memcapacitive switching is also originated from the NSTO/Au junction. The C_p hysteresis curve of the In/NSTO/Au indicates that the capacitance of the NSTO/Au junction is varied between 2.7 pf and 0.7 pf, with a ratio of ~ 3.8. In addition, the simultaneously measured equivalent parallel resistance (R_p) hysteresis of the In/NSTO/Au stack is also demonstrated in Figure 2(c). The reverse rotation of C_p and R_p hysteresis loops indicate that the memcapacitive and memrisitive switching happen at the same time.

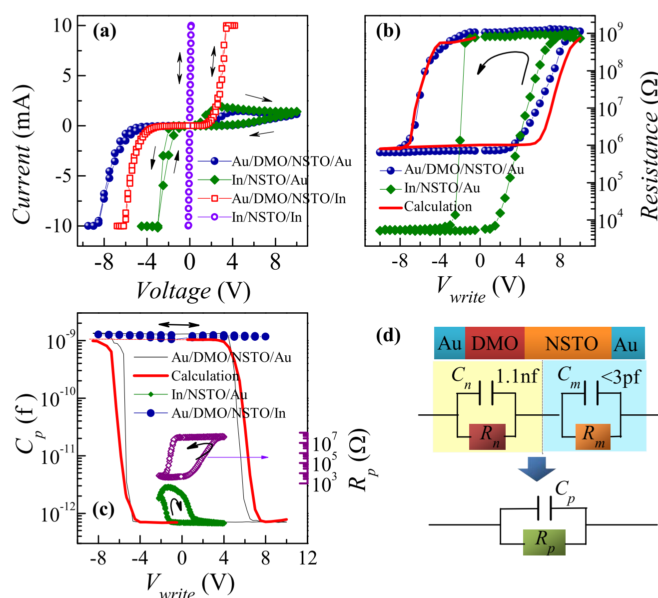

Figure 2 | (a) *I-V* loop curves of the Au/DMO/NSTO/Au, In/NSTO/Au, Au/DMO/NSTO/In, and In/NSTO/In stacks. (b) V_{write}-dependent resistance hysteresis of the In/NSTO/Au and Au/DMO/NSTO/Au stacks, readout at 0.5 V. (c) V_{write}-dependent capacitive hysteresis of the In/NSTO/Au, Au/DMO/NSTO/In, and Au/DMO/NSTO/Au stacks (left axis), and the equivalent parallel resistance hysteresis of the In/NSTO/Au structure (right axis), respectively. The red curves in (b) and (c): calculated resistance and capacitance hysteresis respectively, basing on the serial connection of Au/DMO/NSTO/In with In/NSTO/Au stack. (d) Schematic diagram for equivalent circuit of the Au/DMO/NSTO/Au device.

The impact of the Au/DMO/NSTO part on the memory performance of the device. Figure 2(c) shows that the C_p variation in the Au/DMO/NSTO/Au device is much larger than that in the In/NSTO/Au stack, which is well explained by the large capacitance and the voltage dividing effect of Au/DMO/NSTO part. For the Au/DMO/NSTO/Au device, the HCS capacitance (C_H ~ 1.1 nf) is almost equal to the capacitance of the Au/DMO/NSTO/In stack, while the LCS capacitance (C_L ~ 0.7 pf) is approximately equal to the LCS capacitance of the In/NSTO/Au stack. Besides, the capacitance of the Au/DMO/NSTO/In stack is V_{write}-independent. These facts suggest that the Au/DMO/NSTO part must be regarded as a nonlinear resistor paralleling with a constant capacitance. With these experimental data in Figure 2(b) and (c), the equivalent circuit of the device is determined and shown in Figure 2(d). Based on this equivalent circuit and the calculation method used in Fig. 2(b), we also calculate the V_{write}-dependent C_p of the Au/DMO/NSTO/Au device. The calculated result, shown in Fig. 2(c), agrees with the experimental data quite well, which verifies the correctness of the equivalent circuit.

As the NSTO/Au junction is at the LRS (R_m ~ 5.3 kΩ), the Au/DMO/NSTO part has much larger resistance (R_n ~ 710 kΩ) which burdens most of the voltage drops, so the HCS is mainly contributed by the Au/DMO/NSTO part. As the NSTO/Au junction is at the HRS (R_m ~ 10^9Ω), however, the NSTO/Au junction burdens most of the voltage drops and hence contributes to the LCS of the device. Therefore, the HCS mainly comes from the Au/DMO/NSTO part while the LCS from the NSTO/Au part. The Au/DMO/NSTO part contributes to the large capacitance change in the Au/DMO/NSTO/Au device.

Besides, the Au/DMO/NSTO part also stabilizes the LRS of the Au/DMO/NSTO/Au device. Figure 3(a) and (b) shows the relaxation

characteristics of the LRS for the In/NSTO/Au stack under the positive and negative reading bias respectively. The linear increase of the normalized resistance with time in the *log-log* scales satisfies the power-law of $R \propto t^n$. Here, t is the relaxing time, and n is the index number which scales the relaxation rate. By fitting the data with this power-law, n is found to linearly depend on the $|V_{bias}|^{1/2}$, as shown in Figure 3(c). Moreover, the pulse time dependent resistance switching from the LRS, which can be easily converted from the data in Figure 1(c) with the constant pulse duration, also satisfies the power-law and has the relation of $n \propto V_{write}^{1/2}$, as shown in Figure 3(d). These suggest that an extra small reading bias is expected to effectively enhance the retention of the LRS. Obviously, a serial connection of a large resistor is one of the most effective ways to reduce the voltage-drop on the NSTO/Au junction. Considering that the resistance of the Au/DMO/NSTO part is more than two orders of magnitude larger than that of the NSTO/Au junction as the device is at the LRS, the voltage-drop on the NSTO/Au junction is smaller than 1.0 mV as the 0.1 V is applied to the whole device, ensuring the good retention of the LRS [Figure 1(f)].

It is noted that the serial connection of a constant resistor would enlarge the switching voltage or reduce the R_H/R_L ratio due to the voltage dividing effect. In order to enhance the retention of the LRS and also maintain other switching properties, for example the R_H/R_L ratio and the value of V_{write}, a resistor with high nonlinearity is a good solution. Considering that the nonlinear resistor like the Au/DMO/NSTO stack here has a high resistance at low voltage and low resistance at high voltage, a large V_{write} applying to the device is almost dropped on the NSTO/Au memory junction while the voltage-drop on the Au/DMO/NSTO part is very small.

To compare the performances of the In/NSTO/Au and the Au/DMO/NSTO/Au stacks, consecutive cycling of V_{write} pulses (0 → 10 V → −10 V → 0, with fixed 100 μs-width and current compliance of 10 mA) is carried out, during which the resistances are measured at 0.5 V at the interval of V_{write} pulses. The endurances of the two stacks are shown in Figure 4(a) and 4(b), and the resistance distributions of them are presented in Figure 4(c) and 4(d), respectively. For the In/NSTO/Au stack, the LRS is always stabilized at ~ $10^{3.7}$ Ω, while the HRS is first distributed between 10^8 Ω and 10^9 Ω and then steps to ~ $10^{6.5}$ Ω after ~ 300 cycles. Therefore, the resistance change ratio is stabilized at ~ $10^{6.5}/10^{3.7} = 10^{2.8}$. For the Au/DMO/NSTO/Au stack, however, the step-like change of the HRS does not appear during the endurance test. Although the LRS is raised to ~ 10^6 Ω, the resistance change ratio still remains at ~ $10^9/10^6 = 10^3$, which is a little larger than that in In/NSTO/Au structure. This result indicates that the integration of the Au/DMO/NSTO stack to the NSTO/Au junction does not actually reduce the R_H/R_L ratio after the 'training' of the first 300 cycles.

In addition, the distributions of V_{set} and V_{reset} of the In/NSTO/Au and Au/DMO/NSTO/Au stacks are shown in Figure 4(e) and 4(f) respectively. Here, V_{set} and V_{reset} are the critical V_{write} at which the steepest switching between the HRS and LRS happens. It can be seen that with the serial connection of the Au/DMO/NSTO stack, V_{set} and V_{reset} are still stable even though the distribution widths of them have small enlargement due to the voltage dividing effect. Additionally, it is observable that the shift of V_{reset} is smaller than that of V_{set}. This is because that the *I-V* nonlinearity of the Au/DMO/NSTO stack in the positive voltage region is higher than that in the negative voltage region (the red curve in Figure 2(a)). This result implies that replacing the Au/DMO/NSTO stacks with other more highly nonlinear stacks can further reduce the enlargement of the switching voltage.

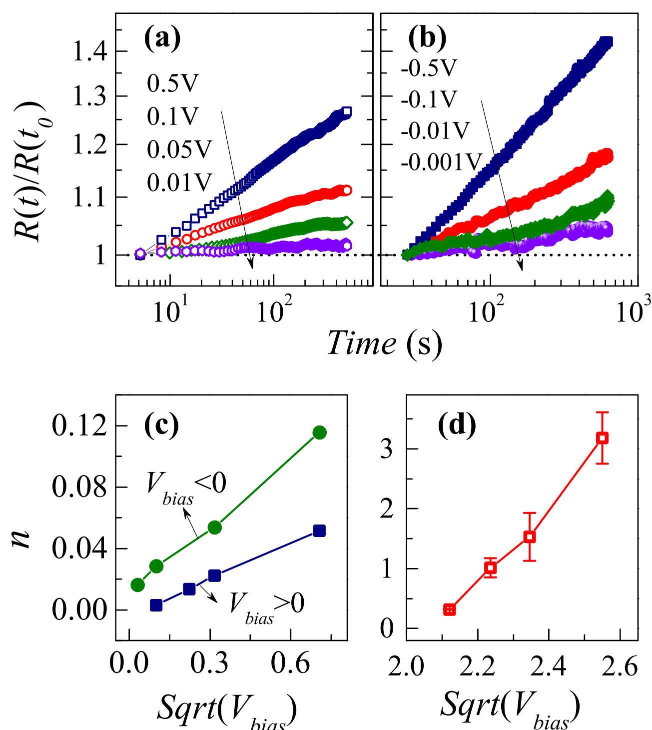

Figure 3 | Normalized resistance relaxing characteristics of LRS, with (a) the reading bias of 0.5, 0.1, 0.05, 0.01 (V), and (b) the reading bias of −0.5, −0.1, −0.01, −0.001(V), respectively. (c) Sqrt(V_{bias}) dependent n, obtained by fitting the relaxation data in (a) and (b) with the law of $R \propto t^n$. (d) Sqrt(V_{write}) dependent n, obtained by fitting the data in Figure 1(c) with the law of $R \propto N^n$ (N is the pulse number).

Memory switching mechanism. To gain insight into the mechanisms responsible for the memory effect in the NSTO/Au junction, we investigate the *I-V* behaviors of the HRS and LRS of the NSTO/Au junction using the 3-probes measurement configuration on the In/NSTO/Au stack, as shown in the inset of Figure 5(a). During the measurement, an Au-pad is grounded and the device is first switched to the target state (HRS or LRS) by voltage pulse through an In-pad. Then the source voltages (V_{sour}) with the sequence of 0 → 0.5 V → −0.5 V → 0 are applied to this In-pad, accompanied with the synchronous current measurement at different V_{sour}. Simultaneously, the actual voltage-drops (V_{mea}) on the NSTO/Au junction are also measured synchronously through another In-pad during the V_{sour} sweeping. Figure 5(a) indicates that there is a rectifying I-V_{mea} behavior at the HRS at low voltage region. The linear $\ln(-I) \sim (-V_{mea})^{1/2}$ dependence in the negative voltage region, as shown in the inset, supports the Schottky emission mechanism[5]. As the junction is at the LRS, however, a linear I-V_{mea} behavior is observed, favoring the Ohmic behavior rather than the Schottky emission.

It is proposed that the formation of conductive filaments in the Schottky junction or the electrons tunneling through the thin Schottky barrier would bring out a LRS with linear *I-V* behavior[1,8,15]. To clarify the dominated switching mechanism, we fabricate the Au/DMO/NSTO/Au(bottom electrodes) structure, in which several Au pad bottom electrodes with different areas are deposited. Then the device is switched to the LRS by −10 V voltage pulse or to the HRS by + 10 V voltage pulse imposed through these Au bottom electrodes respectively. After these switches, we measure the bottom electrode-area dependent resistances of the LRS or the HRS at a low voltage of 0.1 V. During the measurement, the Au bottom electrode is grounded and the top Au electrode with fixed pad area is connected to the voltage source [illustrated in Fig. 1(a)]. Figure 5(b) shows that the resistances of both the HRS and LRS become smaller for larger Au bottom electrode area. Good scaling behavior of the resistance is shown, suggesting that the filament-type switching mechanism can't be the dominant one for the present device. Besides, the clear switching of capacitance in the NSTO/Au junction also suggests that the

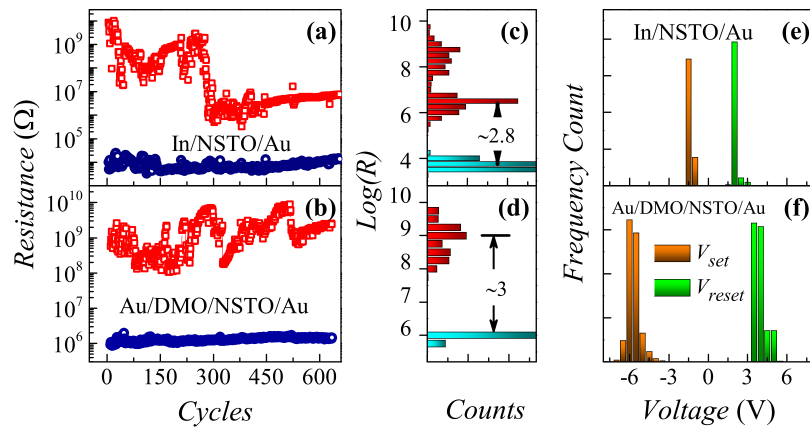

Figure 4 | (a) and (b) The endurances, (c) and (d) the distributions of $Log(R_H)$ and $Log(R_L)$, and (e) and (f) the distributions of V_{set} and V_{reset}, of the In/NSTO/Au stack (upper panel) and the Au/DMO/NSTO/Au stack (lower panel), respectively. The data is obtained by continuously repeating the same measurement as that in Figure 2(b) with V_{max} = 10 V. R_H and R_L are the upper and lower boundary values of each resistance hysteresis curves respectively. V_{set} and V_{reset} are the critical V_{write} at which the steepest switching between HRS and LRS happens.

formation of conductive filaments is not the major mechanism, since the junction capacitance depends on the mean Schottky barrier width but insensitive to the formation/rupture of local conductive filaments[8,15].

Hence, the memory switching in the present device is dominated by the field-induced uniform modulation of the Schottky barrier profile rather than the formation of filaments. The decrease of the barrier height/width leads to the decrease of resistance and the increase of capacitance of the junction[1,2,9,22], i.e. the switching from the LCS (HRS) to the HCS (LRS), and vice versa. Since the variation of the Schottky barrier profile is continuous and remnant rather than abrupt[18], the appearance of many metastable states demonstrated in Figure 1(b), (c) and (d) is well understood.

There are two ways to electrically modulate the barrier profile of a metal/NSTO junction. One is the movement of defects and/or oxygen vacancies toward/away the junction interface under the reversely polarized bias stressing[29,30]. However, Jiang *et al.* proposed that the uniform motion of defects or oxygen vacancies is too slow to produce the nanosecond switches[31]. The other one is the carrier trapping/detrapping at defect sites near the junction interface[13,22,26,27]. Upon a forward pulse to the NSTO/Au junction (negative voltage applies to the NSTO side and the Au electrode is grounded), the barrier height is lowered and some detrapped electrons are possibly flowing through it toward the Au electrode, leaving to the positively charged empty traps nearby the interface[9,22]. As illustrated in Figure 5(c), such positively charged traps provide an additional potential, which reduces the build-in potential and the depletion width for maintaining the Fermi energy balance between NSTO and Au[1], thus leading to the LRS. On the contrary, as a reverse pulse is applied to the LRS, the barrier is raised and electrons are hindered to flow through it but are possibly injected into the empty traps, causing the traps to be neutral and then resuming the depletion width, i.e. the resume of the HRS. The relaxation of the LRS [Figure 3(a) and 3(b)] and the pulse number dependent switching from the LRS to the HRS [Figure 1(c)], which follows to the power-law, are consistent with the charge trapping/detrapping mechanism[23,24,28].

In order to verify the dominated switching mechanism, we fabricate different Au/NSTO junctions by depositing Au to the same NSTO substrate under different Ar atmosphere pressures and different depositing currents. The change in the depositing conditions alters the space defect density near the junction interface. However, the oxygen vacancy density near the interface is scarcely altered due to the usage of the same substrate and the deposition under an atmosphere without oxygen gas and with small depositing current. Figure 5(d) shows the V_{write}-dependent resistance hysteresis of the Au/NSTO junction deposited under the Ar atmosphere pressure of 15 Pa, 20 Pa, and 30 Pa respectively. By decreasing the deposition pressure from 30 Pa to 20 Pa with a depositing current of 4 mA, the hysteresis curve is shrunk, i.e. the LRS is increased and the HRS is decreased. As the depositing pressure is further reduced to 15 Pa and a depositing current of 2 mA is used, the hysteresis curve almost disappears and the junction retains at the LRS. These results suggest

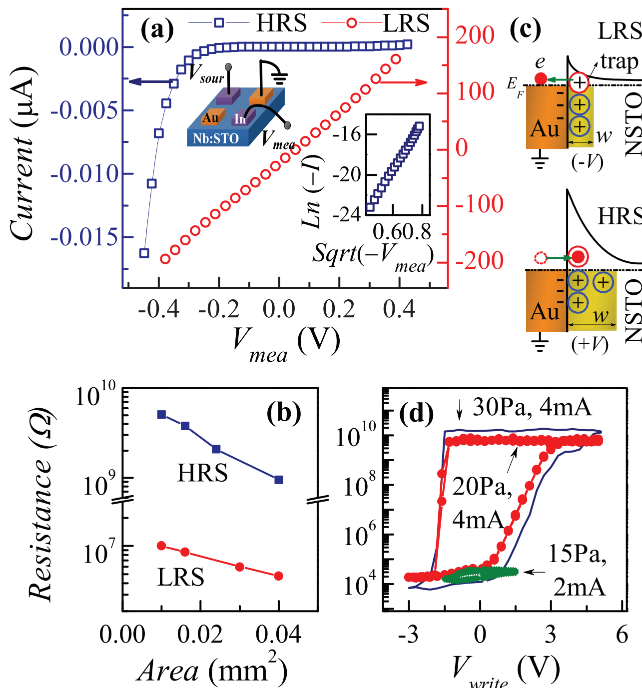

Figure 5 | (a) I-V_{mea} behaviors of the HRS and the LRS of the Au/NSTO junction, measured by using 3-probes configuration on the In/NSTO/Au stack. Inset: $Sqrt(-V_{mea})$ dependent $ln(-I)$ plot of the HRS. (b) The grounded Au pad area dependent resistances of the HRS and the LRS of the Au/DMO/NSTO/Au device respectively, with the configuration shown in Figure 1(a). (c) Schematic diagrams for the detrapping and trapping electrons in the NSTO/Au junction. The electron trapping(detrapping) causes to the broadening(narrowing) of barrier and consequently forms to the HRS(LRS) respectively. (e) V_{write}-dependent resistance hysteresis of In/NSTO/Au, with Au deposited under the Ar pressure of 15 Pa, 20 Pa, and 30 Pa, and the depositing current of 4 mA and 2 mA, respectively.

that the space defects other than oxygen vacancies seriously affect the junction transport behavior, and imply that the space defects related charge trapping/detrapping near the interface dominate the memory switching behavior.

It is noted that the charge trapping/detrapping is field-controlled and the related memory switching should be reversible. However, the step-like variation in the endurance data of the In/NSTO/Au stack is observed in Figure 4(a). This suggests that except for the charge trapping/detrapping at the defect sites, the other incompletely reversible factor like as the movement of defects and/or oxygen vacancies also affects the memory switching. With decreasing voltage stress on the switching interface, the incompletely reversible movement of oxygen vacancies should be reduced, which may be the reason why the Au/DMO/NSTO nonlinear element essentially enhances reliabilities of memory.

Discussion

The Au/DMO/NSTO/Au stack is not only a high performance memristor but also a memcapacitor. In this stack, the switching time is below 10 ns, the retention is much longer than 10^5 s,and the ratios of R_H/R_L and C_H/C_L are larger than 100 over the 10^8 switching cycles. These memory effects come from the NSTO/Au junction where the junction barrier profile is electrically modulated. The serial connection of Au/DMO/NSTO stack, which behaves as a nonlinear resistor paralleling with a capacitance, is demonstrated to be a good solution to amplify the change ratio of capacitance and improve the memory switching stability of NSTO/Au junction.

Methods

Sample fabrication. The polycrystalline $DyMnO_3$ (DMO) ceramic target with 2 cm in diameter was synthesized by the solid-state reaction method from Dy_2O_3, and MnO_2 with 99.99% purity. Then this target was used to deposit DMO films on 0.7 wt% Nb-doped $SrTiO_3$ <111> (NSTO) single-crystal substrates by pulsed laser deposition using a KrF excimer laser with wavelength of 248 nm. The laser energy density, laser repetition rate, oxygen ambient pressure, and growth temperature are 2 J cm^{-2}, 2 Hz, 15 Pa, and 750°C, respectively. The Au electrodes with 100 μm in diameter were deposited by ion sputtering with a shadow mask under air pressure of 20 Pa, or under argon pressure of 30 Pa, 20 Pa, or 15 Pa. The Indium electrode was carefully pressed to the rough surface of NSTO by hand for obtaining the Ohmic contact.

Measurement method. The crystallization of DMO films is confirmed by X-ray diffraction (XRD) technologies, and the morphology and thickness of the films were investigated by scanning electron microscopy (SEM). The *I-V* characteristics, resistance relaxation, and the retention and endurance performances were measured by two-probe method using a Keithley 2636A source meter unit at room temperature with homemade software. Three-probe method was used to measure the *I-V* behavior of the NSTO/Au junction. During the measurement of the V_{write}-dependent resistance hysteresis, the resistances were measured by a bias of 0.1 V (Figure 1(b))) or 0.5 V (Figure 2(b)) after 1 s delay from the application of different V_{write} pulses (pulse-width is fixed to 100 μs, and the current compliance is set to 10 mA), schematically shown in the lower panel of Figure 1(a). For measuring the V_{write}-dependent capacitive hysteresis, the same measuring protocol was used but the C_p and R_p was measured by an *Ac* voltage with 50 mV in amplitude and 50 kHz in frequency by using Agilent 4294A. During the switching speed measurement, the Agilent 33250B and the Agilent Infiniium 54830 oscilloscope were respectively used to generate and real-time monitor the burst pulse (full width at half maximum: ~ 8 ns), and the Keithley 2636A was used to read the resistance before and after the burs pulse. By using *NI Multisim 12.0 software*, the simulations based on the equivalent circuit in Figure 2(d) and the data in Figure 2(b) and (c) are carried out. The results (see supplementary Fig. S online) indicate that, due to the large capacitive charging in the Au/DMO/NSTO part, the NSTO/Au junction burdens most of the voltage drops during the burst pulse whether the device is at the HRS or the LRS.

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Author contributions

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Additional information

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