Video Article

Silicon Metal-oxide-semiconductor Quantum Dots for Single-electron Pumping

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Abstract

As mass-produced silicon transistors have reached the nano-scale, their behavior and performances are increasingly affected, and often deteriorated, by quantum mechanical effects such as tunneling through single dopants, scattering via interface defects, and discrete trap charge states. However, progress in silicon technology has shown that these phenomena can be harnessed and exploited for a new class of quantum-based electronics. Among others, multi-layer-gated silicon metal-oxide-semiconductor (MOS) technology can be used to control single charge or spin confined in electrostatically-defined quantum dots (QD). These QD-based devices are an excellent platform for quantum computing applications and, recently, it has been demonstrated that they can also be used as single-electron pumps, which are accurate sources of quantized current for metrological purposes. Here, we discuss in detail the fabrication protocol for silicon MOS QDs which is relevant to both quantum computing and quantum metrology applications. Moreover, we describe characterization methods to test the integrity of the devices after fabrication. Finally, we give a brief description of the measurement set-up used for charge pumping experiments and show representative results of electric current quantization.

Video Link

The video component of this article can be found at http://www.jove.com/video/52852/

Introduction

Silicon is the material of choice for most of the modern microelectronics. Its properties, combined with advanced lithographic techniques, have allowed the semiconductor industry to achieve very large-scale integration and deliver billions of transistors per chip. The metal-oxide-semiconductor (MOS) technology[1] has been the key of this relentless technological progress[2]. In brief, it is based on a selectively doped Si substrate which is thermally oxidized to grow a high quality SiO_2 gate oxide on which a metal gate electrode is deposited. Recently, it has been shown that the use of a stack of gate oxides could be beneficial[3] . While present industry standards have reached minimum feature sizes for gate lengths below 20 nm, it is becoming increasingly evident that, at this level of miniaturization, detrimental quantum mechanical phenomena come into play that may complicate further downscaling[4].

Remarkably, silicon is also an excellent host material to exploit the quantum properties of the electron charge and spin[5]. This has broadened its range of applicability to entirely new fields such as quantum computing[6] and quantum electrical metrology[7]. Among other approaches[5], the use of a multi-gate MOS technology[8,9] has led to electrostatically-defined quantum dots (QD) whose occupancy can be controlled down to single-electron level[10]. Unlike the conventional MOS process where just one gate per transistor is needed[1], these QDs are defined via a three-layer stack of Al/Al_yO_x gates which are used to selectively accumulate electrons at the Si/SiO_2 interface, as well as provide lateral and vertical confinement[11].

Although these devices had been originally developed for quantum computing applications, they have also recently shown promising performances as metrological tools[12,13]. In the field of quantum electrical metrology, a long-standing goal is the redefinition of the unit ampere in terms of the elementary charge (e) [14]. In particular, the emphasis is on the realization of nano-scale charge pumps to clock the transfer of individual electrons timely and accurately. These devices generate macroscopic quantized electric currents, $I=nef$, where f is the frequency of an external driving oscillator and n is an integer. To date, the best performance has been achieved with a GaAs-based pump by yielding a current in excess of 150 pA with a relative uncertainty of 1.2 parts per million[15]. Recently, silicon MOS QDs have also stood out for the implementation of highly accurate single-electron pumps thanks to the capability of finely tuning the charge confinement[13].

Here, we discuss the protocol used for the fabrication of silicon MOS QDs. Furthermore, the cryogenic set-up used to test the integrity of the devices after fabrication and the one to perform charge pumping experiments are described. Finally, representative measurements of quantized electric current are reported.

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Protocol

Note: This protocol describes the procedures used to fabricate, package and test single-electron pumps based on silicon MOS QD technology. The steps discussed in sub-sections 1 and 2 are carried out in an ISO5 cleanroom, while those of section 3 are performed in ISO6 laboratories. Ambient conditions are continuously controlled. Nominal values for temperature and humidity are set at 20 ± 1 °C and 55% ± 5%, respectively.

1. Microfabrication

1. Field Oxide
    1. Clean the wafer by immersion in the following: piranha etch (10 min), deionized (DI) water (10 min), RCA-2 solution (DI water 175 ml, HCl 30 ml, H_2O_2 30 ml at 100 °C for 10 min), deionized water (5 min), hydrofluoric (HF) acid diluted in water 10:1 (10 sec), DI water (10 min). Use protective garments when handling HF (*i.e.*, goggles, PVC apron, and PVC gloves). Proceed in the stated order.
    2. Place the wafer in oxidation furnace at 900 °C and oxidize in steps as follows: dry O_2 (10 min), wet O_2 (40 min), dry O_2 (10 min), N_2 (15 min).

2. Ohmic Contacts
    1. Carry out photolithography and etch oxide.
        1. Deposit a few-nm-thick layer of adhesion promoter hexamethyldisilazane (HMDS) onto the wafer surface as follows: pre-bake on a hotplate at 110 °C for 1 min, pour ~50 ml of HMDS in a glass beaker, place the beaker and the wafer in the vacuum chamber, evacuate and wait for 2 min.
        2. Spin a 2–4-µm-thick layer of photoresist on both back and front sides of the wafer (3,000–5,000 rpm, 25–40 sec depending on desired thickness).
        3. Expose to ultra-violet light in mask aligner (10 mW/cm^2 for 4–10 sec according to resist thickness). Post-bake on a hotplate at 110 °C for 1 min.
        4. Develop for 1–2 min, then rinse in deionized water.
        5. Perform O_2 plasma etch for 20 min (pressure = 340 mTorr; incident power = 50 W; reflected power < 1 W).
        6. Etch oxide in buffered HF acid solution (15:1, 4–5 min, etch rate ≈ 20 nm/min at 30 °C). Rinse in deionized water (5 min). Blow dry with N_2.
    2. Remove photoresist by immersion in acetone. Rinse in isopropanol (IPA), then blow dry with N_2.
    3. Place wafer in furnace at 1,000 °C with phosphorus source (N_2 flow for 30–45 min depending on desired doping density).
    4. Remove contaminated oxide layer with HF acid diluted in water (10:1, 3–4 min, etch rate ≈ 40 nm/min at 30 °C), rinse in deionized water (10 min).
    5. Oxidize as in 1.1.2.

3. Gate Oxide
    1. Repeat steps 1.2.1 and 1.2.2.
    2. Place wafer in dedicated furnace at 800 °C and oxidize in steps as follows: dry O_2 (10 min), dichloroethylene+O_2 (20 min), dry O_2 (10–30 min depending on desired oxide thickness), N_2 (15 min).

4. Ohmic Contacts Metallization
    1. Repeat step 1.2.1.
    2. Place wafer in electron-beam evaporator. Evaporate 100 nm of aluminum at 0.2–0.5 nm/sec and 5 x 10^{-6} Torr.
    3. Soak the wafer in *N*-methyl-2-pyrrolidone (NMP) on hotplate at 80 °C for 1 hr to lift off the metal. Use ultrasonic agitation if needed. Rinse in IPA for 2 min. Blow dry with N_2.
    4. Anneal in forming gas at 400 °C for at least 15 min.

2. Nanofabrication

1. Wafer Dicing
    1. Spin any resist onto the wafer to act as protective coating (type of polymer and spinning parameters are irrelevant at this stage).
    2. Use diamond tip dicer to cut the wafer into individual chips of ~10 x 2 mm^2.

2. Cleaning
    1. Soak in NMP for 1 hr on hotplate at 80 °C, then rinse in IPA for 2 min. Blow dry with N_2.
    2. Perform O_2 plasma etch for 5 min (incident power = 50 W; reflected power < 1 W).
    3. Spin clean with acetone and IPA (7,500 rpm, 30 sec)

3. Alignment markers patterning
    1. Spin polymethyl methacrylate (PMMA 950k) A4 resist (5,000–7,500 rpm, 30 sec depending on desired thickness). Typical working thickness ≈ 150–200 nm. Bake the resist on a hotplate at 180 °C for 90 sec.
    2. Carry out e-beam lithography. Use the following write conditions: beam energy = 30 keV, beam current ≈ 30 pA, area dose ≈ 500–650 µC/cm^2 depending on markers size and resist thickness.
    3. Develop the resist in a solution of methyl isobutyl ketone and IPA (1:3) for 40–60 sec, then rinse in IPA for 20 sec. Blow dry with N_2 gun.
    4. Place the chip in electron-beam evaporator. Evaporate 15 nm of Ti and 65 nm of Pt at 0.2–0.4 nm/sec and 5 x 10^{-6} Torr.
    5. Lift off the metal as in step 1.4.3.

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6. Clean chip as in steps 2.2.2–2.2.3.

4. Gate patterning
    1. Spin resist as in 2.3.1.
    2. Carry out e-beam lithography. Use the following write conditions for high resolution features: beam energy = 30 keV, beam current ≈ 30 pA, area dose ≈ 500–700 $\mu C/cm^2$. Write conditions for low resolution features: beam energy = 15 keV, beam current ≈ 10 nA, area dose ≈ 400–600 $\mu C/cm^2$.
    3. Develop the resist as in 2.3.3.
    4. Place the chip in thermal evaporator. Evaporate Al at 0.1–0.4 nm/sec and 1–9 x 10^{-6} mbar. Target thickness varies according to layer number, as shown in **Figure 2B** (25–35 nm for Layer 1, 45–65 nm for Layer 2, 75–90 nm for Layer 3).
    5. Lift off the metal as in step 1.4.3.
    6. Perform Al oxidation on a hotplate at 150 °C for 5–10 min.
    7. Clean chip as in step 2.2.3.
    8. Repeat steps 2.4.1–2.4.7 twice to realize the 3-layer gate stack.

3. Device Packaging

1. Dice chip as in step 2.1
2. Rinse the resulting smaller chips in acetone and IPA for 2 min.
3. Glue an individual piece to a printed circuit board (PCB) with PMMA A5. Wait 2 min for it to dry. Alternatively, to enhance thermalization, use silver epoxy.
4. Load the PCB onto a wedge bonder and proceed with wiring.

4. Device Integrity Tests

1. Mount the PCB containing the wired device onto a dip probe.
2. Wire the electrical lines of the PCB to those of the dip probe.
3. Insert the probe into a vessel containing liquid helium. Proceed slowly to avoid excessive helium boil-off.
4. For each device gate, connect the corresponding room-temperature electrode of the probe to a source-measure unit, while keeping the other gates grounded. Set the compliance current to few nA. Sweep the voltage from zero to 1.5V in steps of 0.1 V, measure and record the current.
5. Connect each gate line to a battery-powered variable dc voltage source, the source line to the built-in ac voltage source of a lock-in amplifier, and the drain line to the input port of the lock-in amplifier.
6. Measure the source to drain conductance for different gate voltage configurations (see **Figure 4**).
    1. Globally ramp up the voltages applied to gates BL, BR, PL, SL and DL, by keeping C1 and C2 gates grounded. Record the 'turn-on' device characteristics.
    2. Individually ramp down each gate voltage and record the gates 'pinch-off' characteristics.
    3. Adjust the gate voltages to electrostatically define a quantum dot by setting the voltages on BL and BR (PL, SL and DL) smaller (greater) than the turn-on voltages. Record the Coulomb blockade characteristics.

Representative Results

Device Fabrication

The initial microfabrication process (sub-section 1 of the Protocol) is performed on a commercial 4-inch high-purity silicon wafer (n-type doping concentration ≈ 10^{12} cm^{-3}; resistivity > 10 kΩcm; thickness = 310–340 µm). The aim is to realize the substrate on which the gate electrodes will be deposited. This substrate is made of an intrinsic region capped with field oxide (step 1.1), an n+ region capped with field oxide (step 1.2), an intrinsic region capped with high-quality gate oxide (step 1.3), and a metallized n+ region for ohmic contacts (step 1.4). **Figures 1A-D** illustrate the main steps of the microfabrication process. **Figure 1E** shows a microscopic image of a substrate field after microfabrication. The minimum feature size for the lithography at this stage is approximately 4 µm.

The SiO_2 oxide layer grown in step 1.1 has a nominal thickness of 100 nm and is used as a passivation layer. The n-type regions that act as ohmic conductors are obtained via phosphorus diffusion. The target doping density is approximately 10^{19} – 10^{20} cm^{-3}. The high-quality SiO_2 which is selectively grown to be used as gate dielectric has a nominal thickness of 5 nm. The target interface defect density is <10^{10} $eV^{-1}cm^{-2}$ at mid-gap. A dedicated and purposely built triple wall furnace is used for this process. This system is designed to minimize contamination from heavy metal ions and mobile alkali ions, as well as prevent moisture from diffusing into the oxidation chamber. In order to form the electrical contacts, aluminum pads are deposited via electron-beam evaporation on part of the n-type regions.

The nanofabrication process (see sub-section 2) is performed on chip substrates obtained by dicing the wafer processed in step 1. The aim is to realize the nano-scale gate electrodes used to electrostatically define the MOS QDs. Each nanofabrication run typically produces 10–15 complete device samples. Scanning electron micrograph (SEM) imaging of 1–2 devices per batch is usually carried out to confirm that the EBL lithography stages have been successful. Since SEM imaging may inject charges in the substrate or in the metallic gates and cause leakages, only a small number of devices is checked in this way, while the rest is electrically tested. Minimum feature size for the lithography at this stage is approximately 35 nm. To achieve good uniformity of the deposited Al films, the metal is evaporated at rates as slow as few angstrom/second, while the substrate is mounted on a rotating stage. This is kept at RT, and the Al grain size is estimated to be of approximately 20 nm. **Figure 2A** illustrates the main steps of the nanofabrication process. **Figure 2B** shows a SEM image with which the correct definition of the gate electrodes is verified. In general, one aims at realizing those gates which directly define the QD (BL, BR and PL) with the smallest possible feature size. By

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contrast, those gates used to define the electron reservoirs (DL and SL) can have larger dimensions to avoid the unintentional discretization of energy levels in the leads. The nano-scale Ti/Pt markers realized in step 2.3 are used as reference for consistent alignment of the three layers of gates. Platinum is chosen for its excellent contrast with respect to the SiO_2 surface in the e-beam. Titanium is used to enhance adhesion.

At all stages of the fabrication process, carbon-fiber-tip tweezers are used to handle the chips, in order to reduce the likelihood of destructive electrostatic discharge (ESD).

Finally, in order to perform electrical measurements on individual devices, each chip needs to be cleaved in smaller pieces of about 2 x 2 mm^2 (sub-section 3). Each piece is then glued to a custom-made PCB (Rogers R03010 low-loss dielectric) whose pins are connected to the device electrodes through Al wires. Wire bonding is carried out with a wedge bonder machine without heating the chips. The choice of the appropriate bonding parameters is based on two considerations. On the one hand, the wire bond needs to perforate the thermal Al_yO_x layer and make good metal-to-metal contact with the gate pad. On the other hand, an excessive mechanical stress may result in a punch-trough event which damages the field oxide underneath the gate and cause substrate leakages. During the wiring process, the use of an antistatic bracelet is advisable to prevent ESD. In **Figure 3**, a chip with 6 individual devices is glued onto the PCB.

Device integrity tests

Before loading a device into a mK temperature measurement platform such as a dilution refrigerator, preliminary electrical tests are performed at 4.2 K to check the integrity of the sample (see sub-section 4 of the Protocol). To this end, the PCB is inserted into an oxygen-free copper enclosure and is mounted onto a dip probe, which is eventually immersed in liquid He.

The initial test is typically a leakage test that is performed sequentially on each gate. A source-measure unit is connected to an individual gate electrode while the others are grounded. The voltage is ramped up to 1.5 V and the current is measured at the source. Within this voltage range, a properly working gate is not supposed to conduct, because the SiO_2 layer insulates the metal from the silicon substrate and Al_yO_x insulates overlapping gates. Typically, oxide breakdown is known to occur for voltages larger than ~4 V, depending on device geometry and oxide thickness. Therefore, if current is detected during the test, it is likely that at least one of the oxide layers is damaged and the device has to be discarded. Usually, less than 10% of the gates show leakages. The yield is known to be affected by the planar extension of the gate electrodes. In particular, the larger the overlap of the gates with the gate oxide region the more likely it will be to have gate-to-substrate leakages. Similarly, the larger the overlap between gates from different layers the more likely the occurrence of gate-to-gate leakages will be. The quoted yield is relevant for gates that occupy an area of about 50 μm^2 on the thin oxide and with interlayer overlaps of approximately 0.5 μm^2.

Once the device has passed the initial leakage test, the source and drain contacts are connected to a lock-in amplifier and the gates to a modular controllable-voltage battery rack. In this configuration, the device is turned on by globally ramping up all the gate voltages simultaneously. Next, each gate voltage is separately ramped down while keeping the others at high voltages to verify the ability of individual gates to pinch off the current. **Figure 4A** shows representative traces of these measurements. The absence of either a source-drain conduction pathway or individual gate pinch-off is often an indication of some type of gate damage such as gate explosion or metal discontinuity.

Finally, the source-drain current is measured as a function of source-drain bias and plunger gate voltage to observe the signature of Coulomb blockade[16] (see **Figure 4B**).

Measurements

Once a suitable device has been found, it is removed from the liquid He vessel, and dried with a hot-air gun to avoid formation of moisture which may cause ESD. Finally, it is transferred to a dilution refrigerator.

The experiments are performed in a self-made plastic dilution refrigerator with a base temperature of about 100 mK. The cryostat is in a vacuum chamber immersed in a 4.2 K helium bath. The electrical lines are thermalized at the 1 K pot which is also employed to condense the incoming 3He vapor. In the mixing chamber, the endothermic transfer of 3He atoms from the 3He-rich phase into the 3He-dilute phase allows the system to reach a base temperature of about 100 mK.

As shown in **Figure 5**, the fridge is equipped with 20 dc lines and 3 rf lines used to connect the room-temperature electronics to the device at low temperature. Five of the dc lines are Thermocoax cables and 15 are twisted pair loom wires. These lines connect the gate electrodes of the sample to battery-powered dc voltage sources. Voltage dividers at RT are used to reduce electrical noise on individual gates. The RF lines are semirigid coaxial cables that are attenuated by 10 dB at 4 K to reduce thermal noise and dc blocked at RT. These lines are connected to the coplanar waveguides of the bias tees on the PCB.

A low-noise transimpedance amplifier and a digital multimeter are used to measure the current generated by the pump. The electronics is connected to the device via battery-powered optoisolators to prevent the formation of ground loops. The RF drive signals are produced by an arbitrary waveform generator whose grounding is isolated from the one of the cryostat via a dc block component (see **Figure 5**).

The PCB contains 16 pure dc lines and 4 bias tee lines used to combine dc and ac voltages at low temperature. As shown in **Figure 3B**, RC discrete components are used to realize the tee connection (R = 100 kΩ, C = 10 nF), and 50 Ω-matched integrated coplanar waveguides are used for the propagation of high-frequency signals.

Once the device is at mK temperature, the gate voltages are adjusted so that single-electron occupancy in the QD is attained. In particular, tunnel barriers are formed under gates BL and BR, and an electron accumulation layer is induced under gates PL, SL and DL. To this end, the barrier gate voltages are set below their turn-on values, while the accumulation gates are polarized at a greater-than-turn-on voltage. In this way a QD is formed under gate PL and its planar extension is controlled via gates C1 and C2 whose voltages are kept below their turn-on values to induce electrostatic confinement. Next, the rf signals are turned on to periodically modulate the transparency of the tunnel barrier(s), and the electrochemical potential of the dot. Single-electron pumping is achieved with either one or two sinusoidal driving voltages. In the case of one-signal drive, the driving signal is applied to gate BL to modulate the potential of the tunnel barrier at the left-hand-side of the QD. In the case of the two-signal drive, the ac excitations are applied to gates BL and PL to modulate the potentials of both the left barrier and the QD at the

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same frequency but with different phases and amplitudes. These additional degrees of freedom allow one to control the direction of the electron transfer[13]. An iterative process is typically needed to tune the main experimental parameters (*i.e.*, rf drive signal amplitudes/phases and dc gate voltages) and achieve optimal current quantization. Note that neither of the two pumping protocols needs a drain-source bias to perform charge transfers. Hence, the source and drain electrodes are grounded during the pump operation. **Figure 6** shows the characteristic current plateaux at integer multiples of *ef* obtained by applying a two-signal sinusoidal drive to the input barrier (BL) and the plunger (PL) gate. These data are taken at a relatively low driving frequency (10 MHz) for which the tuning of the parameters can be carried out fast. In practice, it is desirable to operate the pump at several hundreds of MHz, typically requiring a much finer parameter optimization[13].

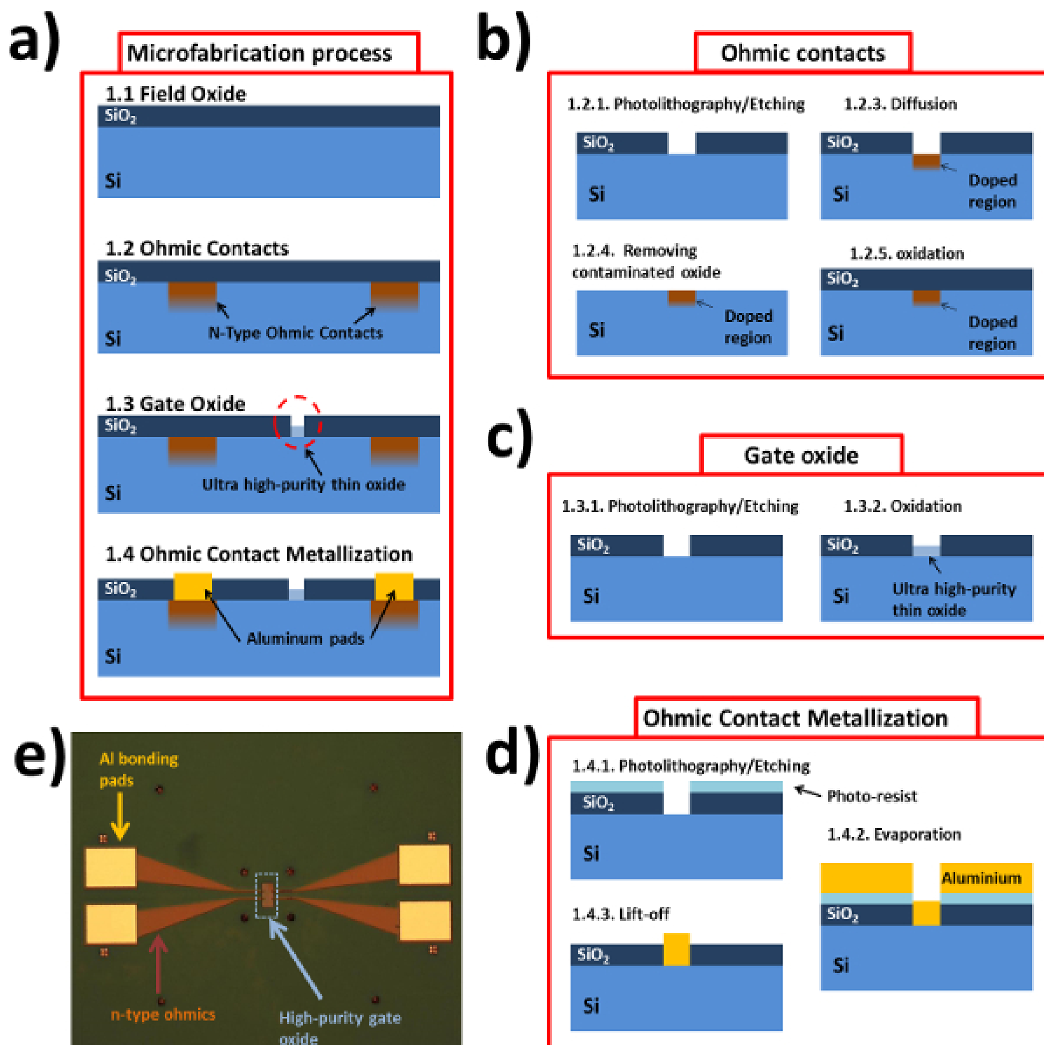

Figure 1. Microfabrication. (**A**) Schematic illustration of main steps in microfabrication. Cartoons are not drawn to scale. (**B**) Realization of a doped region for ohmic contacts. (**C**) Realization of gate oxide. (**D**) Metallization of ohmic contacts. (**E**) Microscopic image of an individual field on a chip after the microfabrication process is completed. Field size is 1.2 x 1.2 mm^2. Please click here to view a larger version of this figure.

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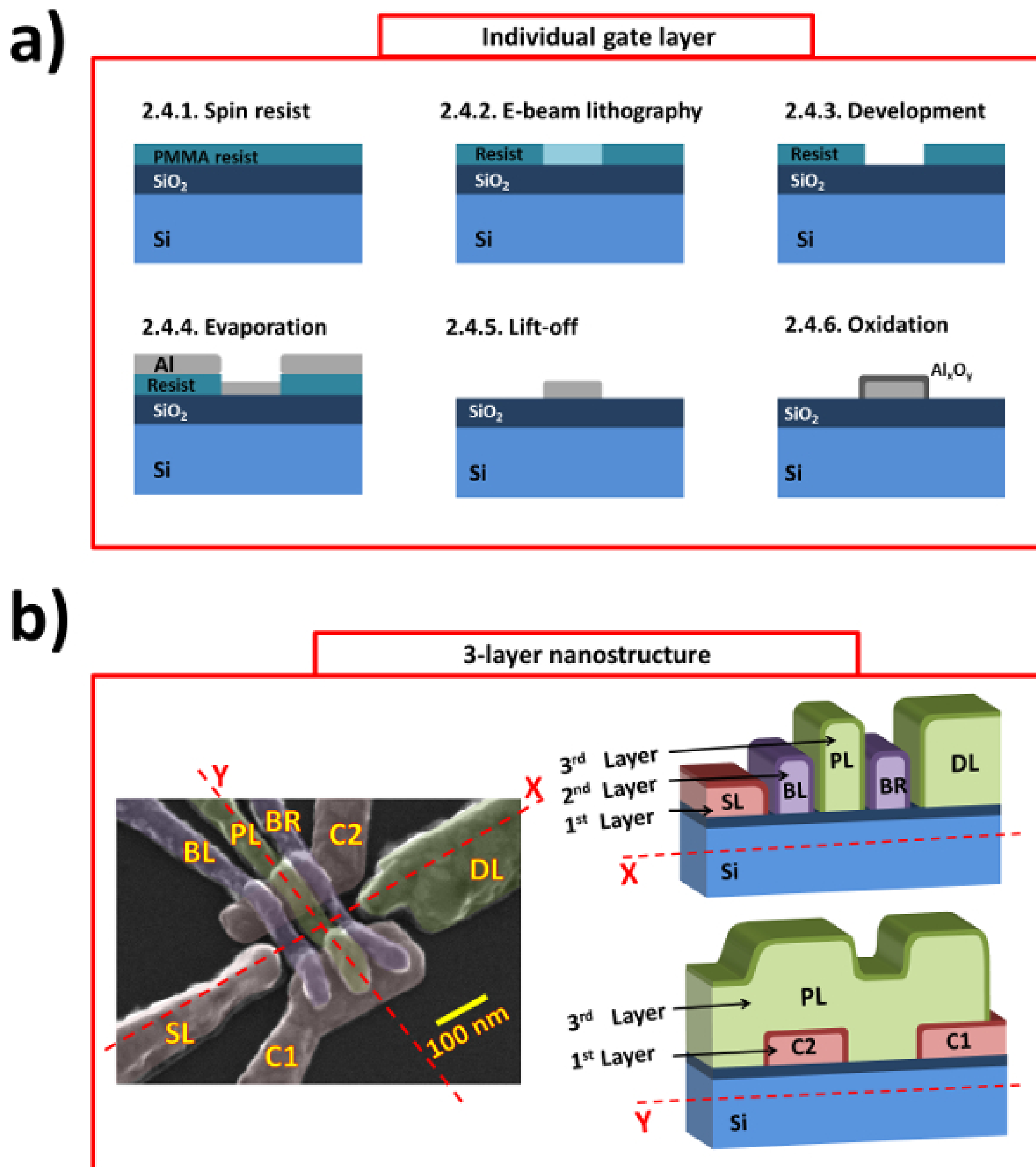

Figure 2. Nanofabrication. (**A**) Fabrication process for individual gate layers. Cartoons are not drawn to scale. (**B**) The 3-layer gate nanostructure used for charge pumping experiments. Left: SEM image of a device similar to the one used for the measurements. Right: Schematic cross-sectional views of the device across X-cut and Y-cut. Please click here to view a larger version of this figure.

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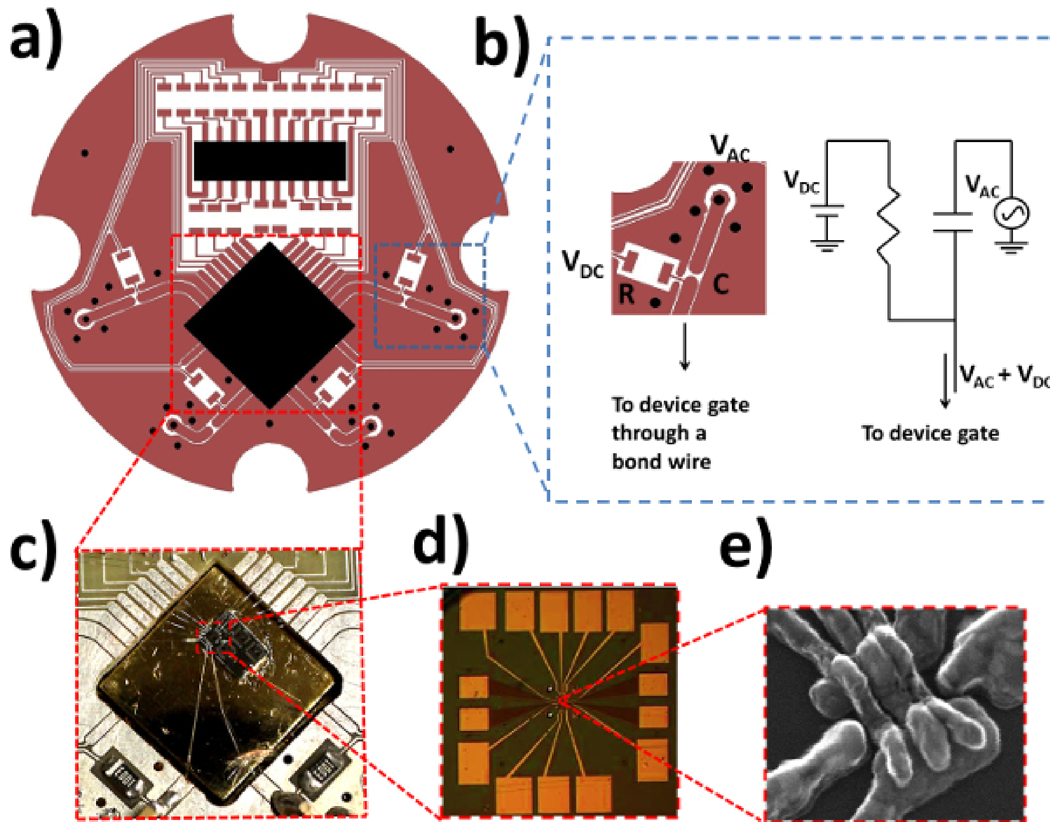

Figure 3. Electrical connections to the sample. (**A**) Layout of the printed circuit board. (**B**) Magnification of a region of the PCB with a bias-tee (left) and equivalent circuit (right). (**C**) A chip with 6 individual fields glued on the chip holder and bond wires for electrical connection to the PCB. (**D**) Microscopic image of an individual field after nanofabrication. (**E**) SEM image of the gate layout at the center of the gate oxide region. Please click here to view a larger version of this figure.

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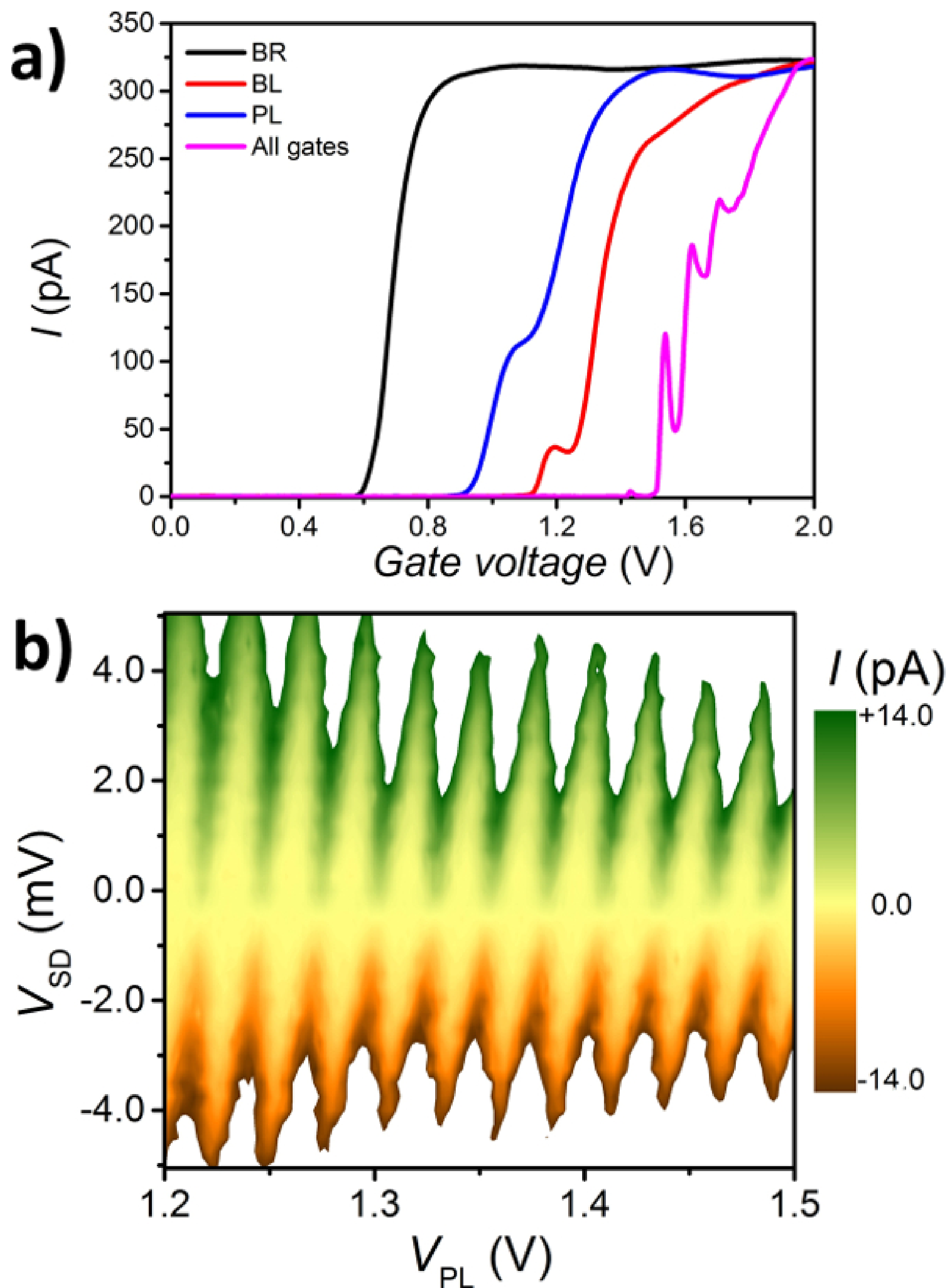

Figure 4. Preliminary tests. (**A**) Source-drain ac current (root mean square) as a function of different gate voltages. Traces are measured with a lock-in amplifier with 50 μV_{RMS} excitation at 113.17 Hz. For individual gate voltage traces the remaining gate voltages are fixed at 2.0 V, except for $V_{C1} = V_{C2} = 0.0$ V. (**B**) Color map of source-drain current as a function of plunger gate voltage and source-drain bias voltage. $V_{SL} = 1.5$ V, $V_{DL} = 1.15$ V, $V_{BL} = 0.78$ V, $V_{BR} = 0.85$ V, $V_{C1} = V_{C2} = 0.0$ V. Please click here to view a larger version of this figure.

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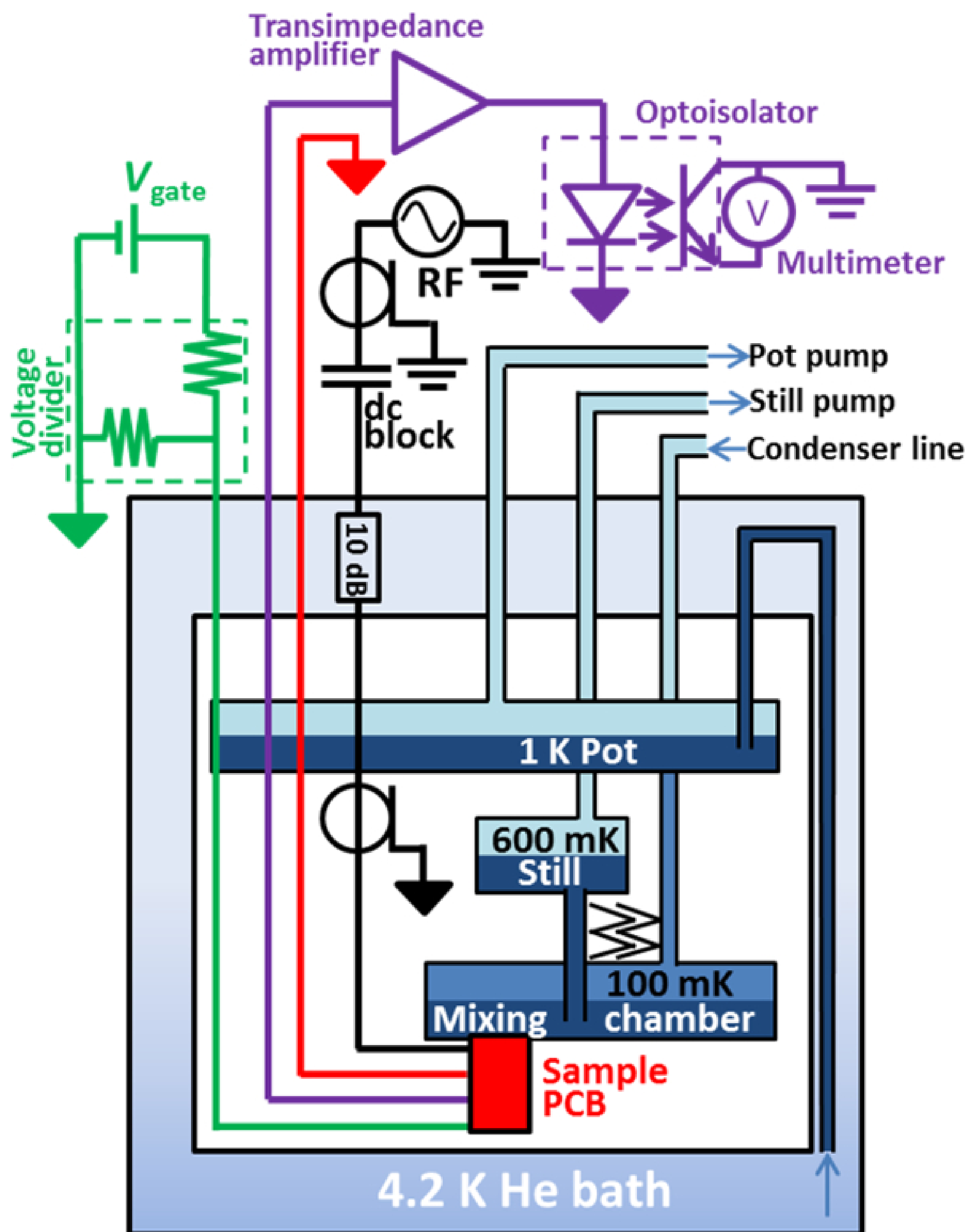

Figure 5. Schematic of the measurement set-up. Twenty dc lines (green) and three coaxial rf lines (black) connect the RT electronics to the PCB. The drain of the pump (purple) is connected to a transimpedance amplifier and to a digital multimeter via an optoisolator, while the source contact (red) is grounded. Separate ground connections (indicated with different symbols) are used for the electronic instrumentation and the cryostat electric lines. Please click here to view a larger version of this figure.

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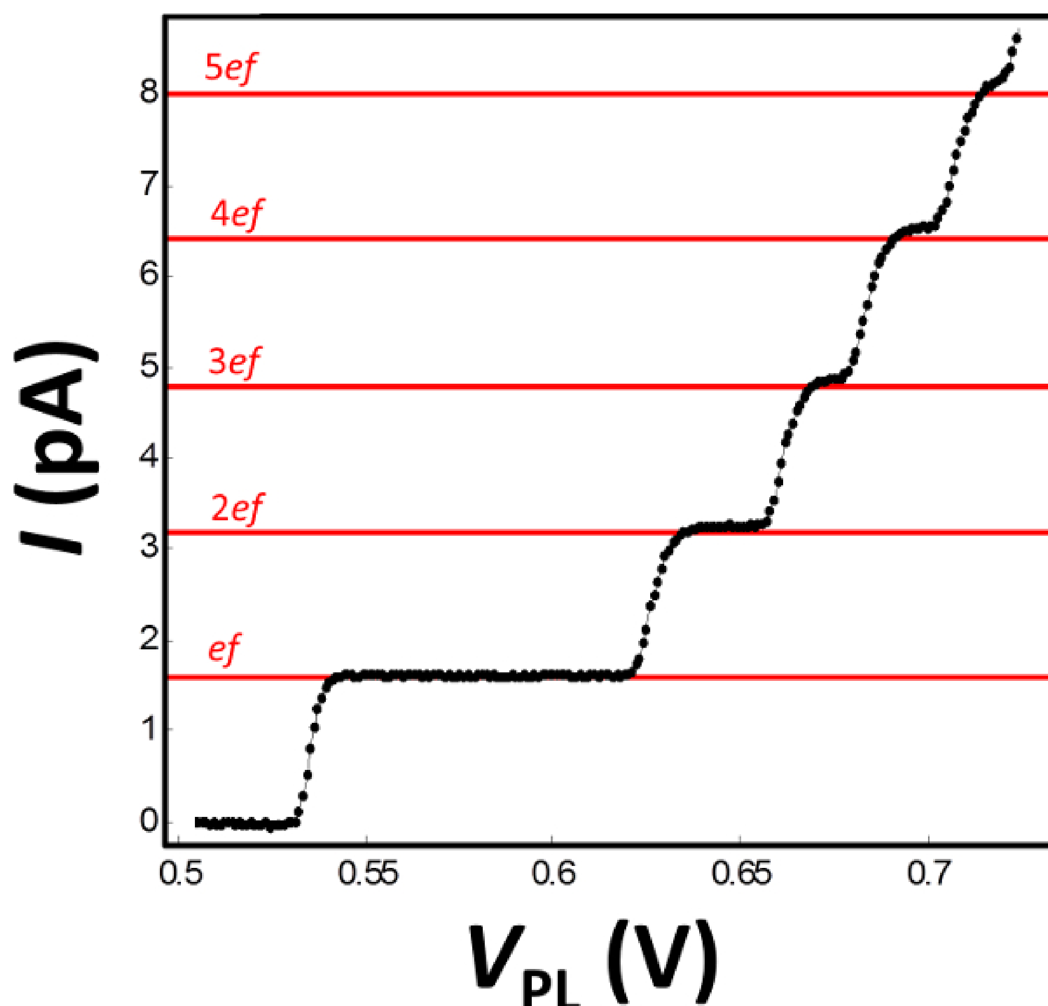

Figure 6. Current quantization. Pumped current as a function of V_{PL} for two-signal sinusoidal drive at f = 10 MHz applied to gates BL and PL. Phase difference = 49 deg, $V^{RF}{}_{PL} = V^{RF}{}_{BL}$ = 0.31 V_{pp}. The ideal position of the pumping plateaux at integer multiples of *ef* are shown as red horizontal lines. Please click here to view a larger version of this figure.

Discussion

The protocol reported in this paper describes the techniques to fabricate silicon MOS QDs, as well as the experimental procedures to test their functional integrity and operate them as single-electron pumps. Remarkably, by tailoring the gate design, the same fabrication process can be employed to produce devices suitable for quantum bit readout and control[17], as well as charge pumping[12,13]. We note that many of the process parameters quoted in this article may vary depending on the fabrication tools used (calibration, make or model), as well as on the type of silicon substrate (thickness and background doping density). Quantities such as lithography exposure dose or development time, etching or oxidation duration, have to be carefully calibrated and tested to ensure a reliable yield. Furthermore, it is crucial to avoid cross-contamination arising from the use of the same fabrication tools for different processes. To this end, a number of critical steps are carried out with equipment exclusively dedicated to silicon processing such as metal evaporators, oxygen furnaces and HF baths.

More generally, silicon is drawing a growing interest as the material of choice to realize charge pumps[18-20]. This is partly due to the attractive perspective of implementing a new quantum-based electric current standard using an industry-compatible silicon process. This would benefit from well-established and reliable integration techniques for scalability, parallelization and driving overhead. Importantly, a full complementary MOS (CMOS) technology, free of traditional metal as the gate material, has shown greatly reduced background charge fluctuations in single-electron devices[21]. Such fluctuations can be harmful in achieving metrological accuracies.

The protocol discussed here is limited to the realization of MOS nano-devices with metal gates. Therefore, to achieve full industrial compatibility and reduce charge fluctuations, it would be needed to modify the gate deposition techniques and use highly doped polycrystalline silicon as the gate material.

In conclusion, the MOS QD pumps discussed here have recently combined the technological advantage of silicon with very good performance in terms of accurate current generation[13]. This stems from the high flexibility of the design and fabrication process which allow one to stack multiple gate layers leading to a compact and versatile system. The resulting fine tunability of the electrostatic confinement of the dot together with the

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potential to reduce background charge fluctuations sets the stage to overcome the main challenges observed in other semiconductor pumps[22,23].

Disclosures

The authors have nothing to disclose.

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