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Interface Optimization and Transport Modulation of Sm_2O_3/InP Metal Oxide Semiconductor Capacitors with Atomic Layer Deposition-Derived Laminated Interlayer

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Abstract: In this paper, the effect of atomic layer deposition-derived laminated interlayer on the interface chemistry and transport characteristics of sputtering-deposited Sm_2O_3/InP gate stacks have been investigated systematically. Based on X-ray photoelectron spectroscopy (XPS) measurements, it can be noted that ALD-derived Al_2O_3 interface passivation layer significantly prevents the appearance of substrate diffusion oxides and substantially optimizes gate dielectric performance. The leakage current experimental results confirm that the Sm_2O_3/Al_2O_3/InP stacked gate dielectric structure exhibits a lower leakage current density than the other samples, reaching a value of 2.87×10^{-6} A/cm^2. In addition, conductivity analysis shows that high-quality metal oxide semiconductor capacitors based on Sm_2O_3/Al_2O_3/InP gate stacks have the lowest interfacial density of states (D_{it}) value of 1.05×10^{13} cm^{-2} eV^{-1}. The conduction mechanisms of the InP-based MOS capacitors at low temperatures are not yet known, and to further explore the electron transport in InP-based MOS capacitors with different stacked gate dielectric structures, we placed samples for leakage current measurements at low varying temperatures (77–227 K). Based on the measurement results, Sm_2O_3/Al_2O_3/InP stacked gate dielectric is a promising candidate for InP-based metal oxide semiconductor field-effect-transistor devices (MOSFET) in the future.

Keywords: MOS capacitors; Sm_2O_3 high-k gate dielectric; atomic layer deposition; conduction mechanisms; interface state density

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1. Introduction

As the integration of IC continues to increase, CMOS feature sizes will also continue to decrease in order to reduce the cost of individual transistors, increase the switching speed of transistors, and reduce the power consumption of the circuit. As the feature size of CMOS devices continues to decrease, it will also cause the SiO_2 gate dielectric and Si substrate used in conventional processes to decrease in size as well. When the size is smaller than a certain limit, the gate leakage current will grow exponentially, while the device will not operate properly due to the laws of quantum physics [1,2]. The use of high-k materials for the replacement of SiO_2 gate dielectrics is an option that has been shown to be feasible [3]. Among these high k materials, samarium oxide (Sm_2O_3) is considered as the next potential gate dielectric due to its high dielectric constant (~15) [4], sufficiently large band gap (5.1 eV) [5], low hygroscopicity, and high chemical and thermal stability [6]. Coulomb scattering and phonon scattering at the interface between the high-k gate dielectric and the channel material lead to a significant reduction in channel mobility, which severely affects

the further increase in the speed of CMOS logic devices. Selecting channel materials with high mobility is an effective way to solve this problem [7]. Compared with conventional Si-based material CMOS devices, III-V group semiconductors have advantages due to their large switching speed and small dynamic power consumption [8]. Among the group III-V semiconductors, InP has received more attention due to its higher carrier mobility and smaller band gap [9].

However, InP is prone to the formation of interfacial defects, which can limit the operating performance of the device [10]. Also, a surface with many chemical impurities can have a considerable impact on the performance of InP MOS capacitors [11]. High D_{it} leads to the frequency dispersion of the Fermi energy level pegging and capacitance, which also prevents the formation of inverse or accumulation layers in CMOS devices [12].

Different InP surface passivation methods have been investigated for a long time, including low-temperature processes [13], ozone treatment [14], chemical etching [15], and sulfide solution passivation [16,17]. A great deal of work has also been devoted to atomic layer deposition (ALD) passivation layers to modulate the InP interface [18]. It has been demonstrated that ALD-derived Al_2O_3 films can effectively suppress the interfacial diffusion from the substrate to the high-k films. More importantly, the operating temperature can be kept low (~200 °C) when the Al_2O_3 film is on the passivated substrate surface. There are previous reports confirming that the insertion of Al_2O_3 between the high-k gate dielectric and GaAs can improve the thermal stability. However, even in the presence of an Al_2O_3 passivation layer to improve the interface, the diffusion of In and P elements into the gate dielectric still has an impact on the electrical characteristics of the device when fabricating InP MOS capacitors. R. V. Galatage et al. reported that the In-O and P-O states at the interface lead to a degradation of the electrical characteristics [19]. Their results also demonstrated the effectiveness of ALD-derived Al_2O_3 passivation layers between the gate dielectric and the InP substrate. Chee-Hong An et al. systematically analyzed that Al_2O_3 can inhibit dissociation and reactant diffusion in InP substrates [20]. However, the effect of the position of the Al_2O_3 passivation layer on the electrical properties and interfacial bonding state of InP MOS devices has not been reported systematically.

In this work, we deposited Sm_2O_3 films by magnetron sputtering and obtained Al_2O_3 passivation layers by ALD equipment to fabricate three different gate stacks on InP substrates, corresponding to $Al_2O_3/Sm_2O_3/InP$, $Al2_2O_3/Sm_2O_3/Al_2O_3/InP$, and $Sm_2O_3/Al_2O_3/InP$, respectively. X-ray photoelectron spectroscopy (XPS) and electrical measurements were used to investigate the effect of Al_2O_3 passivation position on the chemical composition and electrical parameters of the interface. In addition, the leakage current conduction mechanisms (CCMs) of InP-based MOS capacitors with three different laminated gate electrical stacks measured at room temperature and low temperature (77–227 K) were systematically investigated.

2. Materials and Methods

In this work, we chose sulfur-doped n-type InP wafers as the substrate for fabricating MOS capacitors. Before depositing the Sm_2O_3 gate dielectric, the wafers were subjected to a standard degreasing process by sequential immersion in ethanol and acetone for 5 min each. After that, the wafers were immersed in 20% ammonium sulfide solution for 15 min to remove the native oxides. Then, the wafers are rinsed with deionized water and then blown dry with high purity nitrogen gas. The cleaned wafers are transferred to an ALD system (MNT-PD100Oz-L6S1G2, MNT Micro and Nanotech). On the ALD process, plasma O_2 and trimethylaluminum (TMA) were selected as the oxidant and aluminum metal precursor, and a 2 nm Al_2O_3 passivation layer was deposited on the InP substrate. The Al_2O_3 passivation layers were deposited by using 30 pulse cycles of plasma O_2 precursors [O_2(2s)/Ar purge (25s)] and 15 pulse cycles of trimethylaluminum (TMA) and plasma O_2 [TMA (0.03s)/O_2 2s/Ar purge (25s)], respectively. During this process, the chamber pressure and the deposition temperature were maintained at 35 Pa and 200 °C. After ALD Al_2O_3 passivation, the wafers were transferred to a sputtering chamber to deposit Sm_2O_3 gate

dielectrics by sputtering samarium target with purity of 99.9%. When the chamber pressure was 0.8 Pa, Sm_2O_3 thin film was deposited under an Ar/O_2 (50/10 sccm) atmosphere. To explore the electrical characteristics of Sm_2O_3/InP MOS capacitors with different stacking positions of Al_2O_3 passivation layers, a 200-µm-diameter Al electrode was deposited by thermal evaporation, while an aluminum electrode was grown on the back side to form an ohmic contact. Figure 1 demonstrates the schematics of InP-MOS capacitors based on different stacked gate dielectric structures. Sample S1 corresponds to Al_2O_3 (2 nm)/Sm_2O_3 (8 nm)/InP, sample S2 corresponds to Al_2O_3 (2 nm)/Sm_2O_3 (6 nm)/Al_2O_3 (2 nm)/InP, and sample S3 corresponds to Sm_2O_3 (8 nm)/Al_2O_3 (2 nm)/InP, respectively. By using the ESCALAB 250Xi system, XPS (X-ray photoelectron spectroscopy) measurements were performed at Al Ka (1486.7 eV) to investigate the interfacial chemical properties of the Sm_2O_3/InP gate stack and the chemical function of the Al_2O_3 passivation layer. Furthermore, the escape angle used in obtaining the XPS profiles is 50° and the corresponding probing depth is about 1–10 nm. Ultraviolet-visible spectroscopy (Shimadzu, UV-2550) was performed to obtain the samples' optical band gap. The physical thickness of the above samples was extracted by using spectroscopic ellipsometry measurements (SANCO Inc., Shanghai, China, SC630) with the help of the Cauchy-Urbach model. The Cascade Probe Station was connected to the semiconductor analysis equipment (Agilent B1500A) for capacitance-voltage (C-V), transconductance-voltage (G-V), and leakage current-voltage (I-V) measurements at room temperature. For low temperature (77–227 K) leakage current testing, the Lake Shore Cryotronics Vacuum Probing Station was used.

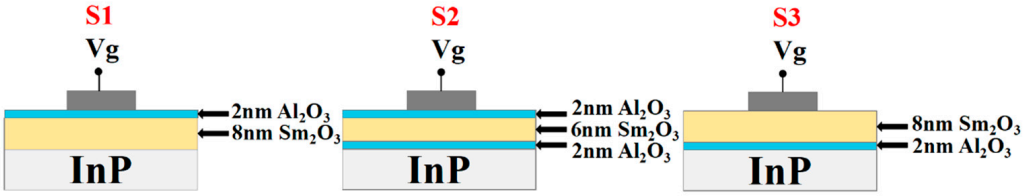

Figure 1. Schematics of InP-based MOS capacitors based on different stacked gate dielectrics.

3. Results and Discussion

3.1. XPS Analyses

To evaluate the chemical bonding states of various stacked gate dielectrics, XPS measurements were carried out. Figure 2 displays the In 3d, P 2p, and O 1s XPS spectra of three samples with various stacked gate dielectrics. It can be noted that In 3d spectra can be deconvoluted into four components that represent the InP, $InPO_4$, $In(PO_3)_3$, and In_2O_3, respectively. The relative intensity values of the different components have been extracted and are shown in Figure 3a. For S2 and S3, the contents of $In(PO_3)_3$ and In_2O_3 shows a decreasing trend, indicating that the ALD-derived Al_2O_3 passivation layers prior to Sm_2O_3 deposition can significantly prohibit the formation of In and P suboxides, which can be attributed to the interface cleaning function of plasma O_2 [21]. Compared to S2, the peak areas of $InPO_4$ corresponding to S1 and S3 remain approximate at about 7.89% and 5.20%, which is much lower than that of S2 (19.41%), indicating that double deposition of ALD-derived Al_2O_3 may accelerate the diffusion of oxygen in the substrate and the formation of indium phosphate. During the secondary deposition of Al_2O_3, more oxygen vacancies may generate, which can be ascribed to plasma O_2 acting as an oxygen source, and promote the oxygen interdiffusion between Al_2O_3 passivation layers and the InP substrate. $In(PO_3)_3$ can react with In to produce InP and $InPO_4$ using the following reaction Equation [22].

$$8In + 4In(PO_3)_3 \rightarrow 3InP + 9InPO_4 \quad (1)$$

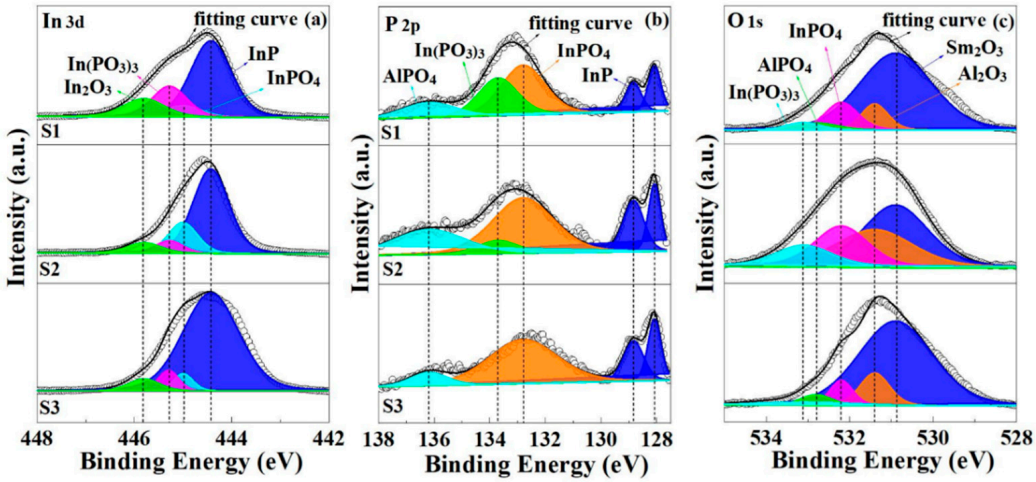

Figure 2. (**a**) In 3d, (**b**) P 2p, and (**c**) O 1s XPS spectra for S1, S2, and S3 sample.

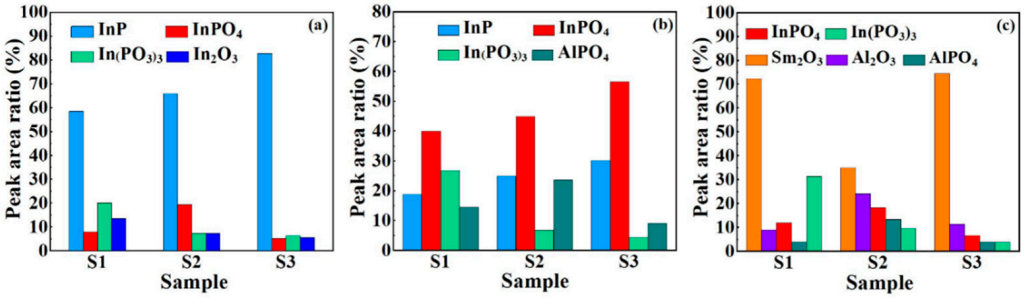

Figure 3. Peak area ratio histograms of (**a**) In 3d, (**b**) P 2p, and (**c**) O 1s spectra.

More importantly, sample S3 shows a tendency to decrease the content of $In(PO_3)_3$ and $AlPO_4$ compared to sample S2, which can give a detailed illustration from the phenomenon of P 2p spectral changes. As shown in Figure 2b, it can be noted that P 2p spectra can be deconvoluted into four components, which represent InP, $InPO_4$, $In(PO_3)_3$, and $AlPO_4$, respectively. No P_2O_5 was detected in all samples, which can be attributed to the fact that gaseous P_2O_5 generated during the deposition can easily diffuse through the defects in the gate dielectric [22]. The peak area ratio of $In(PO_3)_3$ for S2 and S3 showed a significant decreasing trend compared to S1, indicating that Al_2O_3 prior to the deposition of Sm_2O_3 gate dielectric can inhibit the formation of P-O bound states and improve the interfacial quality. The detection of $AlPO_4$ in P 2p spectra can be attributed to the reaction equation described below [23].

$$4Al + 7O_2 + 2In(PO_3)_3 + 2InP \rightarrow 4AlPO_4 + 4InPO_4 \quad (2)$$

Based on the mentioned reaction above, it can be inferred that two depositions of Al_2O_3 passivation layers increase the formation of $AlPO_4$, which is confirmed by the change in peak area ratio shown in Figure 3c. In order to systematically explore the interfacial chemistry of various stacked gate dielectrics, O 1s spectra were investigated and are shown in Figure 2c. O 1s spectra can be deconvoluted into Sm_2O_3, Al_2O_3, $InPO_4$, $In(PO_3)_3$, and $AlPO_4$. According to the reaction Equation (2), in the plasma O_2 atmosphere, $In(PO_3)_3$ can react with O_2 to produce $AlPO_4$ and $InPO_4$ and leads to the disappearance of $In(PO_3)_3$. In agreement with the previous In 3d and P 2p spectra, S1 has the largest $In(PO_3)_3$ content, leading to a decrease in interfacial quality and deterioration of electrical properties. Meanwhile, $AlPO_4$ of S2 is the highest, originating from the second deposition of Al_2O_3. For S3 sample, the contents of $InPO_4$, $AlPO_4$, and In_2O_3 were significantly controlled, indicating that the addition of an ALD-derived Al_2O_3 layer prior to the deposition of Sm_2O_3 gate dielectric could reduce the generation of suboxides and improve the interfacial quality.

3.2. Band Alignment Characteristics

To assess the optical characteristics of the three various stacked gate dielectrics, UV-Vis spectroscopy was used to obtain the absorption spectra and the optical bandgap values (Figure 4) of samples S1, S2, and S3 were determined to be 5.49, 5.51, and 5.63 eV, respectively, based on the Tauc relationship [24]. Compared with pure Sm_2O_3 and pure Al_2O_3, the band gaps of three various stacked gate dielectrics showed a value balance [25]. Also, this section investigates the valence band maximum (VBM) of various stacked gate dielectrics, as the valence band alignment is crucial for assessing the interface quality. As shown in Figure 5a, the band gap values of InP substrates were derived from XPS measurements, while the valence bands of samples S1, S2, and S3 were deduced from the absorption spectra by linear extrapolation. Based on Kraut's method [26], we also calculated the valence band shift (ΔE_V) to evaluate the valence band electronic structure of the samples. By using Sm $3d_{5/2}$ and In 3d core-level spectra, the ΔE_V of high-k/InP gate stacks was determined based on the following formula:

$$\Delta E_V = (E_{In\ 3d} - E_V)_{InP} - (E_{Sm\ 3d} - E_V)_{high-k} - (E_{In\ 3d} - E_{Sm\ 3d})_{high-k/InP} \quad (3)$$

where $E_{In\ 3d}$ (InP) and $E_{Sm\ 3d}$ (high-k) corresponding to the core-level positions are extracted to be 445.8 and 1084.3 eV. In addition, the E_v (InP) and E_v (high-k) represent the VBM (Valence-Band Maximum) of the bulk materials. The values of ΔE_v are calculated as 1.87, 1.82, and 1.76 eV, respectively, based on the binding energy difference in the high-k/InP structure. Meanwhile, the value of the conduction band offset (ΔE_c) is obtained by subtracting the extracted ΔE_v and the band gap of the InP (1.34 eV) from the band gap of dielectric layers [27].

$$\Delta E_C\ (high - k/InP) = E_g\ (high - k) - \Delta E_V(High - k/InP) - E_g(InP) \quad (4)$$

As shown in Figure 5b, the ΔE_c values for the three samples were calculated as 2.28, 2.35, and 2.53 eV. According to previous reports in the literature, ΔE_c is related with the tunneling leakage current. The higher ΔE_c indicates that the leakage current of the Sm_2O_3/Al_2O_3/InP samples is smaller.

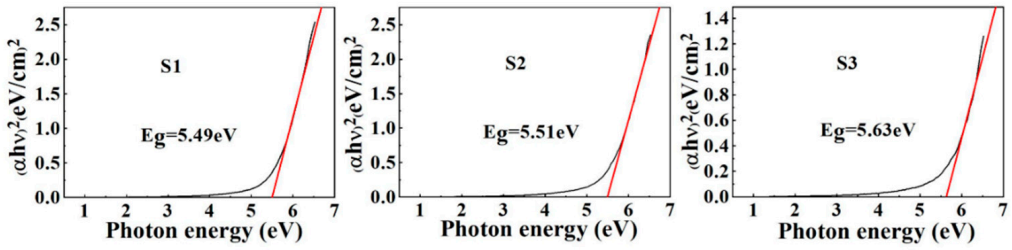

Figure 4. The determination of band gaps for sample S1, S2, and S3.

3.3. Electrical Properties of InP-MOS Capacitors

3.3.1. Capacitance-Voltage Measurements

The frequency dependent capacitance-voltage curves of sample S1, S2, and S3 with double sweep mode are shown in Figure 6a–c. When the frequency increases, all samples show a decreased accumulation capacitance.

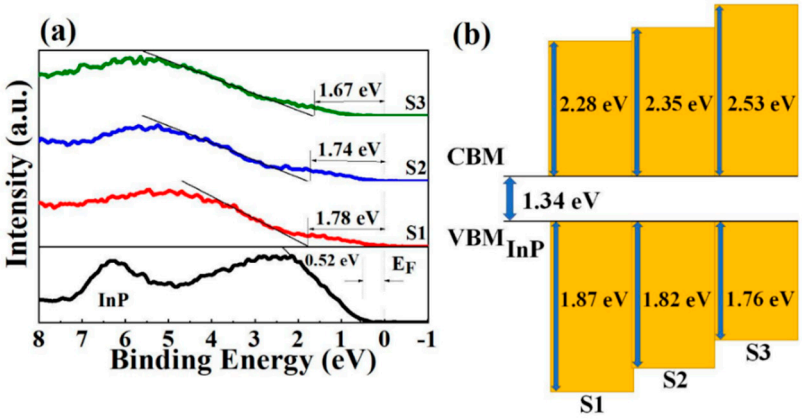

Figure 5. (**a**) Valence band spectra; (**b**) Schematic band diagram of S1, S2, and S3 sample.

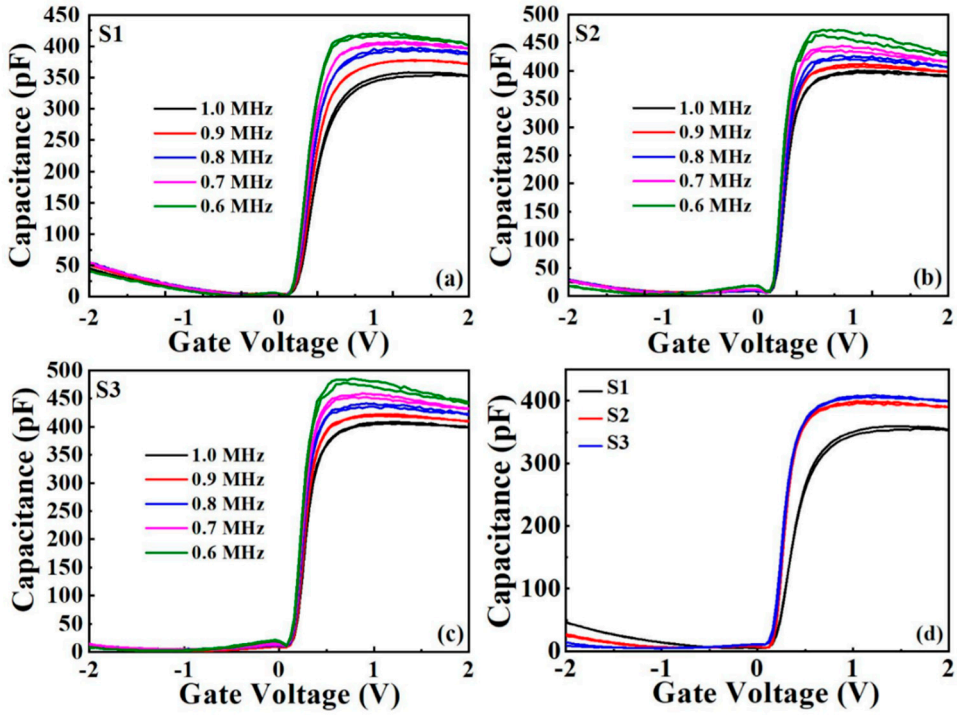

Figure 6. (**a**–**c**) Capacitance–voltage (C–V) curves for S1–S3 measured at different frequency (0.6–1 MHz). (**d**) Capacitance–voltage (C–V) curves for all samples measured at 1 MHz.

Meantime, at high frequency conditions, the series resistance will deviate from the predetermined theoretical value due to the disappearance of the interface trap charge. On the contrary, at low frequencies, when the oxide capacitance (C_{ox}) connects with the space charge capacitance (C_{sc}), the value of the accumulation region increases with the series resistance due to the interface state showing frequency-dependent properties [28–30].

The decrease in the accumulation capacitance can be attributed to the fact that the interfacial traps do not have enough time to respond to the voltage frequency [30]. The maximum accumulation capacitance and minimum hysteresis voltage were observed in the S3 sample, indicating that the Al_2O_3 passivation layer suppressed the appearance of In and P oxides and the formation of low-K interfacial layers. To evaluate the interface quality, important electrical parameters such as equivalent oxide thickness (EOT), dielectric constant (k), flat band voltage (V_{fb}), hysteresis voltage (ΔV_{fb}), oxidation charge density (Q_{ox}), and boundary trapped oxide charge density (N_{bt}) were extracted from the test curves, and these data are presented in Table 1. The variation of V_{fb} depends on the values of oxide capacitance and bulk oxide charge [31]. The k values corresponding to samples S1, S2,

and S3 are calculated to be 12.96, 14.39, and 14.75, which are consistent with the previous investigation [4].

Table 1. MOS capacitors electrical parameters obtained from C−V and *J*–*V* Curves.

Sample	EOT (nm)	k	V_{fb} (V)	$\triangle V_{fb}$ (mV)	Q_{ox} (cm^{-2})	N_{bt} (cm^{-2})	J (A/cm^{-2})
S1	3.01	12.96	0.25	3.44	-1.62×10^{12}	-2.46×10^{10}	1.07×10^{-5}
S2	2.71	14.39	0.21	5.16	-1.43×10^{12}	-4.11×10^{10}	8.42×10^{-6}
S3	2.65	14.75	0.19	1.55	-1.30×10^{12}	-1.26×10^{10}	2.87×10^{-6}

A small V_{fb} of 0.19 V was observed for sample S3. This phenomenon can be explained by the following statement: electrons are easily captured by oxygen vacancies to form negatively charged interstitial oxygen atoms [32] and as fewer oxygen vacancies exist at the interface, the smaller the positive flat voltage required to maintain the band unbent [33]. Also, the hysteresis voltage depends on the boundary trap caused by the intermixing of the high K layer and the interfacial layer [34]. The value of the hysteresis voltage reaches a minimum (1.55 mV) for S3, indicating that the boundary trapping charge becomes weaker after the insertion of Al_2O_3 between the gate dielectric and the substrate. The Q_{ox} and N_{bt} values were calculated from the obtained V_{fb} and ΔV_{fb} values by the following equations [35].

$$Q_{ox} = -\frac{C_{\max}\left(v_{fb} - \varphi_{ms}\right)}{qA} \quad (5)$$

$$N_{bt} = -\frac{C_{\max} \triangle V_{fb}}{qA} \quad (6)$$

where φ_{ms} is the contact potential difference between Al electrode and InP substrate, q is the electronic charge, and A is the Al electrode areas. According to Table 1, it can be noticed that S3 has the lowest Q_{ox} and N_{bt}, which implies the reduction of interfacial trap defects and the optimization of interfacial properties.

3.3.2. Conductivity-Voltage Measurements

Moreover, to quantify the interface defect distribution for all samples, the interface state density (D_{it}) has been extracted by the conductivity-voltage measurements with frequencies varying from 100 kHz to 1 MHz. D_{it} is related to the parallel interfacial trap capacitance (C_{it}) and parallel conductivity (G). At the same time, C_{it} can be related by the following equation. $C_{it} = qD_{it}$, while the condition is that the position of the energy level does not change D_{it}. The basic principle of conductivity measurements is to analyze the losses due to the diversity of charge states at the trap level. Near the Fermi level, the synchronous conductivity occupancy is mobilized by the interfacial traps to produce a regular variation. The maximum loss occurs when the interface trap is resonantly shifted with the applied AC signal ($\omega\tau = 1$). The response time of the characteristic trap changes the frequency, $\tau = 2\pi/\omega$. The capture and emission rates from Shockley-Redhall theory modulate the response time [36]:

$$\tau = \frac{exp[\Delta E/k_B T]}{\sigma v_{th} D_{dos}} \quad (7)$$

where there is an energy difference ΔE between the trap level E_T and the edge of the majority carrier band, v_{th} is the majority carrier being thermally activated to obtain the average velocity, D_{dos} is the effective density of states of the majority carrier band, k_B is the Boltzmann constant, and T is the temperature [37]. The curves between conductivity (G/ω) and gate voltage for all samples are shown in Figure 7a–c. The apparent shift of the conductivity peak proves the validity of the Fermi-level shift and confirms the existence of

the Fermi-level deconvolution effect [38]. Assuming that the underlying surface oscillations can be neglected, the value of D_{it} is inferred using the normalized parallel conductivity peak $(G_P/\omega)_{max}$ [39].

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_p}{\omega}\right)_{max} \quad (8)$$

where A is the device area. It is necessary to confirm the transformation law between the band bending potential of the energy location E_T and the trap energy level distribution. Furthermore, the values of E_T can be determined by the frequency of $(G_P/\omega)_{max}$, where Equation (8) is used to calculate D_{it} and to correspond its value to ΔE [40].

$$\Delta E = (E_C - E_T) = \frac{k_B T}{q} In\left(\frac{\sigma v D_{dos}}{2\pi f_{max}}\right) \quad (9)$$

Figure 7d shows the variation of D_{it} for the three samples. With the increase of ΔE, the value of D_{it} shows an increasing trend. However, S3 possesses a lower density of interfacial states compared to S1 and S2, which indicates that the insertion of an Al_2O_3 passivation layer between the Sm_2O_3 gate dielectric and the InP substrate can suppress the formation of In and P suboxides and improve the quality of MOS capacitors.

We compared some of the data obtained from this work with some previously published work. As can be seen in Table 2, the Sm_2O_3 dielectric has a smaller leakage current density than TiO_2 and HfO_2, indicating that the Sm_2O_3 stacked gate dielectric has a larger conduction band shift, resulting in an increased barrier height and thus a reduced leakage current density. The Sm_2O_3 stacked gate dielectric has the smallest hysteresis value, indicating that the trapped charge in the gate dielectric is not very sensitive to the frequency response of the voltage, and will trap fewer electrons to keep the energy band from being bent, while the device maintains a consistent response to different test voltages in the antipattern region. In the interface state density, it is smaller than HfO_2 as the gate dielectric directly deposited in InP, but it seems to be higher than TiO_2 gate dielectric, considering the different testing methods, the interface state density of the current work is obtained directly by conductivity method with accuracy, the previous work is by C–V curve, there may be some differences.

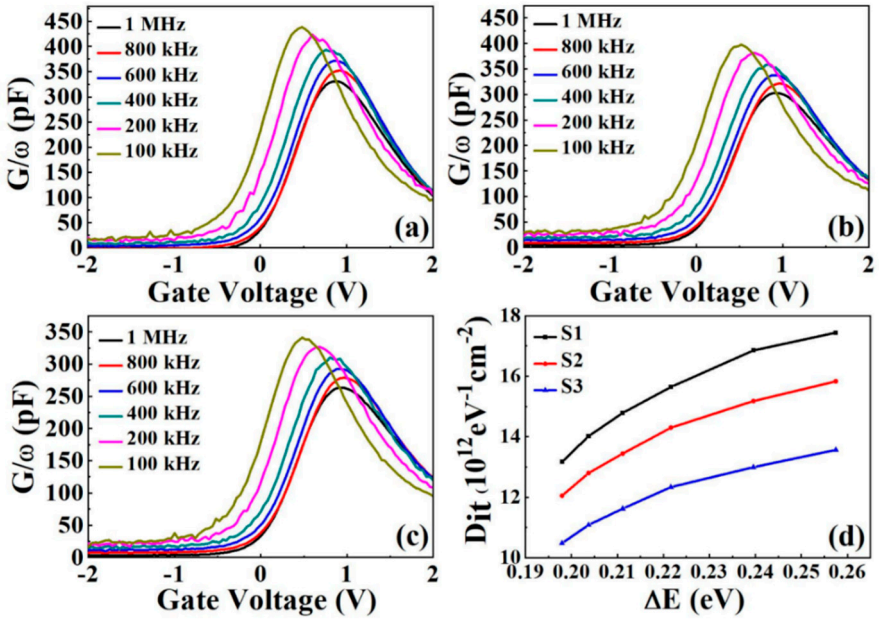

Figure 7. Multi-frequency G–V characteristics of InP-based MOS capacitors of (**a**) S1, (**b**) S2, and (**c**) S3. (**d**) Energy distributions of Dit for S1, S2, and S3.

Table 2. Comparison of different InP MOS capacitor parameters.

	$Sm_2O_3/Al_2O_3/InP$ (This Work)	PMA-TiO_2/S-InP [41]	TiO_2/S-InP [41]	10 Å Si IPL/51 Å HfO_2/InP [42]	70 Å HfO_2/InP [42]	HfO_2 (10 nm)/Al_2O_3 (0.2 nm)/InGaAs/InP [43]
Leakage current density (A/cm^2)	2.87×10^{-6} at 1 V	1.9×10^{-7} at 2 V 2.7×10^{-5} at −2 V	5.01×10^{-6} at 2 V 1.5×10^{-2} at −2 V	1.32×10^{-3} at 1 V	3.94×10^{-2} at 1 V	2.4×10^{-2}
k	14.75	39	34	/	/	/
ΔVfb (mV)	1.55	40	250	240	280	/
D_{it} (cm^{-2}eV^{-1})	(G-V) 1.05×10^{13}	(C-V) 3.1×10^{11}	(C-V) 5×10^{11}	(C-V) 3-8 $\times 10^{12}$	(C-V) 2-9 $\times 10^{13}$	(C-V) 2×10^{12}

3.3.3. $J-V$ Analyses and Conduction Mechanisms at Room Temperature

Figure 8a shows the leakage current characteristics of all samples measured at room temperature. The leakage current density (J) values for S1, S2, and S3 at 1 V are 1.07×10^{-5}, 8.42×10^{-6}, and 2.87×10^{-6} A/cm^2, respectively. It can be seen that S1 has a higher leakage current density, which can be attributed to larger interface traps and the border traps that deteriorate the interface quality and degrade the device performance [44]. For the S3 sample, the minimum leakage current density has been observed, which is due to the higher ΔE_c and the suppressed tunneling in the $Sm_2O_3/Al_2O_3/InP$ gate stack [45].

To investigate the leakage current characteristics of various stacked gate dielectrics, we systematically studied three different current conduction mechanisms (CCMs) under substrate injection, as shown in Figure 8b–d. The extracted important electrical parameters are listed in Table 3.

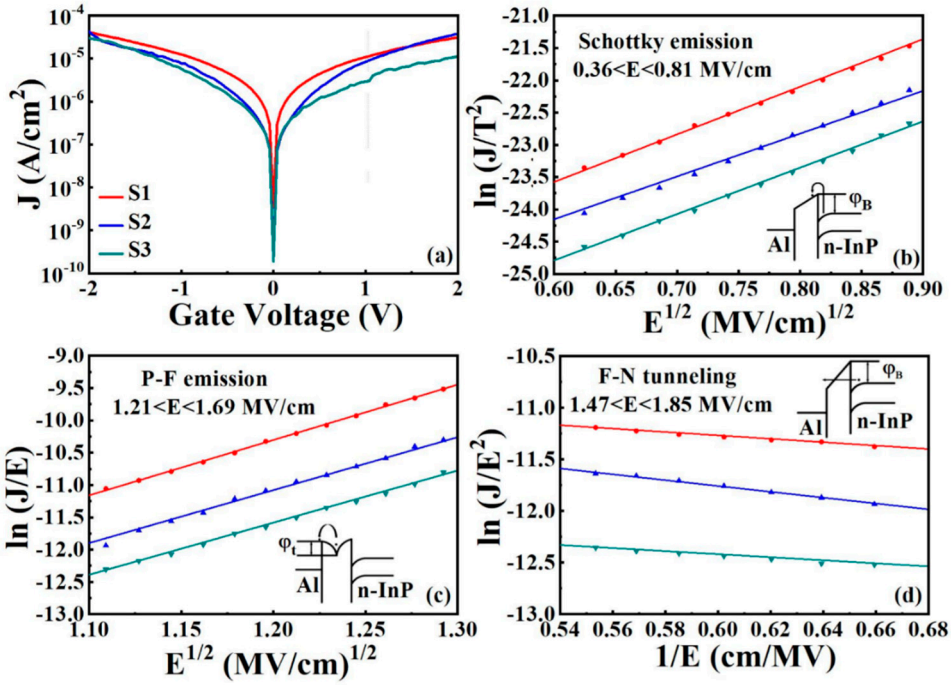

Figure 8. (**a**) J–V characteristics measured at room temperature. (**b**) SE emission, (**c**) PF emission, and (**d**) FN tunneling plots for all the samples under substrate injection.

Table 3. Extracted MOS capacitors electrical parameters measured at room temperature.

Sample	J (A/cm^2)	ε_r	n	ε_{ox}	φ_t (eV)
S1	1.07×10^{-5}	4.00	2.00	11.90	0.53
S2	8.42×10^{-6}	4.96	2.23	13.01	0.54
S3	2.87×10^{-6}	4.23	2.06	13.41	0.55

Schottky emission (*SE*) is a typical type of thermal ionization emission in which charges gain energy to overcome barriers to migration into the dielectric. The standard *SE* can be described as [46]:

$$J_{SE} = A^* T^2 exp\left[\frac{-q\left(\varphi_B - \sqrt{qE/4\pi\varepsilon_0\varepsilon_r}\right)}{k_B T}\right] \quad (10)$$

$$A^* = \frac{4\pi q k_B^2 m_{ox}*}{h^3} = 120\frac{m_{ox}*}{m_0} \quad (11)$$

where A^* is the effective Richardson constant, the free electron mass and the effective mass of electrons in the gate dielectric correspond to m_o and m_{ox*}, E is the electric field, $q\varphi_B$ is the Schottky barrier height, and ε_o and ε_r represent the vacuum dielectric constant and the optical dielectric constant, respectively [47]. It is observed in Figure 8b that at lower electric fields (0.36–0.81 MV/cm), there is a good linear relationship between $\ln(J/T^2)$ and $E^{1/2}$ for S1, S2, and S3. The slope of the SE diagram is denoted as $\sqrt{q^3/4\pi\varepsilon_0\varepsilon_r}/k_B T$. The fitted ε_r and the refractive index n ($n = {\varepsilon_r}^{1/2}$) for S1, S2, and S3 are (4, 2), (4.96, 2.23), and (4.23, 2.06), respectively. All the fits are consistent with the previously reported values [48], revealing that CCM (current conduction mechanism) at room temperature is dominated by SE emission in the low electric field region.

The Poole–Frenkel (*PF*) emission can be ascribed to the thermally excited electrons obtaining sufficient energy to escape from traps into the conduction band of the dielectric at a higher electric field, which can be expressed by the following formula [49]:

$$J_{PF} = AE\, exp\left[\frac{-q\left(\varphi_t - \sqrt{qE/\pi\varepsilon_0\varepsilon_{ox}}\right)}{k_B T}\right] \quad (12)$$

where A represents a constant, the trap energy level of the conduction band corresponds to φ_t, and ε_{ox} represents the dielectric constant. According to the previous theory, $\ln(J/E)$ should have a good proportionality with $E^{1/2}$, as shown in Figure 8c. The ε_{ox} extracted from the slope of the fitted line for all samples was calculated as 11.90, 13.01, and 13.41, which is in agreement with the reported reference [4]. It can be concluded that at higher electric fields (1.21–1.69 MV/cm), the PF emission dominates the CCM of all samples. Also, the value of the trap energy level (φ_t) can be extracted based on the intercept point of the fitted curve described as $lnB - \frac{q\varphi_t}{k_B T}$. As shown in Figure 8c, the calculated values of φ_t are 0.53, 0.54, and 0.55 eV, corresponding to S1, S2, and S3. S3 has the largest φ_t value in the three samples, indicating that the electrons obtain more energy to cross the trap, leading to present the smallest leakage current density in the S3 sample.

The high-field dependent conduction mechanism is represented by Fowler-Nordheim tunneling, which is manifested by the fact that the insulating layer can be penetrated by electrons, which enter the conduction band of the gate dielectric in a high electric field. The leakage current density is linked to other parameters of Fowler-Nordheim (*FN*) tunneling and is described by the following Equation [46]:

$$J_{FN} = \frac{q^3 E^2}{16\pi^2 \hbar \varphi_{ox}}\, exp\left[-\frac{4\sqrt{2m_T^* \varphi_B^{3/2}}}{3\hbar q E}\right] \quad (13)$$

where φ_{ox} is oxide barrier height; m_T^* is the tunneling effective electron mass in the gate oxide film, and the other notations remain unchanged from the previous definitions. Figure 8d shows the curve of $\ln(J/E2)$ versus $1/E$. The slope of the linear fit for the above samples shows an increase in current with increasing electric field, indicating that at high electric fields (1.47–1.85 MV/cm), all three samples are consistent with the *FN* tunneling conduction mechanism. Based on the previous analysis, it can be concluded that all samples are dominated by three main conduction mechanisms. In the lower electric fields,

SE emission dominates, however, in the higher electric fields, PF emission dominates together with FN tunneling.

3.3.4. Low Temperature *J–V* Analyses and Conduction Mechanisms

To investigate the variation of CCMs in Sm_2O_3/Al_2O_3/InP MOS capacitor, low temperature (77–227 K) measurements were performed. The leakage current densities of Sm_2O_3/Al_2O_3/InP MOS capacitors measured at 1 V were extracted as 4.64×10^{-9}, 1.48×10^{-8}, 1.13×10^{-7}, and 1.02×10^{-6} A/cm^2, corresponding to the temperature range of 77–227 K, respectively. By observing the leakage current densities at different temperatures, the Sm_2O_3/Al_2O_3/InP gate stack exhibits nearly three orders of magnitude lower leakage current density at 77 K than that measured at room temperature, indicating that the low temperature is favorable for the MOS capacitor to exhibit optimized *J–V* characteristics. Figure 9b–d show the variation of the CCM under substrate injection along with the temperature trend. The extracted important electrical parameters are listed in Table 4. Figure 9b shows the fitted lines for the vertical temperature range suitable for SE emission at lower electric fields (0.49–0.90 MV/cm). The extracted important electrical parameters are listed in Table 4. With increasing temperature, the values of ε_r and n calculated from the slope and intercept are (20.39, 4.52), (18.53, 4.31), (10.40, 3.22), and (6.10, 2.47). It can be noted that at extremely low temperature of 77–177 K, these values are completely different from the theoretical values, indicating that SE emission is not the dominant conduction mechanism at lower temperatures. Figure 9c shows the curves in the temperature range 77–227 K compatible with PF emission at higher electric fields (0.64–1.44 MV/cm). Again, it can be noted that φ_t and ε_{ox} are not in the expected range of values, indicating that the PF emission is not compatible for all samples at intermediate electric fields of 0.64–1.44 MV/cm. FN tunneling is a potential conduction mechanism because of its dependence on the electric field at low temperatures. Figure 9d shows the fitted line of FN tunneling with a temperature range of 77–227 K at higher electric fields (1.11–1.67 MV/cm), and the established slope indicates that FN tunneling is dominant at low temperatures. In conclusion, the effects of SE emission and PF emission are attenuated due to low temperature, and FN tunneling is used to explain the Sm_2O_3/Al_2O_3/InP stacked gate dielectric structure showing low drain current density.

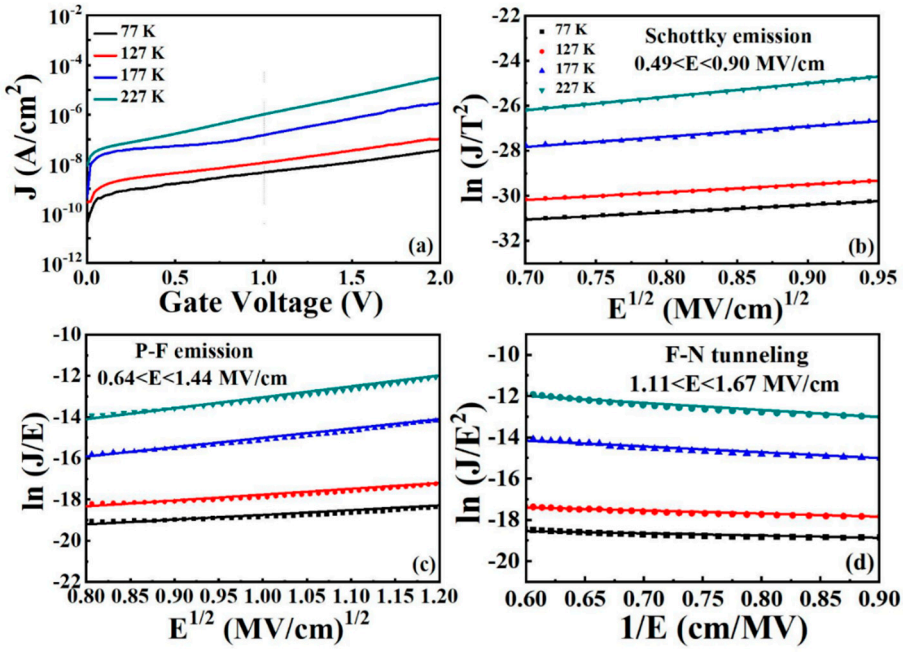

Figure 9. (**a**) J–V characteristics measured at low temperature. (**b**) SE emission, (**c**) PF emission, and (**d**) FN tunneling plots for all the samples under substrate injection.

Table 4. S3's MOS capacitors electrical parameters measured at low temperature.

T	J (A/cm^2)	ε_r	n	ε_{ox}	φ_t (eV)
77 K	4.64×10^{-9}	20.39	4.52	164.88	0.54
127 K	1.13×10^{-8}	18.53	4.31	108.14	0.53
177 K	1.48×10^{-7}	10.40	3.22	42.66	0.50
227 K	1.02×10^{-6}	6.10	2.47	31.05	0.47

Additionally, the integrated dielectric properties in MOS capacitors can be estimated from two important values, including the electron effective mass m^*_{ox} and the barrier height $q\varphi_B$ [50]. The intercept of the SE emission fitting curve described as $\ln\left(120\frac{m^*_{0x}}{m_0}\right) - \frac{q\varphi_B}{k_B T}$ and the slope of the FN tunneling fitting curve expressed as $-6.83 \times 10^7 \sqrt{\left(\frac{m^*_T}{m_0}\right)\varphi_B^3}$ can be calculated together with the above two values. By setting the equation $m^*_{0x} = m^*_T$, the two key physical quantities m^*_{0x} and $q\varphi_B$ of $Sm_2O_3/Al_2O_3/InP$ MOS capacitor are obtained by applying mathematical analysis, which are calculated as 0.23 m_o and 0.95 eV, respectively. Figure 10 shows the determination of the electron effective mass and barrier height for S3 sample. The smaller m^*_{0x} and the higher $q\varphi_B$ are beneficial to obtain better electrical properties and optimized interface quality.

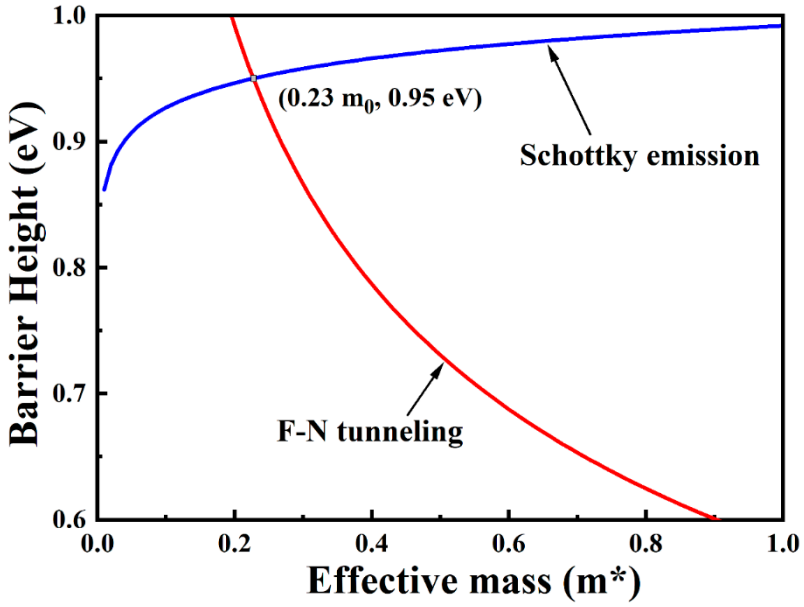

Figure 10. The determination of the electron effective mass and barrier height for S3 sample under substrate injection.

4. Conclusions

In this work, we explore in detail the effect of ALD-derived laminated interlayers on the interfacial chemistry and transport properties of sputter-deposited Sm_2O_3/InP gate stacks. It has been found that $Sm_2O_3/Al_2O_3/InP$ gate stack can obviously prevent the diffusion of the substrate diffusion oxide and substantially optimize the electrical properties of MOS capacitors, including a larger dielectric constant of 14.75, a larger accumulation capacitance, and a lower leakage current density of 2.87×10^{-6} A/cm^2. Three different stacked gate dielectric structures are also evaluated by means of conductivity of the interfacial density of states. The results show that the $Sm_2O_3/Al_2O_3/InP$ stacked gate dielectric achieves the lowest interfacial density of states of 1.05×10^{13} cm^{-2}eV^{-1}. According to the analysis of CCMs, SE emission is dominant in lower electric fields and higher temperature environments, and PF emission as well as F-N tunneling is dominant in higher electric fields. Meanwhile, FN tunneling is the only dominant mechanism at

lower temperatures. Also, to evaluate the properties of the whole MOS capacitor in low temperature environment, m^*_{0x} and $q\varphi_B$ have been determined by a self-consistent method. These findings are of crucial importance for the future fabrication of high mobility InP-based MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices.

Author Contributions: G.H. and Z.F. conceived and designed the experiments; J.L., J.Y. and L.Q. performed the experiments; S.J., Z.D., Q.G. and G.Z. analyzed the data; J.L. and G.H. wrote the paper. All authors have read and agreed to the published version of the manuscript.

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