

Article

Investigation of 3.3 kV 4H-SiC DC-FSJ MOSFET Structures

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Abstract: This research proposes a novel 4H-SiC power device structure—different concentration floating superjunction MOSFET (DC-FSJ MOSFET). Through simulation via Synopsys Technology Computer Aided Design (TCAD) software, compared with the structural and static characteristics of the traditional vertical MOSFET, DC-FSJ MOSFET has a higher breakdown voltage (BV) and lower forward specific on-resistance ($R_{on,sp}$). The DC-FSJ MOSFET is formed by multiple epitaxial technology to create a floating P-type structure in the epitaxial layer. Then, a current spreading layer (CSL) is added to reduce the $R_{on,sp}$. The floating P-type structure depth, epitaxial layer concentration and thickness are optimized in this research. This structure can not only achieve a breakdown voltage over 3300 V, but also reduce $R_{on,sp}$. Under the same conditions, the Baliga Figure of Merit (BFOM) of DC-FSJ MOSFET increases by 27% compared with the traditional vertical MOSFET. $R_{on,sp}$ is 25% less than that of the traditional vertical MOSFET.



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1. Introduction

Currently, most power devices are based on mature Si technology and applied to the high voltage areas. As the material properties of silicon materials are restricted by higher breakdown voltage, operating temperature and switching frequency, a Si IGBT seems to be the better option for higher power systems. However, the switching speed of a Si IGBT is not as fast as that of a Si power MOSFET, so it is difficult for the silicon power devices to achieve higher power conversion efficiency. Instead, wide band gap materials (such as silicon carbide, gallium nitride and gallium oxide) are very suitable for the applications of high power. In terms of physical characteristics, silicon carbide materials have the advantages of a wider band gap, a higher breakdown electric field and higher thermal conductivity [1–5] compared with silicon materials. Therefore, many SiC power devices are developed and applied in various areas.

In general, power MOSFET structures can be divided into lateral double-implanted metal oxide semiconductor field-effect transistors (LDMOSFET) and vertical double-implanted metal oxide semiconductor field-effect transistors (VDMOSFET). In the design of high power devices, an LDMOSFET needs a wider drift region in order to withstand high voltage so that the chip size is larger; a VDMOSFET needs a thicker drift region to maintain higher voltage so that the chip size can be smaller and the problem of the excessive surface electric field can also be improved. Therefore, when designing high voltage devices, the vertical device structure is a better choice.

As the demand of breakdown voltage is increased, the resistances of the JFET region and drift region inside a power MOSFET increase rapidly [6–13], causing power dissipa-

tion. Therefore, it is necessary to develop a power MOSFET with low resistance. To date, 650, 1200 and 1700 V SiC MOSFETs with relatively low specific on-resistance are already commercialized, while 3300 V SiC MOSFET products will be commercialized soon.

This research proposes a floating structure that can reach a breakdown voltage greater than 3300 V and reduce the $R_{on,sp}$. Compared with the traditional whole-column superjunction structure which needs more epitaxial regrowth, the floating-P structure can not only achieve the same result, but also reduce the time and cost of the epitaxial regrowth. In addition, the challenges in fabricating the superjunction MOSFET are the ability to precisely control the concentration and the uniform thickness of each epilayer. It will increase the difficulty of fabrication if more concentrations of the drift region are used. Therefore, two concentrations of the drift region are used.

2. Structures of MOSFETs

Technology Computer Aided Design (TCAD) software (Sentaurus, Synopsys, Mountain View, CA, USA), is used to simulate structures and performances of 3.3 kV 4H-SiC MOSFETs. The three devices are a traditional vertical MOSFET, a MOSFET with three floating P-type structure and a MOSFET with three floating P-type structures and two different concentrations of the drift region, known as the floating superjunction MOSFET (FSJ MOSFET) and the different concentration floating superjunction MOSFET (DC-FSJ MOSFET), respectively. DC-FSJ MOSFET is the main structure designed in this paper. Figure 1a shows a schematic diagram of a traditional vertical MOSFET with an epitaxial layer thickness of 30 μm . The concentration and thickness are commonly used in academia and the industry for 3.3 kV 4H-SiC MOSFET. When the V_{DS} (Drain-source voltage) is applied and the V_{GS} (Gate-source voltage) is larger than the threshold voltage, the MOSFET will be turned on and the current will vertically flow through the MOSFET from the drain to the source. When the V_{GS} is smaller than the threshold voltage and the V_{DS} is still applied, the MOSFET will be turned off. There will be no more current, the MOSFET will be then depleted and the electric field is induced. If the electric field is larger than the critical value, the MOSFET will break down. Therefore, the structure and parameters need to be well designed [14–23]. Figure 1b shows a schematic diagram of a MOSFET with three floating P-type structures. Considering the limitation and cost of producing 4H-SiC SJ MOSFET via multiple epitaxy growth, the more floating P-type structures, the longer the process is. The depth and spacing of the three floating P-type structures are the same. The thickness of each epitaxial layer is 2 μm and the thickness of the total epitaxial layer is 30 μm . The concentrations of the three floating P-type structures are the same. The uppermost layer (the JEFT region) is the CSL, which can improve the current spreading ability when the device is turned on and reduce the parasitic JFET effect [14–16]. Figure 1c is DC-FSJ MOSFET. The thickness of the epitaxial layer is 26 μm , which enables the device to maintain a breakdown voltage greater than 3800 V and also reduce the $R_{on,sp}$. The epitaxial layer is divided into three layers; the top layer is CSL and the other epitaxial layers under the CSL are N1 and N2 epitaxial layers. The concentration of the N1 epitaxial layer is higher than that of the N2 epitaxial layer. The purpose of the N1 epitaxial layer is to achieve the charge compensation with the floating P-type structures [17–19]. In addition to maintaining the breakdown voltage of the MOSFET, it can also greatly reduce $R_{on,sp}$ of the device. In order to withstand most of the reverse voltage, the N2 epitaxial layer concentration is relatively lighter. The main differences between the three MOSFET structures are the floating P-type structures and the N1 epitaxial layer.

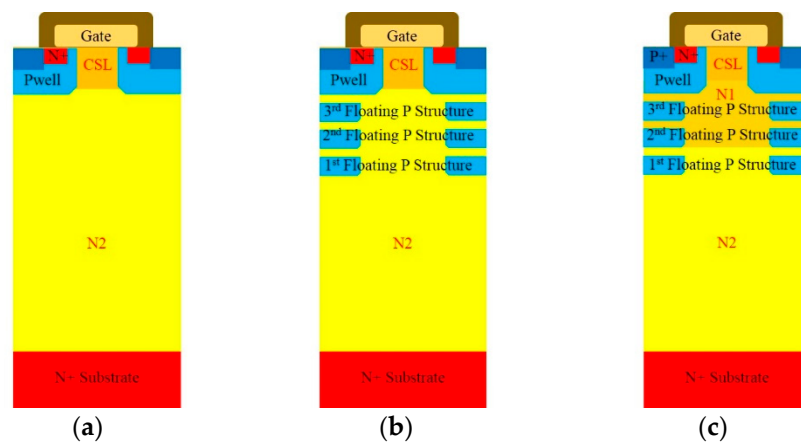


Figure 1. Three device structure schematic diagrams (a) traditional vertical MOSFET, (b) FSJ MOSFET, (c) DC-FSJ MOSFET.

3. Influence of Structure and Doping

3.1. Floating P-Type Structure Depth

For designing the depth of the P-type structure, the deepest floating P-type structure is investigated in the beginning. The simulation results show that the breakdown voltage of the MOSFET increases as the floating P-type structure becomes deeper in the epitaxial layer. By changing the depth of the floating P-type structure, the electric field extension is enhanced so that the breakdown voltage increases [20–22], as shown in Figure 2. However, when the depth of the floating P-type structure exceeds 8 μm , as seen from the vertical electric field distribution, the electric field along the PN region shown in Figure 3a and MOS region shown in Figure 3b becomes uneven, leading to the slightly increasing breakdown voltage; this is because the distance between the structure and the P-well is too long.

Considering the multiple epitaxial growth, the depth of the floating P-type structure, process time and alignment deviation, a depth of 6 μm and three P-type structures are chosen.

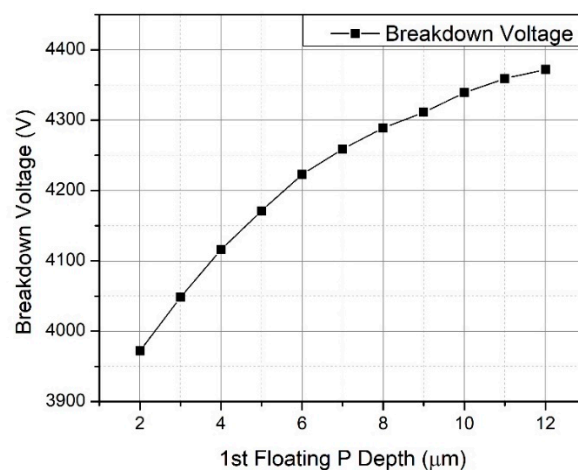
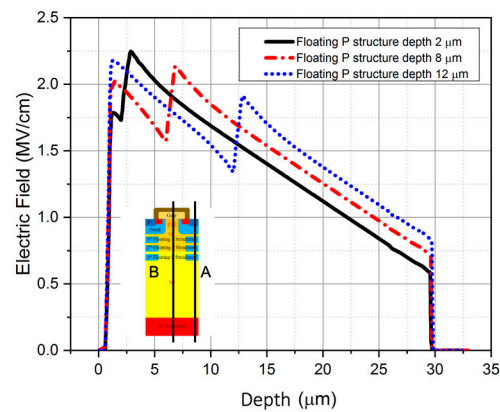
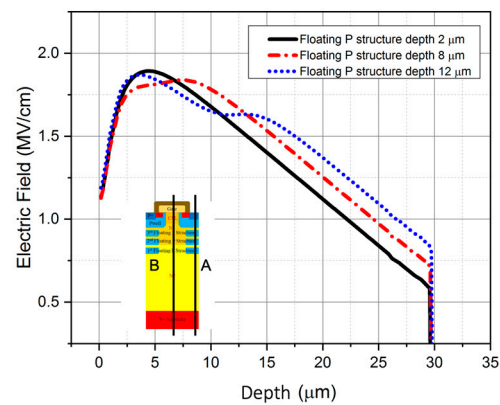


Figure 2. Relationship of different floating P-type structure depths and breakdown voltage.



(a)



(b)

Figure 3. The electric field distribution of different floating P-type structure depths (a) in the P-well region and the floating P-type structure area, (b) in the drift region of the MOSFET.

3.2. Concentration of N1 Epitaxial Layer

The concentration and thickness of the epitaxial layer N1 are the key points in the design of DC-FSJ MOSFET because the concentration directly affects the breakdown voltage and $R_{on,sp}$ of the device. The normalized N1 value of 1.0 means that the origin N1 concentration reaches the highest reverse breakdown and it is higher than the concentration of N2. Seen from Figure 4, when the N1 epitaxial layer concentration ratio exceeds 2, the $R_{on,sp}$ significantly decreases but the breakdown voltage dramatically drops. It can be seen from Figure 5 when the N1 epitaxial layer concentration is too high and cannot balance with the floating P-type concentration, the electric field will be crowded around the P-well area, causing the premature breakdown. As the N1 concentration fades, the electric field gradually concentrates at the bottom of the floating P-type structure. When the N1 epitaxial layer concentration and the floating P-type concentrations are compensated, the electric field is distributed more uniformly in the drift region.

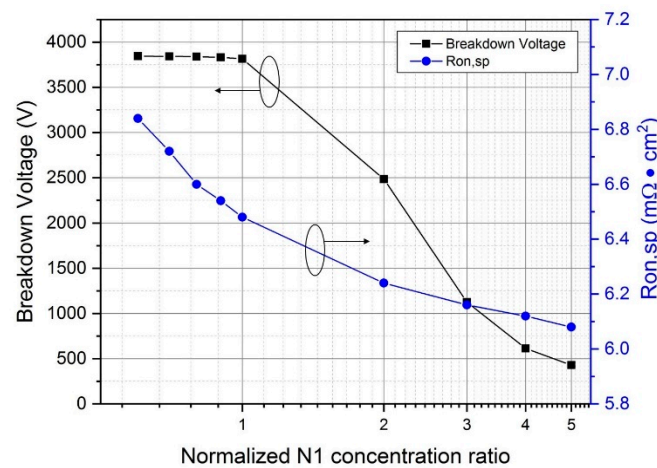


Figure 4. Relationship between different N1 epitaxial layer concentration ratios and the breakdown voltage and $R_{on,sp}$.

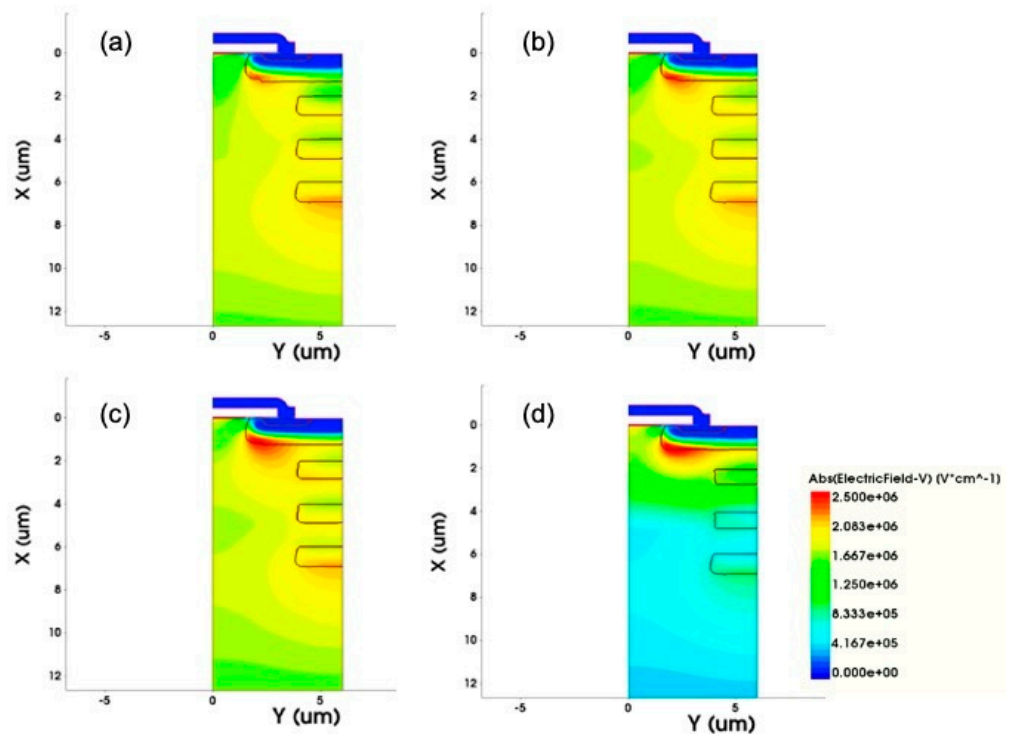


Figure 5. Electric field distributions of different N1 epitaxial layer concentrations: normalized N1 concentration ratio of (a) 0.6, (b) 0.8, (c) 1, (d) 3.

3.3. Thickness of N1 Epitaxial Layer

The thickness of the N1 epitaxial layer determines the relative position of the epitaxial layer boundary with respect to the floating P-type structure. From Figure 6, when the N1 epitaxial layer is thicker, the $R_{on,sp}$ decreases linearly. In addition, when the thickness is less than 4 μm , the bottom of the N1 epitaxial layer is slightly above the bottom of the second floating P-type structure, which will not greatly affect the breakdown voltage of the MOSFET. Instead, when the thickness is greater than 4 μm , the breakdown voltage will drop significantly. The main reason is when the bottom of the N1 epitaxial layer exceeds the bottom of the second floating P-type structure, the electric field between the first and second floating P-structures becomes discontinuous. Furthermore, the N2 epitaxial layer mainly relies on the first floating P-type structure to extend the electric field, which mainly determines the breakdown voltage of the device as shown in Figure 7. Therefore, the

thicker N1 epitaxial layer and the first floating P-type structure cannot evenly spread the electric field towards to the N2 epitaxial layer, leading to the lower breakdown voltage. Because of the thicker N1 epitaxial layer, the N-type concentration is greater than that of the P-type region, which means the electric field is easy to gather at the bottom of the P-well region. Therefore, a worse charge balance is achieved, and the breakdown voltage of the device decreases. Thus, when designing a DC-FSJ MOSFET, the thickness of the N1 epitaxial layer and the charge balance theory need to be considered together.

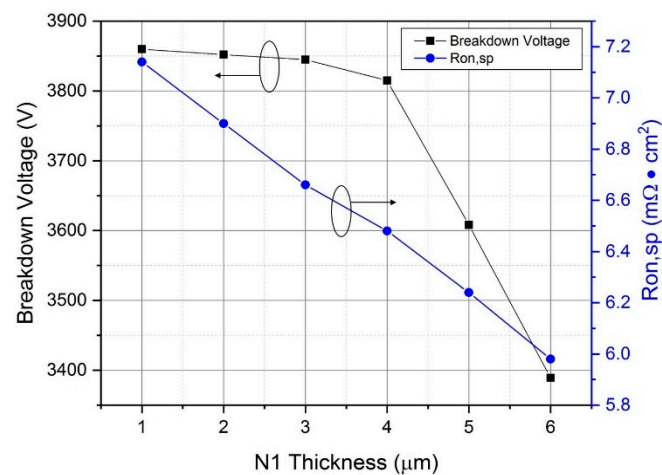


Figure 6. Relationship of different N1 epitaxial layer thicknesses and breakdown voltage and $R_{on,sp}$.

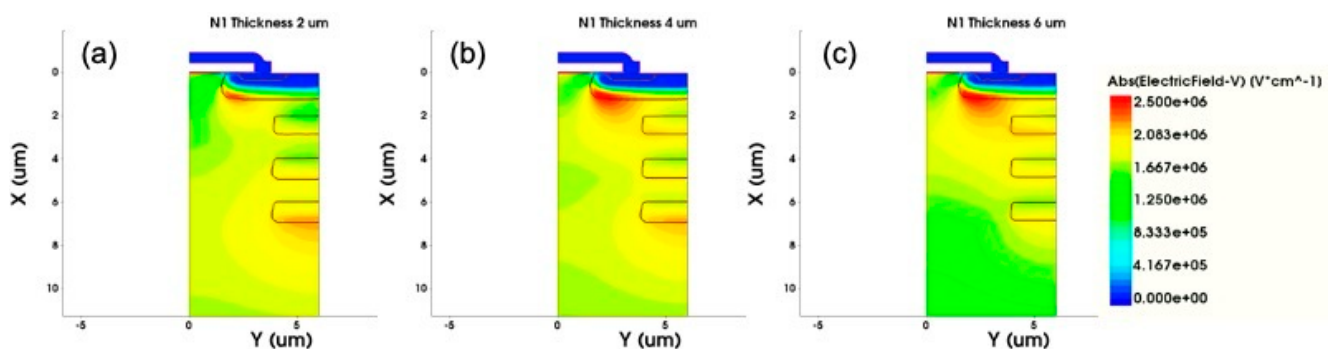


Figure 7. The electric field distribution diagrams of different N1 epitaxial layer thicknesses (a) 2 μm, (b) 4 μm, (c) 6 μm.

3.4. Floating P-Type Structures in the Different Epitaxial Layers in the Drift Region

A traditional power MOSFET that uses different concentrations of the epitaxial layers will cause the dramatic drop of the breakdown voltage, because the junction of the P-well structure and the high-concentration N1 epitaxial layer is prone to inducing the high electric field and then collapsing prematurely. The floating P-type structure compensates the N1 epitaxial layer concentration and spreads out the electric field evenly so that the device can reach a higher breakdown voltage, as shown in Figure 8.

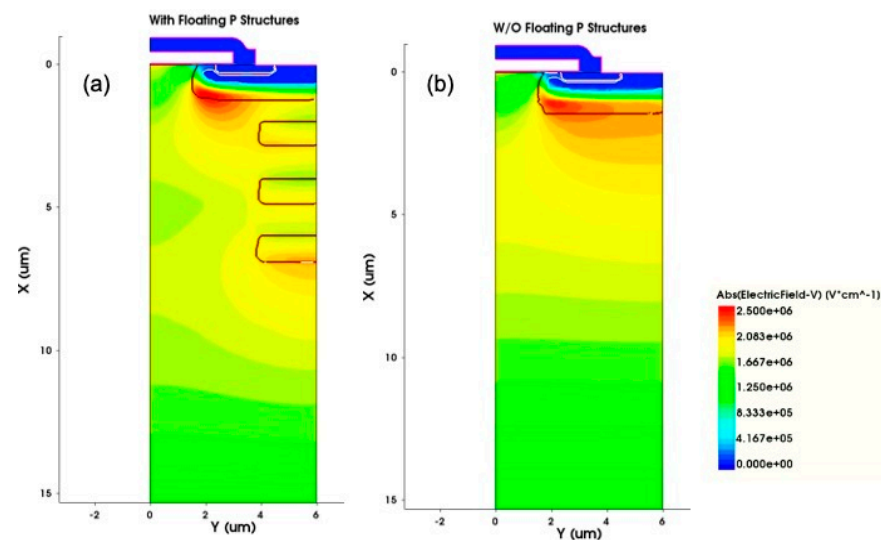


Figure 8. Comparison of the electric field distribution with and without the floating P-type structures (a) with floating P structures, (b) without floating P structures.

4. Comparison of Electrical Properties

According to the simulation results in Table 1, Figures 9 and 10, the reverse breakdown voltage of the traditional vertical MOSFET is 3912 V, and $R_{on,sp}$ is $8.66 \text{ m}\Omega\cdot\text{cm}^2$; the MOSFET with floating P-type structures can extend the electric field from the P-well region to the deeper area of the drift region and then increase the breakdown voltage. In this work, the breakdown voltage can be increased up to 4162 V. However, when the FSJ-MOSFET is in the forward conduction, due to the floating structures, the area that the current flows through is narrow and the $R_{on,sp}$ becomes the highest among these three structures (about $9.12 \text{ m}\Omega\cdot\text{cm}^2$). Therefore, the N1 epitaxial layer with the higher concentration is added to form DC-FSJ MOSFET. When reaching the charge balance, the DC-FSJ MOSFET can maintain a breakdown voltage of 3800 V and reduce the $R_{on,sp}$ to $6.5 \text{ m}\Omega\cdot\text{cm}^2$. The BFOM of DC-FSJ MOSFET increases by 27% compared with the traditional vertical MOSFET; and increases by 18% compared with the BFOM of the FSJ MOSFET. The N1 epitaxial layer of DC-FSJ MOSFET can reduce the area of depletion generated by the floating P-type structures in the forward bias and then reduce the current crowding in the JFET region. The uncertainty error on the floating P-type structures should be the precision of the depth and the concentration of the floating P-type structures. If the desired depth and concentration are not achieved, the breakdown voltage will be significantly reduced and the specific on-resistance will be increased.

Table 1. Comparison of the characteristics of the three MOSFET structures.

Parameter	Traditional	FSJ	DC-FSJ
Thickness (μm)	30	30	26
$R_{on,sp}$ ($\text{m}\Omega\cdot\text{cm}^2$)	8.66	9.12	6.5
BV (V)	3912	4162	3815
V_{th} (V)	3.13	3.35	3.29
BFOM (MW/cm^2)	1767	1899	2239

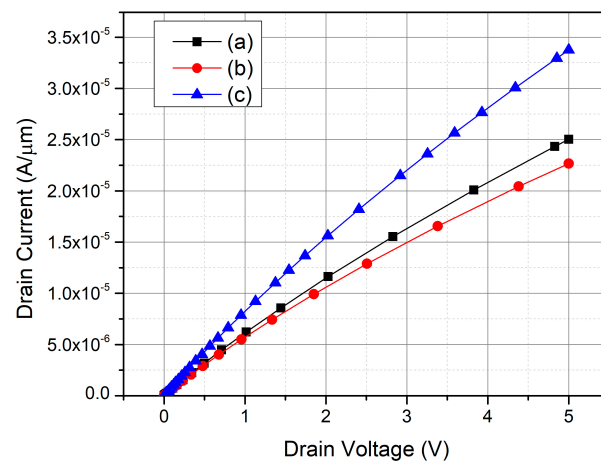


Figure 9. Forward I_d - V_d diagram of the three structures (a) traditional vertical MOSFET, (b) FSJ MOSFET, (c) DC-FSJ MOSFET.

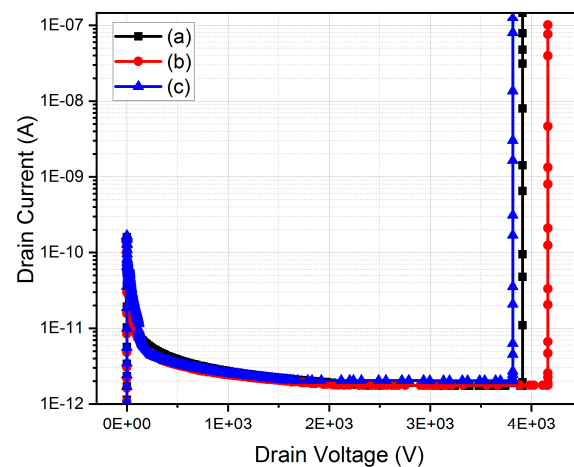


Figure 10. Reverse I_d - V_d diagram of the three structures (a) traditional vertical MOSFET, (b) FSJ MOSFET, (c) DC-FSJ MOSFET.

5. Conclusions

The proposed 3.3 kV 4H-SiC DC-FSJ MOSFET structure is formed by using the multiple epitaxial growth, floating P-type structures and the epitaxial layers with different concentrations. Not only can it reach the desired breakdown voltage but it also greatly reduces the $R_{on,sp}$. Under the same conditions, the BFOM of DC-FSJ MOSFET increases by 27% and 18% compared with the traditional vertical MOSFET and the FSJ MOSFET, respectively. The $R_{on,sp}$ also reduces by about 25% compared with the traditional vertical MOSFET.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Baliga, B.J. *Fundamentals of Power Semiconductor Devices*; Springer: New York, NY, USA, 2008.
2. Godignon, P.; Soler, V.; Cabello, M.; Montserrat, J.; Rebollo, J.; Knoll, L.; Bianda, E.; Mihaila, A. New Trends in High Voltage MOSFET Based on Wide Band Gap Materials. In Proceedings of the International Semiconductor Conference (CAS), Sinaia, Romania, 11–14 October 2017.
3. Millanv, J. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Trans. Power Electron.* **2013**, *29*, 2155–2163. [[CrossRef](#)]
4. Marckx, D.A. *Breakthrough in Power Electronics from SiC*; NREL/SR-500-38515; Nat. Renewable Energy Lab.: Golden, CO, USA, 2006.
5. León-Masich, A.; Valderrama-Blavi, H.; Bosque-Moncusí, J.M.; Martínez-Salamero, L. Efficiency comparison between Si and SiC-based implementations in a high gain DC-DC boost converter. *IET Power Electron.* **2015**, *8*, 869–878. [[CrossRef](#)]
6. Masuda, T.; Kosugi, R.; Hiyoshi, T. 0.97 mΩcm²/820 V 4H-SiC super junction V-groove trench MOSFET. In Proceedings of the European Conference on Silicon Carbide and Related Materials (ECSCRM), Thessaloniki, Greece, 10–14 May 2017; pp. 483–488.
7. Ueda, D.; Takagi, H.; Kano, G. A new vertical power MOSFET structure with extremely reduced on-resistance. *IEEE Trans Electron Devices* **1985**, *32*, 2–6. [[CrossRef](#)]
8. Palmour, J.W.; Cheng, L.; Pala, V.; Brunt, E.V.; Lichtenwalner, D.J.; Wang, G.-Y.; Richmond, J.; O’Loughlin, M.; Ryu, S.; Allen, S.T.; et al. Silicon Carbide Power MOSFETs: Breakthrough Performance from 900 V up to 15 kV. In Proceedings of the 26th International Symposium on Power Semiconductor Devices & IC’s, Waikoloa, HI, USA, 15–19 June 2014.
9. Matin, M.; Saha, A.; Cooper, J.A. A Selfn-Aligned Process for High-Voltage, Short-Channel Vertical DMOSFETs in 4H-SiC. *IEEE Trans. Electron Devices* **2004**, *51*, 1721–1725. [[CrossRef](#)]
10. Wang, S.R.; Cooper, J.A. Double-Self-Aligned Power DMOSFETs in 4H-SiC. In Proceedings of the Device Research Conference, University Park, PA, USA, 22–24 June 2009; pp. 277–278.
11. Cheng, L.; Ryu, S.H.; Jonas, C.; Dhar, S.; Callanan, R.; Richmond, J.; Agarwal, A.K.; Palmour, J. 3300V, 30A 4H-SiC Power DMOSFETs. In Proceedings of the International Semiconductor Device Research Symposium, College Park, MD, USA, 9–11 December 2009; pp. 1–2.
12. Bolotnikov, A.; Losee, P.; Matocha, K.; Glaser, J.; Nasadoski, J.; Wang, L.; Elasser, A.; Arthur, S.; Stum, Z.; Sandvik, P.; et al. 3.3 kV SiC MOSFETs Designed for Low On-Resistance and Fast Switching. In Proceedings of the ISPSD 2012, Bruges, Belgium, 3–7 June 2012; pp. 389–392.
13. Huang, X.; Vursin, L.; Bhalla, A.; Simon, W.; Dries, J.C. Design and fabrication of 3.3 KV SiC MOSFETs for industrial applications. In Proceedings of the ISPSD 2017, Sapporo, Japan, 28 May–1 June 2017; pp. 255–258.
14. Saha, A.; Cooper, J.A. A 1-kV 4H-SiC power DMOSFET optimized for low on-resistance. *IEEE Trans. Electron. Devices* **2007**, *54*, 2786–2791. [[CrossRef](#)]
15. Zhou, X.; Yue, R.; Dai, G.; Li, J.; Wang, Y. An improved structure to enhance the robustness of SiC power MOSFETs for a low Ron, sp. In Proceedings of the IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, China, 3–5 August 2016.
16. Shi, S.; Zhou, X.; Yue, R.; Wang, Y. An improved structure of 3.3kV 4H-SiC VDMOSFETs with lower on-resistance and reverse transfer capacitance. In Proceedings of the 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Hangzhou, China, 25–28 October 2016.
17. Liu, T.; Hu, S.; Wang, J.; Guo, G.; Luo, J.; Wang, Y.; Guo, J.; Huo, Y. An Investigation of Electric Field and Breakdown Voltage Models for a Deep Trench Superjunction SiC VDMOS. *IEEE Access* **2019**, *7*, 145118–145123. [[CrossRef](#)]
18. Qian, Q.; Sun, W.; Zhu, J.; Liu, S. A novel charge-imbalance termination for trench superjunction VDMOS. *IEEE Electron Device Lett.* **2010**, *31*, 1434–1436. [[CrossRef](#)]
19. Hu, S.; Huang, Y.; Liu, T.; Guo, J.; Wang, J.; Luo, J. A comparative study of a deep-trench superjunction SiC VDMOS device. *Comput. J. Electron.* **2019**, *18*, 553–560. [[CrossRef](#)]
20. Qingwen, S.; Xiaoyan, T.; Yimeng, Z.; Yuming, Z.; Yimen, Z. Investigation of SiC trench MOSFET with floating islands. *IET Power Electron.* **2016**, *9*, 2492–2499. [[CrossRef](#)]
21. Vaid, R.; Padha, N. A novel trench gate floating islands power MOSFET (TG-FLIMOSFET): Two-dimensional simulation study. *Microelectron. Eng.* **2011**, *88*, 3316–3326. [[CrossRef](#)]
22. Baliga, B.J. *Advanced Power MOSFET Concepts*; Springer: New York, NY, USA, 2010.
23. Scognamiglio, C.; Catalano, A.P.; Lasserre, P.; Duchesne, C.; d’Alessandro, V.; Castellazzi, A. Combined experimental-FEM investigation of electrical ruggedness in double-sided cooled power modules. *Microelectron. Reliab.* **2020**, *114*, 113742. [[CrossRef](#)]