



# Enhanced and continuous electrostatic carrier doping on the SrTiO<sub>3</sub> surface

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**Paraelectrical tuning of a charge carrier density as high as  $10^{13} \text{ cm}^{-2}$  in the presence of a high electronic carrier mobility on the delicate surfaces of correlated oxides, is a key to the technological breakthrough of a field effect transistor (FET) utilising the metal-nonmetal transition. Here we introduce the Parylene-C/Ta<sub>2</sub>O<sub>5</sub> hybrid gate insulator and fabricate FET devices on single-crystalline SrTiO<sub>3</sub>, which has been regarded as a bedrock material for oxide electronics. The gate insulator accumulates up to  $\sim 10^{13} \text{ cm}^{-2}$  carriers, while the field-effect mobility is kept at  $10 \text{ cm}^2/\text{Vs}$  even at room temperature. Further to the exceptional performance of our devices, the enhanced compatibility of high carrier density and high mobility revealed the mechanism for the long standing puzzle of the distribution of electrostatically doped carriers on the surface of SrTiO<sub>3</sub>. Namely, the formation and continuous evolution of field domains and current filaments.**

A prominent feature of phase transitions in correlated electron systems is the nanoscale dynamics leading to future electronics such as switching devices and novel nonvolatile resistance-change memory applications<sup>1–9</sup>. In spite of the long-standing research, device prototypes remain limited mainly due to the absence of a method for a continuous (*i.e.*, paraelectrical) and precise electrostatic control (gating) of a two dimensional (2D) charge carrier density  $\gtrsim 10^{13} \text{ cm}^{-2}$ . Furthermore, oxygen and cation stoichiometry are fairly unstable in perovskite-type (ABO<sub>3</sub>) transition-metal oxides (TMOs)<sup>10</sup>. Deposition of dielectric oxides on the surface of ABO<sub>3</sub> channel for gating inevitably results in such kind of defects, introducing randomness and eventually smearing the critical features of metal-insulator transitions<sup>11</sup>. In the face of these challenges, we have chosen to fabricate FET adopting single-crystalline SrTiO<sub>3</sub> for the channel. This compound is a band insulator with a crystal structure characteristic of many TMO Mott insulators, and becomes metallic by electron doping. SrTiO<sub>3</sub> is an n-type wide-gap semiconductor with a band gap of 3.2 eV. It is considered as a matrix for spintronic devices due to the unique configuration of the spin-precession vector at the surface and the absence of the Dresselhaus term. The surface of the single crystal can be atomically flat and is widely used as a substrate for correlated TMO thin films, making it preferable candidate to test the suitability of the reported gate insulator for future electronics. Identifying the technical methods and physical mechanism for paraelectric tuning of electronic conduction in two dimensional electron gases (2DEG) created at the surface of SrTiO<sub>3</sub> is a problem of bursting interdisciplinary interest<sup>12</sup>.

High-density charge accumulation  $\sim 10^{15} \text{ cm}^{-2}$  was recently realised<sup>13</sup> through an electric double-layer (EDL) on the surface of electrolytes such as ionic liquids. Although the gating with EDL is a promising method for future correlated electron devices, its viability is hindered, because ionic liquids on the surface of TMOs may trigger redox reactions, causing vacancies at the interface especially in the presence of high electric fields<sup>14,15</sup>. In addition, the continuous control of the carrier density with EDL can be done only by using liquid electrolytes, which are unsuitable for integration to the present solid-state electronics.

Here, we have engineered a bilayer of poly-monochloro-*para*-xylylene (known as Parylene-C)<sup>16</sup> with Ta<sub>2</sub>O<sub>5</sub>, Fig. 1. Ta<sub>2</sub>O<sub>5</sub> has a high dielectric constant  $\epsilon = 25$  and a relatively high dielectric strength  $\sim 4 \text{ MV/cm}^{17}$ . The combination of Ta<sub>2</sub>O<sub>5</sub> and Parylene-C into a single gate insulator enabled a sheet carrier density of  $\sim 10^{13} \text{ cm}^{-2}$  while keeping the field effect mobility of the SrTiO<sub>3</sub> surface at  $\sim 10 \text{ cm}^2/\text{Vs}$ . Fabrication details can be found in the Methods Summary. The electronic transport measurements were performed using an Agilent 4155C semiconductor parameter analyser.

## Results

Fig. 1(c) shows the gate leak currents plotted against the sheet carrier density for the bilayer gate insulator and for the single Parylene-C gate insulator. Although the total thickness of the bilayer gate insulator is 10 times thinner

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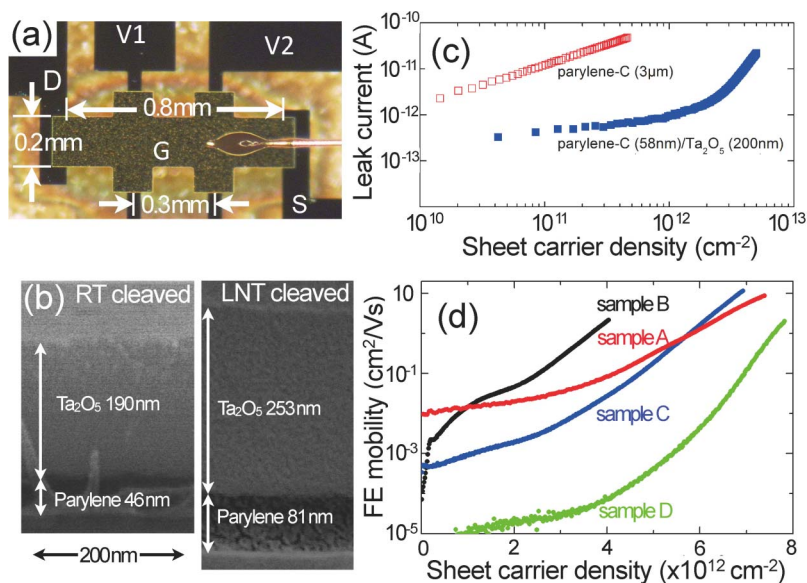
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**Figure 1** | (a) Photograph of a typical FET structure fabricated on the top of a (100) surface of a single-crystalline SrTiO<sub>3</sub>. Gate (G), source (S), drain (D) electrodes and four other potential probes such as V<sub>1</sub> and V<sub>2</sub> are indicated. A gold wire of 25 μm diameter is attached by conducting gold paint (Silvest 8560-1A, Tokuriki Chemicals). (b) Scanning electron microscopy images of the cross sections of the bilayer gate insulator. The sample was cleaved at room temperature (left) and at liquid N<sub>2</sub> temperature (right). See Methods Summary for details. (c) Gate leak current plotted against the sheet carrier density for the bilayer gate insulator with 200 nm Ta<sub>2</sub>O<sub>5</sub> deposited on the top of 48 nm Parylene-C (blue opaque square) and for the single layer gate insulator of 3 μm Parylene-C (red transparent square). (d) Field-effect (FE) mobility plotted against the sheet carrier density for samples A, B, C, and D with different Parylene-C thickness as summarised in Table 1.

than the 3 μm-thick Parylene-C, the leak current of the bilayer is an order of magnitude lower, which is similar to the trend reported earlier<sup>18</sup>. Hence, the sputtering deposition of Ta<sub>2</sub>O<sub>5</sub> does not damage the Parylene-C thin film. Fig. 1(d) depicts an upturn in the increase of the field effect mobility at sheet carrier densities 2–4 × 10<sup>12</sup> cm<sup>-2</sup>.

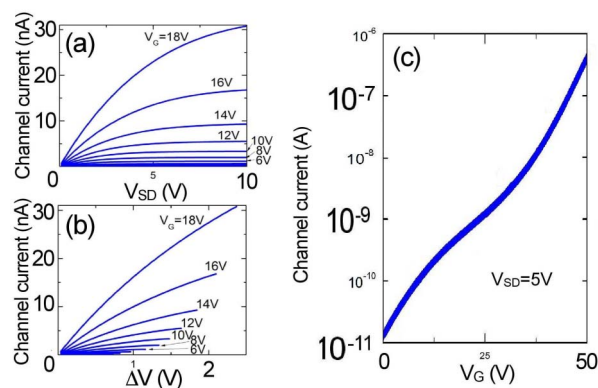
The field effect mobility is defined as  $\mu_{FE} = \frac{1}{e} \frac{d\sigma_{sq}}{dn_{sq}}$ , where  $\sigma_{sq} \equiv (I_{SD}/W)/(\Delta V/L_o)$  is the sheet conductance and  $n_{sq} \equiv C_{sq}(V_G - V_{th})/e$  is the nominal sheet carrier density in the channel region.  $I_{SD}$  is the channel current,  $L_o$  (and  $\Delta V$ ) is the distance (and voltage difference) between channel electrodes V<sub>2</sub> and V<sub>1</sub>,  $W$  is the channel width,  $C_{sq}$  is the measured total capacitance per unit area, and  $e$  is the elementary charge. Although  $I_{SD}$  increased almost exponentially with the application of  $V_G$ , the  $I_{SD}$ - $V_G$  behaviour is different from that in the conventional subthreshold regime. In fact, all our samples showed extremely large  $\mu_{FE}$ , ~10 cm<sup>2</sup>/Vs at large carrier densities (*i.e.*, large  $V_G$ ) without reaching saturation even at room temperature. Thus, we set the threshold voltage  $V_{th} = 0$ . Notably,  $\mu_{FE}$  is an order of magnitude larger than earlier reports for a Parylene-C/SrTiO<sub>3</sub> FET at room temperature ( $\mu_{FE} = 0.3$  cm<sup>2</sup>/Vs for  $n_{sq} = 3 \times 10^{12}$  cm<sup>-2</sup>)<sup>19</sup>, and comparable to the bulk Hall mobility of SrTiO<sub>3</sub><sup>20</sup>.

The typical  $I_{SD}$ - $V_{SD}$  characteristics of Sample B in Fig. 2(a) indicate that the current saturates for large  $V_{SD}$  as in conventional semiconductor FETs, where it occurs due to the pinch-off of the channel. The saturation vanishes when the channel current in Fig. 2(a) is plotted against the voltage drop inside the channel  $\Delta V$ , Fig. 2(b). Hence, the pinch-off region is rather small even at low  $V_G$  and emerges between the drain and the V<sub>2</sub> electrode for  $V_{SD}$  below 5V. Fig. 2(c) shows that the current increases monotonically from ~1 nA to ~100 μA as the gate voltage increases up to 40 V, thereby demonstrating a continuous electrostatic control of the sheet carrier density.

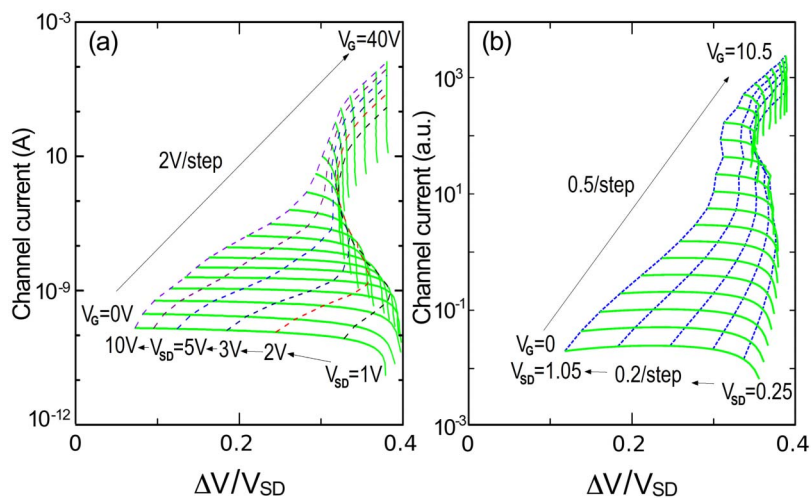
Furthermore, for small fixed values of  $V_G$ , although the channel current does not change very much (Fig. 3(a)), the ratio  $\Delta V/V_{SD}$  decreases rapidly with increasing  $V_{SD}$ . This feature can be associated with the formation of field domains<sup>21</sup>. We also observe that in various parameter conditions,  $\Delta V/V_{SD}$  approaches the geometrical value

~0.37 = (V<sub>1</sub>-V<sub>2</sub> distance 295 μm)/(source-drain distance 800 μm). This indicates that in those regimes the contact resistance between SrTiO<sub>3</sub> and Al electrodes, which is expected to be ohmic, is indeed negligibly small compared to the channel resistance of SrTiO<sub>3</sub>. It is interesting, however, to observe the behaviour of  $\Delta V/V_{SD}$  with increasing  $V_G$  and with fixed (small) value of  $V_{SD}$  in Fig. 3(a). This feature is the so-called S-type negative differential resistivity (SNDR) associated with the formation of current filaments<sup>21</sup>.

The rather complicated behaviour of the  $I_{SD}$  vs  $(\Delta V/V_{SD})$  curves in Fig. 3(a) was qualitatively reproduced (Fig. 3(b)) by a model calculation based on the following assumptions: (i) the existence of a low  $V_G$  regime where charge carriers are mainly spatially and inhomogeneously confined in cells, and move through the channel region by incoherent tunnelling, (ii) a higher  $V_G$  regime where the conductive cells overlap and percolating conduction paths are formed, and (iii) a



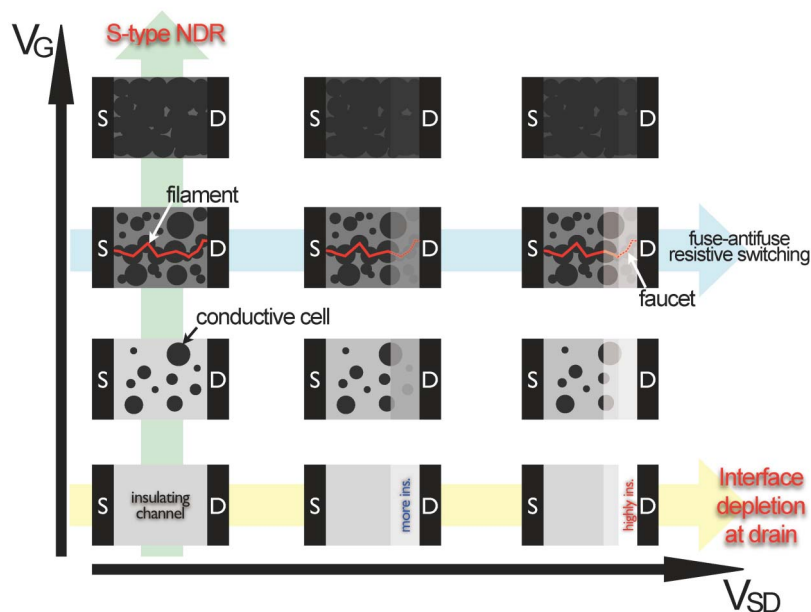
**Figure 2** | (a) Channel current of Sample B plotted against the source-drain voltage  $V_{SD}$  for the different values of the applied gate voltage  $V_G$ . (b) Same as (a) but the horizontal axis is the voltage difference  $\Delta V$  between V<sub>2</sub> and V<sub>1</sub> electrodes. (c) Channel current of Sample C plotted against  $V_G$  for  $V_{SD} = 5$  V.



**Figure 3** | (a) Channel current of Sample C plotted against  $\Delta V/V_{SD}$ .  $V_{SD}$  is swept from 0 to 10 V for the different values of  $V_G$  as shown in the thick green lines. The dashed lines indicate the  $V_{SD}$  contour, in which SNDR is seen for low  $V_{SD}$  and vanishes with increasing  $V_{SD}$ . (b) The results of numerical simulations. The voltages are expressed in arbitrary units. See Supplementary Materials for details.

well developed homogeneous 2DEG with barriers formed at the interfaces. We modelled the experimental system through a 2D resistor network array where the transport properties of each cell is determined primarily by the local electron density. The cells are assumed to be randomly distributed shallow potential wells for carriers with a site dependent potential strength  $\psi_{dis}(r)$ . At low  $V_G$  and  $V_{SD}$ , the cells have low density and the carriers are confined. The carriers move between cells by a variable range hopping (VRH) mechanism. At higher applied voltages, the occupation of cells increases and the carriers delocalise, augmenting their mobility. For given external potentials  $V_G$  and  $V_{SD}$ , we solve for the resistor network and compute the local voltages at all cells along the 2D

channel. These local voltages are then compared to the corresponding values of the local confining potential of the cell  $\psi_{dis}(r)$ . If their difference is negative, the mobility is assumed to be the VRH type, whereas if it is positive, we adopt a much larger value, consistent with a band-like conduction in the metallic state. The interfaces at the source and drain electrodes are simply modelled as barriers with potential height  $\psi_b$ . The details of the model and the numerical study are presented in the Supplementary Materials. Our numerical study captures the qualitative transport behaviour shown in Fig. 3, providing new insight to the conduction states of 2DEGs in SrTiO<sub>3</sub>. In fact, it demonstrates that the system evolves through a variety of regimes connected through crossovers depicted schematically in Fig. 4.



**Figure 4** | Schematic pictures of the evolution of conductive cells in the channel as demonstrated in Fig. 3. For increasing  $V_G$ , the channel varies from insulator to relatively good metal as the size of the conductive cells increases and a percolating current filament is formed. This represents SNDR. Meanwhile, for increasing  $V_{SD}$ , the region near the drain electrode is pinched off. By controlling the two parameters  $V_{SD}$  and  $V_G$ , we can realise the formation and continuous evolution of field domains and current filaments; *i.e.*, the competition of SNDR and the interface depletion at drain, which is not only the main topic of the research for the resistance change memory<sup>9</sup> but also a common problem associated to the future oxide electronics. The filament can be ruptured by the Joule-heating at the interface to the metal electrode (called faucet<sup>27</sup>); one of the widely accepted models of the non-volatile resistance change (fuse-antifuse resistive switching<sup>9</sup>).



**Table 1 | Parylene-C thickness of the four different samples reported in this work. The values of thickness were estimated from the measured values of capacitance of the bilayer gate insulators**

Sample	Amount of raw material (mg)	Bilayer capacitance per area (nF/cm <sup>2</sup> )	Estimated Parylene-C thickness (nm)
A	300	34	57.7
B	350	24.97	87.9
C	400	22.25	101.7
D	600	12.56	199.9

## Discussion

In summary, we have demonstrated that the Parylene-C/Ta<sub>2</sub>O<sub>5</sub> bilayer overcomes previous limitations, achieving the required large electrostatic carrier doping, while keeping a high quality interface with the TMO. The hybrid gate insulator can sustain a sheet carrier density of  $8 \times 10^{12} \text{ cm}^{-2}$ , without introducing formidable damage to the channel interface, as the field-effect mobility of SrTiO<sub>3</sub> exceeds  $10 \text{ cm}^2/\text{Vs}$ , even at room temperature. The excellent agreement of our numerical study with measurements on the hybrid gate insulator, indicate a continuous evolution through a variety of different regimes, including tuneability of field domains and current filaments on the surface of SrTiO<sub>3</sub>. Our findings provide a novel method for paraelectric tuning of metal-nonmetal transitions in correlated electron devices made of ABO<sub>3</sub>-type TMOs. Notably, the fabrication details and physical mechanism reported here may be applied towards emergent oxide electronics controlled by low dimensional charge carrier transport.

Further to the practical interest, low temperature studies on similar devices would reveal whether granular superconductivity<sup>22</sup> in SrTiO<sub>3</sub> could be realised for small  $V_G$  and  $V_{SD}$ . Indeed, the behaviour of possible superconducting cells with dimensions comparable to characteristic length scales may be considerably different from bulk materials. Moreover, the quantum confinement in the cells may lift the degeneracy of the lowest energy band of SrTiO<sub>3</sub>, affecting the Rashba effect on its surface<sup>23</sup>.

## Methods

Preparation of Parylene-C thin film was performed as follows. In a  $\phi 46 \text{ mm}$  quartz tube, di-monochloro-*para*-xylylene was sublimated at  $150^\circ\text{C}$ , the dimer flew into a high temperature ( $800^\circ\text{C}$ ) region<sup>24</sup>, where it was cleaved into two monomer units<sup>16</sup>. The reactive intermediates were then transported to a room temperature deposition chamber at the pressure of  $2 \times 10^{-4} \text{ Pa}$ . Upon condensation on the surface of single-crystalline SrTiO<sub>3</sub>, spontaneous polymerisation into Parylene-C took place. The Parylene-C thin film deposited through this so-called Gorham method<sup>16</sup> provides excellent conformal coating on the SrTiO<sub>3</sub> surface. The thin film of Ta<sub>2</sub>O<sub>5</sub> was deposited directly on the top of the Parylene-C by radio frequency (rf) sputtering at room temperature. We used a Ta<sub>2</sub>O<sub>5</sub> ceramic target in a flowing Ar gas of 25 sccm and 5.5 Pa. The rf power was  $2 \text{ W/inch}^2$ , and the sample-target distance was 140 mm. The thickness of the Ta<sub>2</sub>O<sub>5</sub> layer was  $\sim 200 \text{ nm}$  measured by a surface profiler (KLA Tencor). On the top of Ta<sub>2</sub>O<sub>5</sub>, a 150 nm thick Au gate electrode with a 5 nm Ti adhesion layer was deposited by electron-beam deposition. The thickness of the Parylene-C layer was estimated from the measured capacitance of a built-in capacitor (of area  $800 \times 800 \mu\text{m}^2$ ), using the known values  $\epsilon = 3.2$  for Parylene-C, and  $\epsilon = 25$  for Ta<sub>2</sub>O<sub>5</sub>.

We used the Al metal for source and drain electrodes; Al gives ohmic contact to SrTiO<sub>3</sub>. For the other parts of the device fabrication process, we followed the same method and used the same materials as reported by Nakamura *et al.*<sup>25</sup>.

For some samples, the thickness of the gate insulator was also measured by an S-4800 (Hitachi High-Tech) scanning electron microscope (SEM); the values were in good agreement with those estimated from the capacitance. Since the Parylene-C is much softer than Ta<sub>2</sub>O<sub>5</sub>, when we tried to expose the cross sections for the SEM measurement, either cutting with a scalpel or simply cleaving, the bilayer at room temperature easily deformed (stretches and shrinks at the ends) the Parylene-C layer, and the fibrils of Parylene-C always extended out of the cross section. We found that freezing the samples in liquid N<sub>2</sub> facilitates the cleaving.

Fig. 1 (b) shows the comparison of the cross section of a sample cleaved at room-temperature and one at liquid-N<sub>2</sub> temperature. The Parylene-C cross section in the latter case appears rather lumpy. However, this was never observed in the cross sections of the samples cleaved at room-temperature; thus, it is likely that the uneven cross section is due to the steep rise of temperature with heavy bedewing in air after

the cleavage in liquid-N<sub>2</sub>. It has been shown that a conventionally deposited planar Parylene-C thin film<sup>16</sup> does not possess nanostructured morphology<sup>26</sup>.

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## Author contributions

I.H.I. and C.P. conceived and supervised the project. A.B.E. fabricated the devices and performed all the measurements. I.H.I. contributed to the experimental setup. P.S. and M.J.R. did the numerical simulation study. All the authors discussed the results and cowrote the manuscript.



## Additional information

Supplementary information accompanies this paper at <http://www.nature.com/scientificreports>

**Competing financial interests:** The authors declare no competing financial interests.

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