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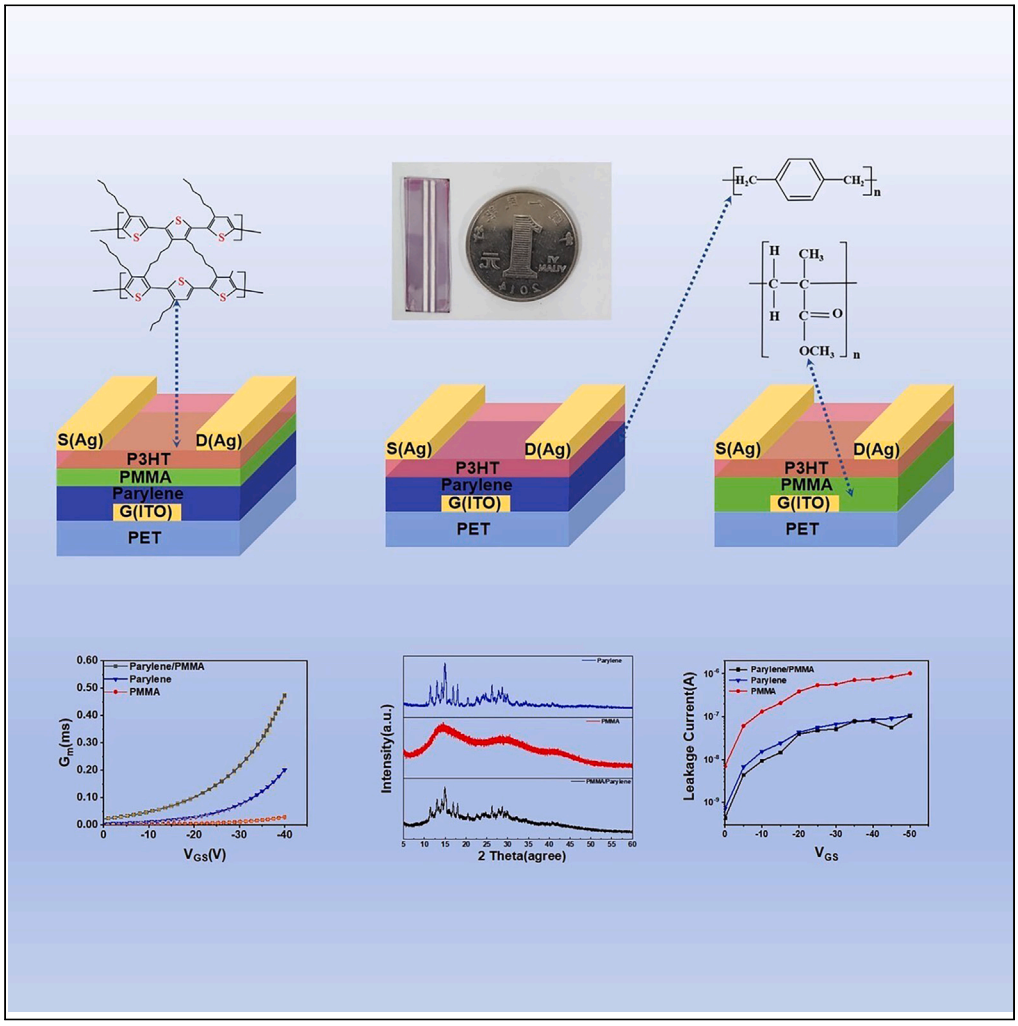

Shengbo Sang, Leilei Li, Qiang Li, ..., Raza Ullan, Jianan Ma, Jianlong Ji

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Highlights

Novel bilayer dielectric structure for P3HT-OFET

Optimized thickness of the insulating film

Parylene/PMMA dual insulating layers achieve excellent electrical performance

Provide guidance for further optimization of OTFT performance

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A high-performance organic thin-film transistor with Parylene/PMMA bilayer insulation based on P3HT

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SUMMARY

This work introduces a pioneering approach in the development of organic thin-film transistors (OTFTs), featuring a double-layer dielectric structure that combines poly(*para*-xylylene)s (Parylene) and poly(methyl methacrylate) (PMMA) to leverage the high insulation properties and high surface polarity of Parylene with the low insulation properties and low surface polarity of PMMA. This combination results in devices that showcase significantly enhanced electrical performance, including superior charge carrier mobility, increased current on/off ratios, and greater transconductance. Utilizing poly(3-hexylthiophene) (P3HT) for the active layer, the study demonstrates the advantage of the dual dielectric layers in minimizing hysteresis in the transfer curve, thereby facilitating the systematic growth of the organic active layer and enhancing electrical conductivity over single-layer alternatives. The superior performance of the Parylene/PMMA double-layer insulating structure opens new avenues for the advancement of organic electronics, presenting methodologies for performance optimization and expanding the application spectrum of OTFTs.

INTRODUCTION

Poly(3-hexylthiophene) has been commonly used as a soluble conjugated polymer in the active layer of organic field-effect transistors in recent decades.[1–6] However, the regularity of π-π stacking and molecular weight enhancement within P3HT is limited as an active layer.[7] The final performance of OTFTs depends not only on the intrinsic properties of each functional component but also on various other factors such as the growth mode of the active layer,[8] molecular order-orientation,[9] grain boundaries,[10] and grain size.[11] Furthermore, the carrier mobility and device performance are substantially affected by the semiconductor/insulator interface, which is a critical factor.[12] This is because the carrier mobility and device performance rely on the semiconductor/insulator interface, which is a significant factor.[13–16]

To achieve optimal charge carrier transport and device performance, it is crucial that the engineering of the insulator/semiconductor interface prioritizes a low density of charge traps and good contact compatibility.[12–14,17] Low-k organic dielectric materials are preferred over high-k dielectrics such as SiO_2/Si, as they have fewer charge traps leading to improved transistor mobility and performance.[18] For example, Zhu investigated the separated interfacial charges of Al_2O_3/AlN and AlGaN/GaN in his paper.[19] Son conducted a study on the fixed charges at the insulator/semiconductor interface of Al_2O_3 or AlTiO dielectrics in AlGaN/GaN MIS devices.[20] Biswas employed frequency-variable conductance measurements to investigate the trap states at the AlInGaN/GaN interface.[21] The use of low-k PMMA as an insulating layer has been conventionally reported for P3HT thin-film transistors.[22–24] However, when utilizing a sole layer of PMMA as the gate dielectric, OTFT currents are not suitably regulated due to the poor insulating properties of PMMA.[25,26]

PMMA is a dielectric with low surface polarity and low insulation properties. High-performance organic field-effect transistors require a dielectric with low surface polarity and high insulation properties, but it is challenging to achieve both properties in a single-layer dielectric.[27–32] To solve the problem, a double-layer gate dielectric was utilized, which included a low-surface-polarity dielectric in contact with the active layer and a high-k insulating layer underneath. This improved the performance of OTFTs by better controlling the interfacial properties, despite the increase in the total dielectric thickness.[33,35] For instance, M. Yi fabricated high-performance field-effect transistors using PMMA and crosslinked poly(4-vinylphenol) (PVP) for a double insulating layer.[33] Meanwhile, Nakamura developed high-performance field-effect transistors with SiN as the upper layer and HfO_2, La_2O_3, $LaLuO_3$, or TiO_2 as the lower layer for double-insulator transistors.[32] Both methods hold various merit for practical applications. Belkacemi examined the electrical properties of HfO_2/Si_3N_4 as a dual insulator.[33]

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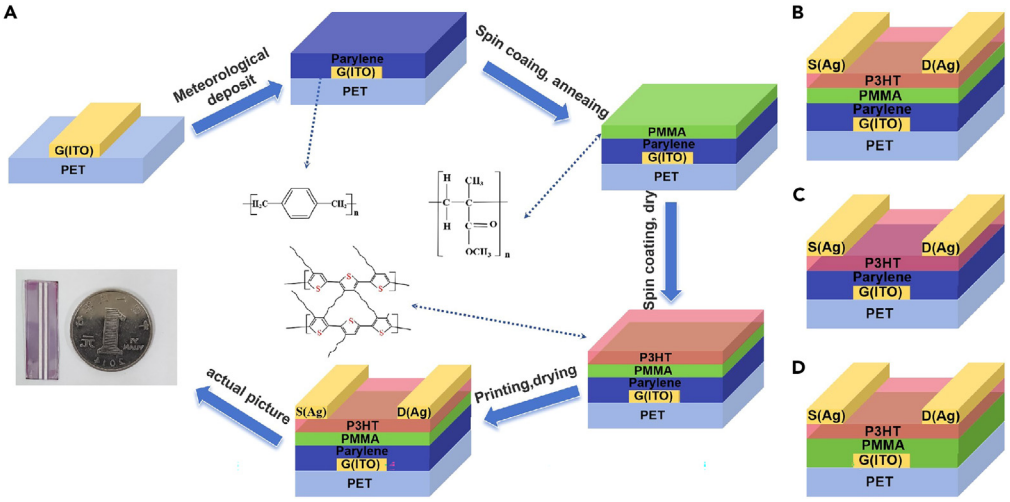

Figure 1. Preparation of high performance organic thin film transistor

(A) Preparation process flow chart.

(B-D) Cross-section of three different organic thin film transistors.

Parylene serves as a widely utilized dielectric layer, showcasing remarkable electrical and insulating properties.[34–37] However, using a single layer of Parylene film as a gate dielectric introduces a challenge—its surface displays a higher root-mean-square roughness. This impedes the crystalline growth of semiconductor molecules and raises the interface trap density.[38–44] Consequently, the diffusion of organic semiconductor molecules is hindered, leading to a decrease in grain boundaries and crystallinity within the organic semiconductor film.[45–47] Additionally, this situation may result in polarization effects and interface charge capture, adversely affecting device performance. Nonetheless, a clever solution lies in combining Parylene with a low surface polarity dielectric to create a dual-layer gate dielectric.[48–51] This optimized dual-layer structure effectively addresses the aforementioned issues, ultimately improving the performance of organic semiconductor devices. Therefore, the combination of Parylene/PMMA bilayer films not only integrates the excellent electrical insulation properties of Parylene with the low surface roughness of PMMA, but also ensures a smoother surface for the active layer, which is crucial for the development of high-quality semiconductor films. This combination leads to the fabrication of devices with superior performance. Moreover, the sequential deposition process, involving chemical vapor deposition (CVD) of Parylene followed by spin coating of PMMA, allows for precise control of interface properties, further enhancing the overall device performance.

This paper describes the design and application of a bilayer polymer dielectric composed of PMMA and Parylene with a low surface polarity and high insulation properties. The dielectric was employed to fabricate a bottom gate top contact field-effect transistor based on a P3HT semiconductor polymer. The surface and dielectric characteristics of bilayers made up of Parylene and PMMA, and of Parylene monolayers and PMMA monolayers, were researched. The findings reveal that the Parylene/PMMA bilayer film has a smooth and uniform surface with low polarity, low surface energy, and excellent solvent resistance. The bilayer film demonstrates high capacitance and low drain current. Meanwhile, compared to devices using a PMMA monolayer film, thin-film transistors prepared with a Parylene/PMMA bilayer film exhibit a higher current on/off ratio. This results in a significantly improved overall device performance. The active layer's growth is more orderly when using a bilayer structure, which has a smoother surface and lower surface polarity than a device prepared with a Parylene single-layer film. Also, the PMMA layer's thickness reduction promotes the accumulation of charge, causing more carriers to appear in the channel area. As a consequence, a larger on current is formed.

RESULTS AND DISCUSSION

In this study, the schematic diagram of an OTFTs with a Parylene/PMMA bilayer film as the dielectric layer, along with its preparation procedure and physical diagram, is depicted in Figure 1.

As illustrated in Figure 1A, the fabrication process of OTFTs with a bilayer insulating structure is depicted, with Figure 1B showing the cross-section of the Parylene/PMMA bilayer, Figure 1C for Parylene as the sole insulating layer, and Figure 1D for PMMA as the insulating layer. In this study, high-performance OTFTs were fabricated using a bilayer structure composed of Parylene and PMMA. Parylene, serving as the bottom dielectric material with a thickness of approximately 629 nm (refer to Figure S1), plays a pivotal role in the OTFTs due to its high molecular weight and crystallinity, which impart superior insulating properties.[52,53] It effectively reduces dielectric loss and enhances insulation strength, ensuring device reliability and stability under high electric fields. The Parylene layer, formed on the substrate via vapor deposition, creates a pinhole-free uniform film, laying the foundation for the subsequent spin-coating of the PMMA layer and the P3HT active layer.[54–56] The PMMA layer, approximately 100nm thick, is coated over Parylene. Its low surface energy characteristic optimizes the interface with the P3HT active layer, facilitating the orderly arrangement and improvement of P3HT crystal quality, crucial for reducing interface traps

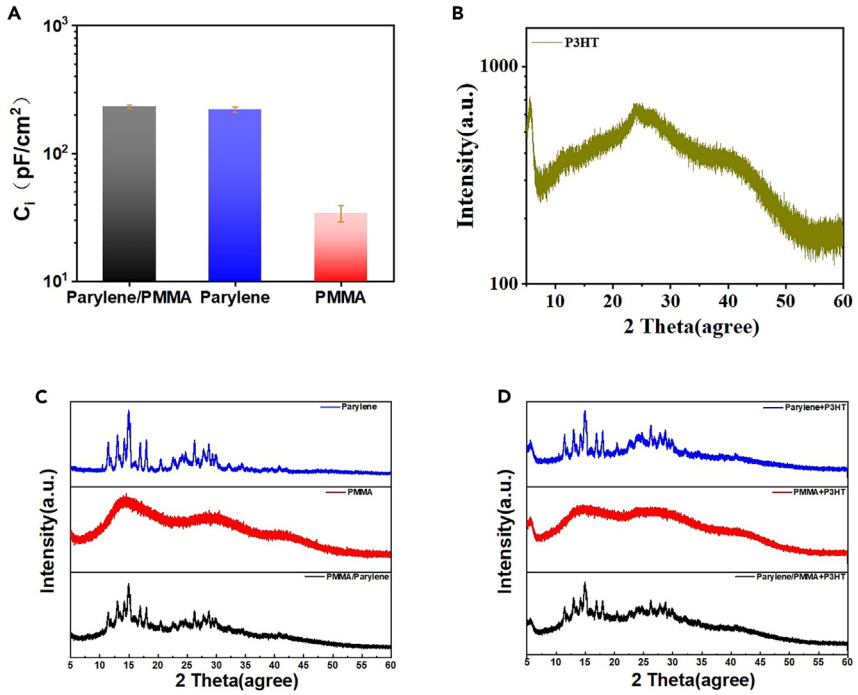

Figure 2. Capacitance and X-ray diffraction

(A) The capacitance size of metal-insulator-metal capacitors.

(B) X-ray diffraction pattern of pure P3HT.

(C) X-ray diffraction pattern of Parylene, PMMA, and Parylene/PMMA.

(D) X-ray diffraction pattern of P3HT on different layers.

and enhancing device stability. Throughout the device fabrication process, the introduction of a bilayer dielectric structure not only utilizes the high insulation performance of Parylene to ensure low leakage current in the OTFTs but also leverages the good interfacial compatibility between PMMA and P3HT, thereby enhancing the overall performance of the OTFTs. This innovative design in achieving high-performance OTFTs provides new perspectives and strategies for the optimization and application expansion of future organic electronic devices.

In the aforementioned preparation process, both Parylene and PMMA are employed as single-molecular-weight polymers. Nevertheless, polymers with varying molecular weights exert diverse influences on device performance. High molecular weight polymers often impart superior electrical properties, enhancing carrier mobility and conductivity. Furthermore, elevated molecular weight contributes to bolstering the mechanical stability of the polymer, thereby improving the device's reliability. The appropriate molecular weight is paramount for processing performance, ensuring the smooth formation of thin films and device fabrication. Polymers with higher molecular weights typically demonstrate enhanced thermal stability, rendering them particularly effective in high-temperature environments.[57–60] Alterations in molecular weight may also impact the electronic structure of the polymer, consequently influencing the electronic transport properties of the device.

In this study, an analysis of Parylene and PMMA as gate dielectric materials was conducted by measuring the capacitance (C) of metal-insulator-metal (MIM) capacitors to characterize these materials. As shown in Figure 2A, the capacitance value of the Parylene/PMMA bilayer film is 2.32347×10^{-10}F/cm^2, while that of the single-layer Parylene is 2.20098×10^{-10}F/cm^2, and the single-layer PMMA is only 3.41591×10^{-11} F/cm^2. This indicates that the bilayer structure has a higher capacitance and superior insulation performance compared to the single-layer PMMA. Based on the X-ray diffraction (XRD) pattern of P3HT shown in Figure 2B, we clearly observe a distinct diffraction peak at $2\theta = 5.57°$. The presence of this peak indicates the crystalline structure within the P3HT sample. Through XRD analysis, we confirm that this diffraction peak corresponds to the (100) crystal plane of the P3HT structure.[57] The intensity and shape of the diffraction peak serve as crucial indicators for evaluating the material's crystallinity. In XRD spectra, stronger and sharper diffraction peaks typically signify higher crystallinity, suggesting a more ordered arrangement of molecules. Therefore, the clear and prominent (100) diffraction peak in the graph signifies the excellent crystallinity of the P3HT sample, indicating a relatively compact arrangement of molecules. This underscores P3HT as a promising active layer material suitable for a variety of devices.

The XRD diagram (Figure 2C) reveals that the single-layer Parylene film exhibits distinct diffraction peaks around $2\theta = 16°$, reflecting its higher degree of crystallinity and surface roughness. In contrast, the PMMA film shows broad and diffuse peaks, indicative of its amorphous structure. The Parylene/PMMA bilayer film in the diffraction diagram presents broad diffuse peaks similar to PMMA, suggesting that the bilayer structure combines the surface properties of PMMA with the high insulation of Parylene. Therefore, the bilayer structure not only offers

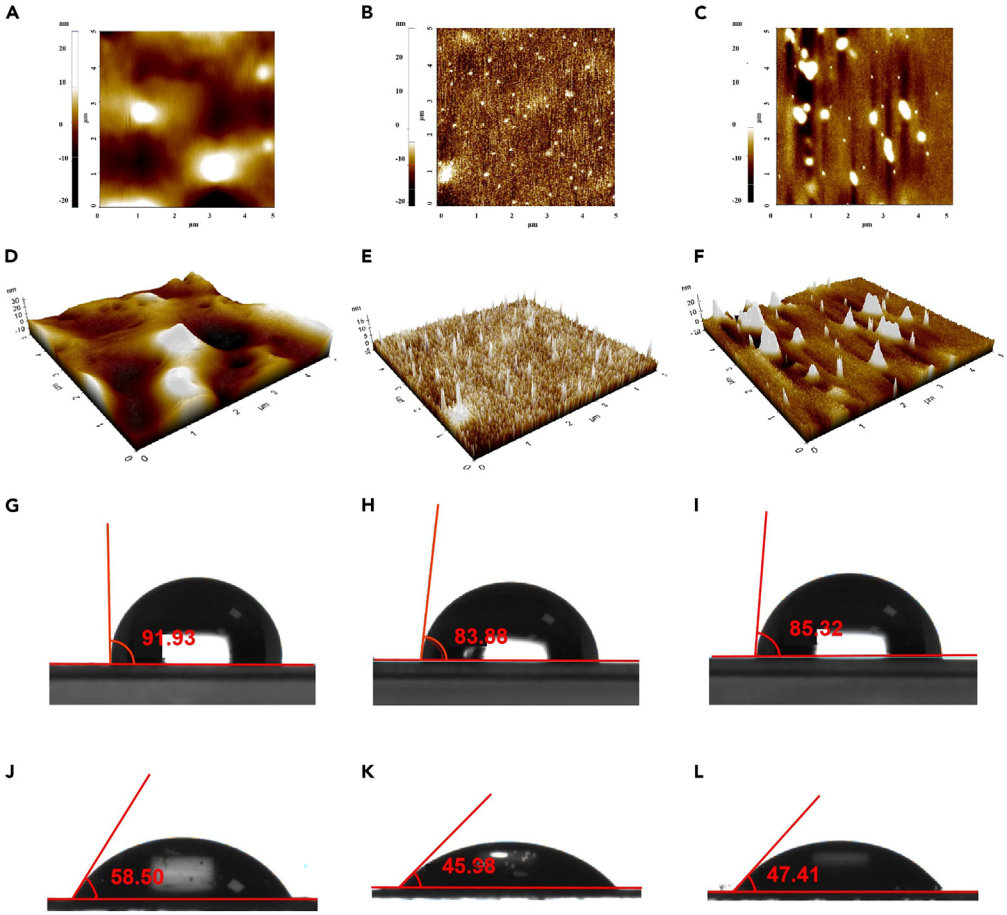

Figure 3. AFM chart and water contact Angle test

(A and D) AFM diagram of Parylene film.
(B and E) AFM diagram of PMMA thin film.
(C and F) AFM diagram of Parylene/PMMA films.
(G) Water contact Angle test diagram for Parylene film.
(H) Water contact Angle test diagram of PMMA film.
(I) Water contact Angle test diagram for Parylene/PMMA films.
(J) Ethylene glycol contact Angle test diagram for Parylene film.
(K) Polyethylene glycol contact Angle test diagram of PMMA film.
(L) Polyethylene glycol contact Angle test diagram for Parylene/PMMA films.

surface properties akin to PMMA but also enhances the insulation performance, making it an ideal choice for the gate dielectric layer material. The XRD pattern provided shows the crystalline structure of P3HT when deposited on different dielectric layers. For P3HT on a Parylene layer, the XRD pattern exhibits sharp peaks, indicating a high degree of crystallinity. In contrast, the P3HT on the PMMA layer shows a less pronounced crystalline structure, with broader and lower intensity peaks, suggesting lower crystallinity. When P3HT is deposited on a bilayer of Parylene/PMMA, the XRD pattern reveals a combination of characteristics, with crystallinity that appears to be enhanced compared to P3HT on PMMA alone, as indicated by sharper peaks than those in the PMMA layer but less sharp than in the Parylene layer alone. This suggests that the bilayer structure may promote a more ordered arrangement of P3HT chains than a single PMMA layer, potentially leading to improved charge transport properties.

In this study, the surface morphology of different dielectric layers in the dielectric system was investigated using atomic force microscopy. As shown in Figures 3A–3F, the surface roughness of Parylene and PMMA films was measured to be 2.959 nm and 0.200 nm (refer to Figure S2), respectively, while the Parylene/PMMA bilayer film exhibited a surface roughness of 0.616 nm. The results indicate that PMMA demonstrates a lower surface roughness compared to the Parylene film, with the surface roughness of the Parylene/PMMA bilayer being slightly higher than that of the PMMA film but significantly lower than that of the Parylene film. To evaluate the hydrophilicity and hydrophobicity of the three, contact angle experiments were conducted under dry conditions at 25°C using 16 μL droplets of water and ethylene glycol. Data collection included five measurements per sample, and the presented results reflect their average values. The contact angle of Parylene with ethylene

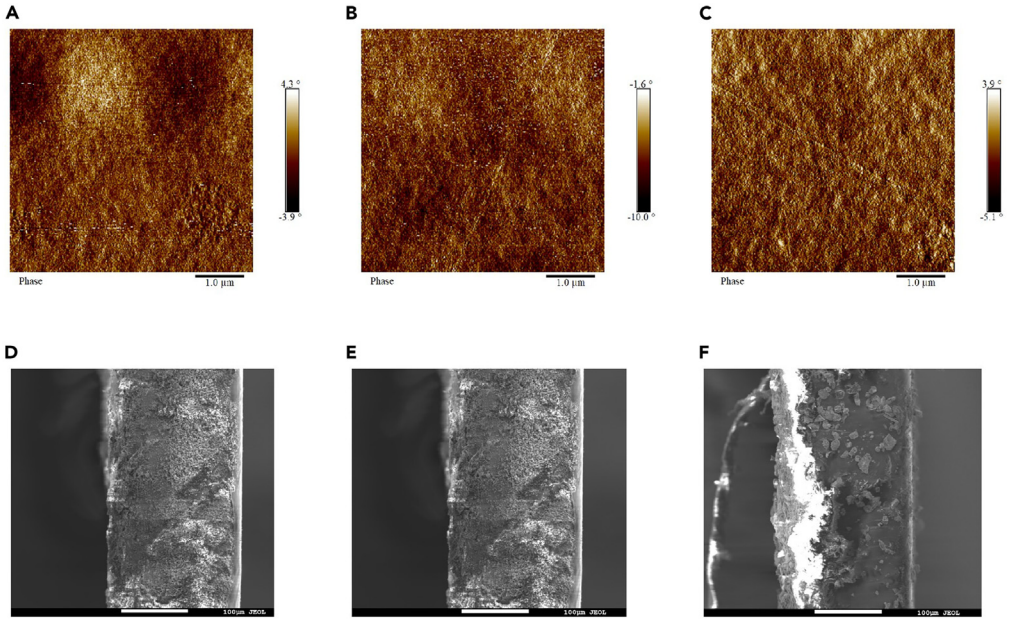

Figure 4. AFM phase diagram and ertical layering diagrams

(A) AFM phase diagram of Parylene film.
(B) AFM phase diagram of PMMA film.
(C) AFM phase diagram of Parylene/PMMA films.
(D) SEM vertical layering of Parylene films diagrams.
(E) SEM vertical layering of PMMA films diagrams.
(F) SEM vertical layering of Parylene/PMMA films diagrams.

glycol was 58.50°, that of PMMA was 45.98°, and for the Parylene/PMMA bilayer film, it was 47.41°. According to the OWRK equation, the total surface energy of Parylene was calculated to be 197.02 mN/m. For PMMA, the total surface energy was found to be 184.23 mN/m, and for the Parylene/PMMA bilayer film, it was 182.66 mN/m. These values show that the Parylene/PMMA bilayer film has a lower total surface energy compared to the monolayer materials. In summary, the Parylene/PMMA bilayer film, with its lower surface roughness and moderate surface energy, displays significant advantages in the application of dielectric layers. It not only improves the smoothness of the transistor interface, reducing carrier scattering and interface state density, thereby potentially enhancing device performance, but also combines the hydrophobicity and chemical stability of the two materials, providing the possibility for higher electrical stability and reliability.

Examining Figures 4A–4C, we can gather insights from the AFM phase diagrams of three distinct thin film transistors. In the analysis of the Parylene/PMMA double insulating layer thin film transistor, a phase difference of 8.2° is observed. Comparatively, the Parylene single insulating layer thin film transistor exhibits a phase difference of 8.4°, and the PMMA single insulating layer thin film transistor has a phase difference of 9.0°. Importantly, the phase difference for the Parylene/PMMA double insulating layer thin film transistor is smaller than that of the other two counterparts. This indicates that the Parylene/PMMA double insulating layer thin film transistor boasts a flatter and smoother surface, accompanied by more uniform chemical properties and less variation in physical properties. Such findings suggest potential superiority in performance for the Parylene/PMMA bilayer thin film transistor compared to the other two transistors. These results offer valuable insights for a deeper comprehension of the characteristics and performance of diverse thin film transistors, providing essential information for further research and optimization.

As shown in the Figures 4D–4F represent the vertical stratification images of Parylene/PMMA, Parylene, and PMMA as insulating layers, respectively. From Figure 4D, clear interfacial stratification can be observed, indicating good adhesion and integration between the two materials. This bilayer film structure provides excellent insulation and a smoother interface, which suggests that thin-film transistors made with this bilayer structure will exhibit superior performance. The cross-section of Parylene shown in Figure 4E displays a uniform film layer, but the absence of PMMA means a higher roughness at the interface. While Parylene possesses excellent electrical insulation properties, surface roughness can negatively affect the formation of the active layer. The PMMA layer is crucial for providing a good substrate for semiconductor deposition; however, as a single material, PMMA may lack the high electrical insulation provided by Parylene, resulting in lower performance of thin-film transistors fabricated with a single layer of PMMA.

In this study, OTFTs devices with P3HT as the active layer and Parylene/PMMA, Parylene, and PMMA as the dielectric layers were fabricated and their output and transfer characteristics curves were measured at room temperature. Figures 5A–5C display the output characteristic curves of three different dielectric layers. The output characteristic curve in Figure 5A clearly shows that OTFTs with Parylene/PMMA bilayer gate dielectric layers possess excellent current saturation characteristics and a high level of gate voltage regulation. With different gate

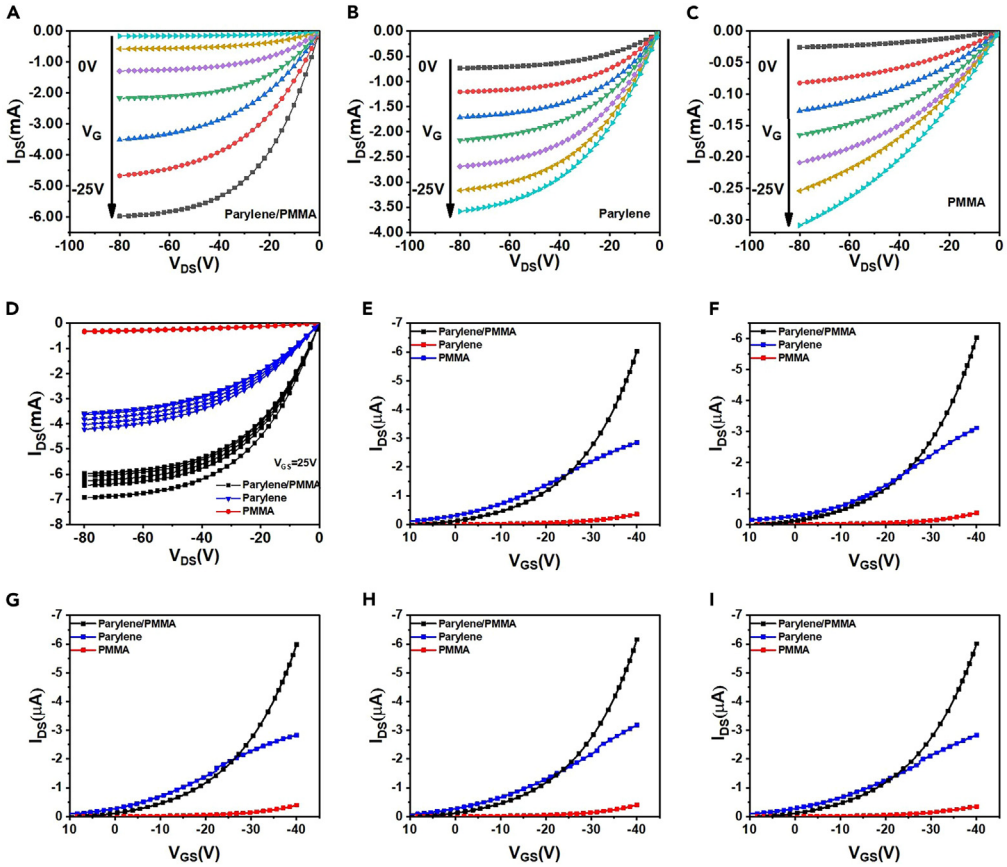

Figure 5. Curves of output and transfer characteristics

(A) Parylene/PMMA double insulation OTFTs output characteristic curve.

(B) Output characteristic diagram of Parylene single insulation layer.

(C) Output characteristic curve of PMMA single insulation layer.

(D) Comparison of output characteristic curves of devices under different OTFTs.

(E–I) Transfer characteristic curve ($I_{DS} \sim V_{GS}$).

voltages applied, the drain current can saturate stably, indicating that the device can operate within a wide voltage range without losing stability. As the gate voltage gradually decreases, the increase in drain current shows good linearity, reflecting the superiority of the bilayer dielectric structure in regulating carrier concentration and controlling device switching characteristics. Such characteristics not only enhance the adjustability of the device but also indicate that the Parylene/PMMA dielectric layer can effectively support the P3HT semiconductor layer, optimizing its charge transfer path. Thus, this bilayer dielectric structure has significant advantages in achieving high-performance OTFTs.

Figure 5B shows the output characteristic curves of OTFTs using Parylene as the gate dielectric layer. It can be observed that these devices do not exhibit as pronounced saturation characteristics of the drain current under various gate voltages compared to the Parylene/PMMA bilayer dielectric layer. Especially in the high gate voltage area, the devices show higher leakage current, which may lead to higher power consumption and reduced efficiency. The shortcomings of these characteristics may stem from the higher surface energy of Parylene, which makes it difficult for the P3HT semiconductor layer formed on its surface to achieve an ideal molecular arrangement and crystal form, thereby affecting its carrier transport efficiency. Moreover, the binding between Parylene and P3HT may not be as tight as that between PMMA and P3HT, which could lead to more interface traps and charge scattering centers, thus reducing the overall carrier mobility and current on/off ratio of the device. These factors combined may be the reason for the poor performance of OTFTs using only Parylene as the gate dielectric layer.

Figure 5C presents the output characteristic curves of OTFTs with PMMA as the single-layer gate dielectric layer. Under each gate voltage level, the relationship between the drain current and the drain-source voltage is relatively consistent, exhibiting good linearity. However, compared to the Parylene/PMMA bilayer dielectric layer structure, the single-layer PMMA structure shows an overall smaller magnitude of drain current at the same gate voltages. This suggests that although the single-layer PMMA dielectric layer demonstrates certain insulating performance, its current modulation capability is significantly weaker than that of the Parylene/PMMA bilayer dielectric layer structure. Additionally, the thinness of the PMMA layer may also limit its insulating performance under higher electric fields, as evidenced by the trend of

current saturation at high gate voltages. This is particularly critical for the high-performance operation of the device, as a good insulating layer can effectively reduce the trapping effect of carriers at the interface between the semiconductor and dielectric layer, thereby improving the device's carrier mobility and on/off current ratio. Therefore, although PMMA as a dielectric layer shows certain advantages, such as facilitating the spin-coating of the P3HT layer, its relatively thin layer thickness and insufficient insulating performance under high electric fields still limit the overall performance of the device.

As shown in Figure 5D, a comparison of the output characteristic curves at V_{GS} = 25V for the three different devices is presented. These observations are based on five tests for each dielectric layer configuration, providing reliable data support. The excellent performance of the Parylene/PMMA bilayer insulating layer may be attributed to Parylene's high insulating strength and PMMA's role in interface optimization, which is consistent with previous studies that PMMA can enhance the crystallinity and orderliness of the P3HT layer, and thus may affect the performance of the device's drain-source current.

Figures 5E–5I presents a comparison of transfer curves of OTFTs with three different dielectric structures, randomly selected from a pool of 50 devices. The logarithmic transfer characteristic curve is displayed in Figure S3. Through these curves, we can observe the trends of drain-source current (I_{DS}) changes under different gate voltages (V_{GS}). It is evident that OTFTs with Parylene/PMMA bilayer insulating layers (black curves) show smooth and consistent current changes across the entire V_{GS} range, indicating that this bilayer structure can maintain stable current regulation over a wide range of voltages. In contrast, OTFTs with a single Parylene structure (blue curves) exhibit slightly increased current changes at the low voltage end, although they show characteristics similar to the bilayer structure at the high voltage end. OTFTs with a single PMMA structure (red curves) display more significant current changes at all V_{GS} levels, which could be due to weaker insulating layer characteristics. A comprehensive analysis of these five transfer curves clearly demonstrates the significant advantages of Parylene/PMMA bilayer insulating layers in stability and current regulation. These results are based on data from five repeated tests of each structure, ensuring the accuracy and reproducibility of the experimental results.

The histograms in Figures 6A–6C display the carrier mobility and current on/off ratio of OTFTs devices fabricated using various insulating layer materials: Parylene/PMMA, Parylene, and PMMA. There are a total of 50 devices for each material. Comparing these three graphs, it's evident that devices with a Parylene/PMMA dual insulation layer exhibit more concentrated parameters, suggesting better stability compared to those with Parylene or PMMA as the insulation layer.

In the study depicted in Figure 6D, OTFTs with a Parylene/PMMA bilayer dielectric layer demonstrated a significantly higher average carrier mobility of 0.364 $cm^2/(V \cdot S)$ from fifty devices, which is substantially greater than that of OTFTs with single-layer Parylene and PMMA dielectrics. The OTFTs with a single-layer Parylene dielectric layer showed an average carrier mobility of 0.013 $cm^2/(V \cdot S)$, indicating a pronounced decrease in carrier mobility compared to the bilayer structure, while the OTFTs with a single-layer PMMA dielectric layer had an average carrier mobility of only 0.032 $cm^2/(V \cdot S)$ from five devices, further lower than the single-layer Parylene structure. These data suggest that among the three different dielectric layer structures, the Parylene/PMMA bilayer structure most effectively facilitates carrier migration due to a synergistic effect that provides a smoother and more orderly semiconductor/dielectric interface, thus reducing the number of interface traps and optimizing the paths for carrier transport. On the other hand, the single-layer Parylene, although providing good insulation characteristics, is less effective in optimizing carrier transport compared to the bilayer structure; and the thinner PMMA layer and its possible surface roughness affect its performance as a dielectric layer, resulting in a significant drop in carrier mobility. These analysis results emphasize the significant impact of dielectric layer structure and surface properties on the carrier mobility of OTFTs.

Figure 6E presents a comparison of the current switching ratio (I_{on}/I_{off}) of OTFTs utilizing different dielectric layer materials. It is evident from the graph that OTFTs with a Parylene/PMMA bilayer dielectric layer possess the highest current switching ratio, far exceeding that of OTFTs with single-layer Parylene or PMMA dielectrics. A high current switching ratio is indicative of high-performance transistors as it signifies a large variation in current between the on and off states, crucial for achieving rapid switching and high contrast display. The Parylene/PMMA bilayer structure provides more effective paths for charge carrier flow and lower interface trap density, allowing carriers to move more easily within the semiconductor channel, resulting in higher on-state currents. While single-layer Parylene and PMMA dielectrics provide some degree of current modulation, they are evidently not as effective as the bilayer structure, due to their limited ability to reduce interface traps or optimize charge transport.

As shown in Figure 6F, the graph illustrates the relationship between transconductance (Gm) and gate voltage (V_{GS}) for OTFTs with Parylene/PMMA, Parylene, and PMMA as dielectric layers. Transconductance measures the transistor's ability to amplify, with higher values indicating a more sensitive response to input signals. The OTFTs with Parylene/PMMA bilayer dielectrics (black curve) exhibit the highest transconductance across the entire V_{GS} range, denoting the best voltage conversion efficiency and signal amplification capability. The OTFTs with a single-layer Parylene dielectric (blue curve) show similar characteristics to the bilayer structure at higher voltages, but slightly increased current variation at the lower voltage end. The OTFTs with a single-layer PMMA dielectric (red curve) display more pronounced current variations at all VGS levels, which may result from weaker insulating properties of the dielectric layer. This comprehensive analysis of the five transfer curves clearly demonstrates the significant advantage of the Parylene/PMMA bilayer dielectric layer in terms of stability and current regulation. These results are based on data from fifty repeated tests of each structure, ensuring the accuracy and reproducibility of the experimental outcomes.

Figure 6G presents a comparison of the leakage current of OTFTs with Parylene/PMMA bilayer dielectric layers, single-layer Parylene, and single-layer PMMA at V_{GS}. As V_{GS} increases negatively, all OTFTs show a trend of increasing leakage current, but those with Parylene/PMMA bilayer dielectrics exhibit lower leakage currents, reflecting superior insulation performance. In contrast, OTFTs with a single-layer PMMA dielectric show significantly higher leakage currents at the same V_{GS}, indicating a weaker barrier effect of the insulating layer. The leakage

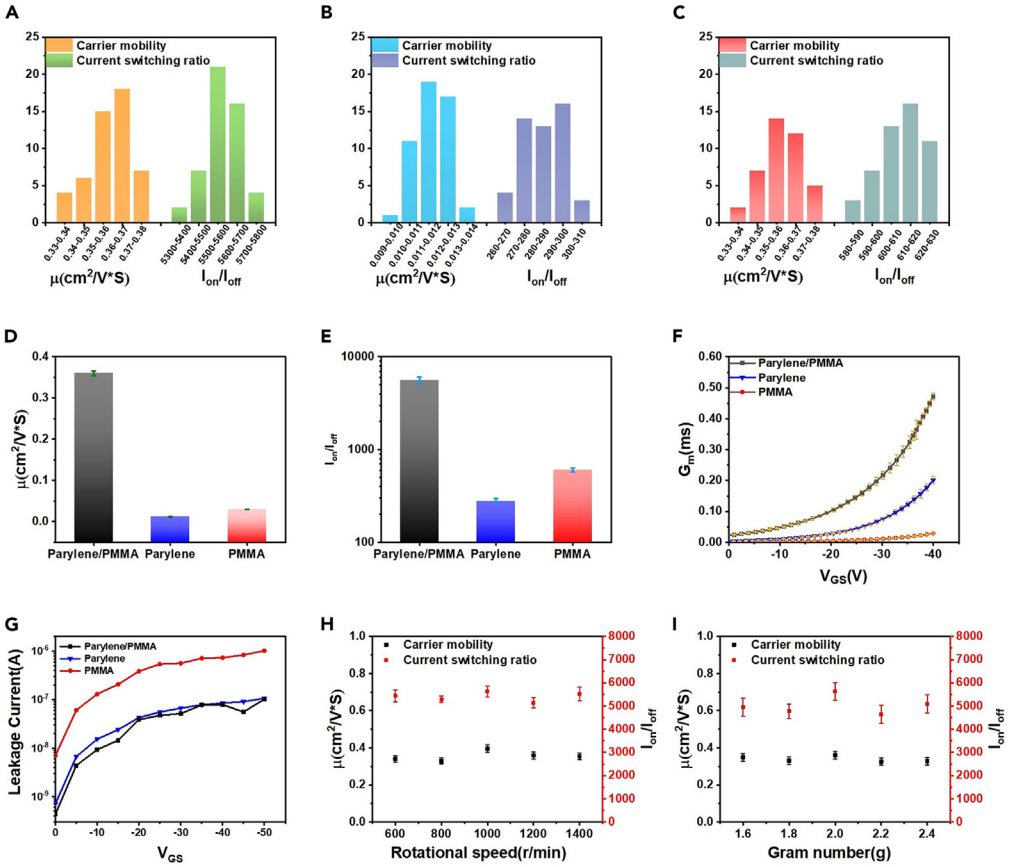

Figure 6. Performance parameter comparison

(A) Parameter distribution diagram of Parylene/PMMA double insulation layer.
(B) Parameter distribution diagram of Parylene single insulation layer.
(C) Parameter distribution diagram of PMMA single insulation layer.
(D) Comparison diagram of carrier mobility of three different OTFTs.
(E) Comparison diagram of three different OTFTs current switches.
(F) Comparison of transconductance of three different OTFTs.
(G) Comparison of leakage current of three different OTFTs.
(H) Influence of different coating speeds on the performance of OTFTs.
(I) Influence of different Parylene on the performance of OTFTs.

current of OTFTs with a single-layer Parylene dielectric lies between the two, emphasizing the significant advantage of the Parylene/PMMA combination in enhancing device insulation and reducing undesired current flow, while also highlighting the limitations of PMMA layer's insulating performance.

Figure 6H shows the variation of carrier mobility (μ_{FET}) and current switching ratio (I_{on}/I_{off}) of OTFTs based on Parylene/PMMA bilayer dielectric layers with increasing PMMA dielectric layer thickness. It is observed that the carrier mobility fluctuates minimally with changes in PMMA layer thickness, indicating that the thickness of the PMMA layer has little effect on the carrier mobility of OTFTs. The current switching ratio initially increases slightly with the thickness of the PMMA dielectric layer, and then stabilizes, suggesting that within the tested PMMA thickness range, the current switching ratio is not sensitive to changes in PMMA layer thickness. This may indicate that within this thickness range, the PMMA layer is already sufficiently thick to maintain its insulating properties, hence not significantly affecting the switching performance of the OTFTs. After the comprehensive consideration, it can be determined that a PMMA layer thickness of approximately 100 nm is an ideal choice. This thickness not only retains insulating properties but also provides a stable performance for carrier mobility and current switching ratio.

Figure 6I presents the comparison of carrier mobility and current switching ratio for thin-film transistors with varying amounts of Parylene. It is evident from the graph that the highest carrier mobility and current switching ratio are achieved when 2 g of Parylene is used, corresponding to a film thickness of 629 nm. This indicates that at a thickness of 629 nm, the Parylene film provides the optimal performance for the thin-film transistors.

In this paper, various aspects of the performance of P3HT organic thin film crystals based on different dielectric layers are compared. Table 1 provides a performance comparison, including carrier mobility, transconductance, and film thickness. It shows that the Parylene/PMMA

Table 1. Comparison table of carrier mobility, transconductance and insulation thickness of P3HT thin film transistors with different dielectric layers

	dielectric layer material	carrier mobility ($cm^2V^{-1}S^{-1}$)	transconductance (mS)	Thickness (nm)
This work	Parylene/PMMA	3.6×10^{-1}	0.473	629/100
This work	Parylene	1.3×10^{-2}	0.202	652
This work	PMMA	3.2×10^{-2}	0.028	100
Hao et al.[61]	PVA	6.3×10^{-3}	0.116	*
Hao et al.[61]	PVA/PMMA	4.6×10^{-2}	0.081	*
Rajeev et al.[62]	SiO_2	3.2×10^{-4}	*	*
Ramajothi et al.[63]	TiO_2	3.7×10^{-3}	*	*
Yamamoto et al.[64]	PVP	2.0×10^{-2}	*	*
Ren et al.[65]	Si/SiO_2	3.9×10^{-2}	*	*
Chang et al.[66]	SiO_2	2.4×10^{-1}	*	*

double insulating layer thin-film transistor exhibits the highest carrier mobility among all the tested devices. Additionally, it demonstrates the best overall performance in terms of transconductance and carrier mobility.

Conclusion

This paper reports the successful preparation of an OTFT with excellent performance, using vapor deposition and spin coating to create a double dielectric layer. Through a comparative study of the molecular structure, XRD, hydrophilicity, hydrophobicity, surface roughness of Parylene, and PMMA, as well as the drain current characteristics of three different thin-film transistors, the advantages of the bilayer dielectric layer are clearly presented. In particular, this study demonstrates the superior performance of the bilayer Parylene/PMMA dielectric layer in terms of hydrophilicity, surface polarity, and surface roughness, as compared to both the single-layer Parylene and the single-layer PMMA. The synergistic effect of the two materials, PMMA and Parylene, is also highlighted in this study. The bilayer structure maximizes the benefits of PMMA's low surface polarity and Parylene's high insulating property. Devices with this double-layer dielectric layer exhibit better carrier mobility, higher current switching ratio, and lower transfer hysteresis. Furthermore, this paper compares the performance of OTFTs with the double-layer Parylene/PMMA dielectric to that of OTFTs with different dielectric layers, and the overall performance is significantly superior to other thin-film transistors. In conclusion, this study provides strong support for the preparation and performance optimization of bilayer Parylene/PMMA thin-film transistors. The combination of the two materials has resulted in a bilayer dielectric layer structure with superior properties, which opens up new possibilities for the enhancement of performance and expansion of the application of OTFTs.

STAR★METHODS

Detailed methods are provided in the online version of this paper and include the following:

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SUPPLEMENTAL INFORMATION

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AUTHOR CONTRIBUTIONS

S.S.: conceptualization and funding acquisition. L.L.: writing-original draft and editing. Q.L.: conceptualization, methodology, funding acquisition, and writing-review and editing. L.D.: funding acquisition and writing-review and editing. X.L.: visualization. Y.L.: visualization. Z.C.: validation. Y.C.: validation. R.U.: validation. J.M.: validation. J.J.: funding acquisition.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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REFERENCES

1. Leite, G.V., and Boudinov, H.I. (2021). Defect-Free and Annealing Influences in P3HT Organic Field-Effect Transistor Performance. IEEE Trans. Device Mater. Reliab. *21*, 111–116.
2. Yedikardes, B., Ordokhani, F., Akkan, N., Kurt, E., Yavuz, N.K., Zayim, E., and Altun, M. (2021). Enhanced Electrical Properties of P3HT:WO3 Hybrid Thin Film Transistors. J. Electron. Mater. *50*, 2466–2475.
3. Nketia-Yawson, B., Ahn, H., and Jo, J.W. (2022). Understanding Effects of Ion Diffusion on Charge Carrier Mobility of Electrolyte-Gated Organic Transistor Using Ionic Liquid-Embedded Poly(3-hexylthiophene). Adv. Funct. Mater. *32*, 1–9.
4. Zhao, S., Hou, S., Fan, H., Wang, Z., and Yu, J. (2020). High performance nitrogen dioxide sensor based on organic thin-film transistor utilizing P3HT/OH-MWCNTs blend film. Synth. Met. *269*, 116569.
5. In, C., Kim, D., Roh, Y.-G., Kim, S.W., Lee, H., Park, Y., Kim, S., Kim, U.J., Choi, H., and Hwang, S.W. (2018). Photocurrent Engineering of Silicon Nanowire Field-Effect Transistors by Ultrathin Poly(3-hexylthiophene). Adv. Mater. Interfac. *5*, 1–7.
6. Huang, H.J.N., Nan, H.R., Yang, Y.G., Gao, X.Y., Chen, F., and Chen, Z.K. (2018). Improved Performance of Thick Films Based Binary and Ternary Bulk Heterojunction Organic Photovoltaic Devices Incorporated with Electrospinning Processed Nanofibers. Adv. Mater. Interfac. *5*, 1–10.
7. Bhatt, M.P., Magurudeniya, H.D., Rainbolt, E.A., Huang, P., Dissanayake, D.S., Biewer, M.C., and Stefan, M.C. (2014). Poly(3-hexylthiophene) nanostructured materials for organic electronics applications. J. Nanosci. Nanotechnol. *14*, 1033–1050.
8. Kang, W.T., Phan, T.L., Ahn, K.J., Lee, I., Kim, Y.R., Won, U.Y., Kim, J.E., Lee, Y.H., and Yu, W.J. (2021). Selective Pattern Growth of Atomically Thin MoSe2 Films via a Surface-Mediated Liquid-Phase Promoter. ACS Appl. Mater. Interfaces *13*, 18056–18064.
9. Lin, C.-J., Liu, C.-L., and Chen, W.-C. (2015). Poly(3-hexylthiophene)-graphene composite-based aligned nanofibers for high-performance field effect transistors. J. Mater. Chem. C *3*, 4290–4296.
10. Ram, M.S., and Abdi, D.B. (2016). Performance Investigation of Single Grain Boundary Junctionless Field Effect Transistor. IEEE J. Electron Devices Soc. *4*, 480–484.
11. Wu, X., Du, R., Fang, L., Chu, Y., Li, Z., and Huang, J. (2019). Grain size adjustment in organic field-effect transistors for chemical sensing performance improvement. Sci. China Mater. *62*, 138–145.
12. Dong, H., Fu, X., Liu, J., Wang, Z., and Hu, W. (2013). 25th Anniversary Article: Key Points for High-Mobility Organic Field-Effect Transistors. Adv. Mater. *25*, 6158–6183.
13. Zhang, F., Hu, Y., Lou, Z., Xin, X., Zhang, M., Hou, Y., and Teng, F. (2018). Interface studies of well-controlled polymer bilayers and field-effect transistors prepared by a mixed-solvent method. RSC Adv. *8*, 11272–11279.
14. Gupta, S., Sharma, D., Soni, D., Yadav, S., Aslam, M., Yadav, D.S., Nigam, K., and Sharma, N. (2018). Examination of the impingement of interface trap charges on heterogeneous gate dielectric dual material control gate tunnel field effect transistor for the refinement of device reliability. Micro Nano Lett. *13*, 1192–1196.
15. Jung, M.-C., Leyden, M.R., Nikiforov, G.O., Lee, M.V., Lee, H.K., Shin, T.J., Takimiya, K., and Qi, Y. (2015). Flat-Lying Semiconductor-Insulator Interfacial Layer in DNTT Thin Films. ACS Appl. Mater. Interfaces *7*, 1833–1840.
16. Liguori, R., Facchetti, A., Licciardo, G.D., and Di Benedetto, L. (2022). Processing-Structure-Performance Relationship in Organic Transistors: Experiments and Model. Electronics *11*, 197.
17. Ismail, A.G., and Hill, I.G. (2011). Stability of n-channel organic thin-film transistors using oxide, SAM-modified oxide and polymeric gate dielectrics. Org. Electron. *12*, 1033–1042.
18. Yang, F.-Y., Hsu, M.-Y., Hwang, G.-W., and Chang, K.-J. (2010). High-performance poly(3-hexylthiophene) top-gate transistors incorporating TiO2 nanocomposite dielectrics. Org. Electron. *11*, 81–88.
19. Zhu, J.-J., Ma, X.H., Chen, W.W., Hou, B., Xie, Y., and Hao, Y. (2016). Comparative study on interface and bulk charges in AlGaN/GaN metal-insulator-semiconductor heterostructures with Al2O3, AlN, and Al_2O_3/AlN laminated dielectrics. Jpn. J. Appl. Phys. *55*, 05FH01.
20. Le, S.P., Nguyen, D.D., and Suzuki, T.-K. (2018). Insulator-semiconductor interface fixed charges in AlGaN/GaN metal-insulator-semiconductor devices with Al2O3 or AlTiO gate dielectrics. J. Appl. Phys. *123*, 1–7.
21. Biswas, D., Torii, N., Fujita, H., Yoshida, T., Kubo, T., and Egawa, T. (2019). Trap state characterization of Al2O3/AlInGaN/GaN metal-insulator-semiconductor heterostructures. Semicond. Sci. Technol. *34*, 1–6.
22. Cavallari, M.R., Zanchin, V.R., Valle, M.A., Izquierdo, J.E.E., Rodriguez, E.M., Rodriguez, E.F.G., Pereira-da-Silva, M.A., and Fonseca, F.J. (2015). On the Performance Degradation of Poly(3-Hexylthiophene) Field-Effect Transistors. IEEE Trans. Device Mater. Reliab. *15*, 342–351.
23. Wang, X., Lee, W.H., Zhang, G., Wang, X., Kang, B., Lu, H., Qiu, L., and Cho, K. (2013). Self-stratified semiconductor/dielectric polymer blends: vertical phase separation for facile fabrication of organic transistors. J. Mater. Chem. C *1*, 3989–3998.
24. Gao, L., Hou, S., Wang, Z., Gao, Z., Yu, X., and Yu, J. (2019). One-Step Coating Processed Phototransistors Enabled by Phase Separation of Semiconductor and Dielectric Blend Film. Micromachines *10*, 716.
25. Xiang, L., Wang, W., and Gao, F. (2016). Improving Mobility and Stability of Organic Field-Effect Transistors by Employing a Tetratetracontane Modifying PMMA Dielectric. IEEE Trans. Electron. Dev. *63*, 4440–4444.
26. Li, X.Y., Yang, G., Xu, L., and Chen, Z.J. (2022). Influence of Polymer Interfacial Protective Layer Thickness on the Stability of Lithium-Metal Batteries. Adv. Mater. Interfac. *9*, 1–9.
27. Zhang, H., Zhang, F., Sun, J., Zhang, M., Hu, Y., Lou, Z., Hou, Y., and Teng, F. (2019). Solution-processed organic field-effect transistors with cross-linked poly(4-vinylphenol)/polyvinyl alcohol bilayer dielectrics. Appl. Surf. Sci. *478*, 699–707.
28. Alhusaiki-Alghamdi, H.M. (2021). The spectroscopic and physical properties of PMMA/PCL blend incorporated with graphene oxide. Results Phys. *24*, 104125–104127.
29. Alsaad, A.M., Ahmad, A.A., Al Dairy, A.R., Al-anbar, A.S., and Al-Bataineh, Q.M. (2020). Spectroscopic characterization of optical and thermal properties of (PMMA-PVA) hybrid thin films doped with SiO2 nanoparticles. Results Phys. *19*, 1–10.
30. Aziz, S.B., Abdullah, O.G., Brza, M.A., Azawy, A.K., and Tahir, D.A. (2019). Effect of carbon nano-dots (CNDs) on structural and optical properties of PMMA polymer composite. Results Phys. *15*, 102776.
31. Chitnis, D., Kalyani, N.T., and Dhoble, S.J. (2019). Comprehensive study on photophysical properties of Eu(TTA)3bipy phosphor molecularly doped in PMMA and PS matrices. Results Phys. *13*, 1–17.

32. Wang, X., Bai, X., Pang, Z., Yang, H., and Qi, Y. (2019). Investigation of surface plasmons in Kretschmann structure loaded with a silver nano-cube. Results Phys. *12*, 1866–1870.
33. Zheng, S., Yang, W., Sun, Q.-Q., Chen, L., Zhou, P., Wang, P.-F., Zhang, D.W., and Xiao, F. (2013). Schottky barrier height reduction for metal/n-InP by inserting ultra-thin atomic layer deposited high-k dielectrics. Appl. Phys. Lett. *103*, 1–5.
34. Yi, M., Guo, J., Li, W., Xie, L., Fan, Q., and Huang, W. (2015). High-mobility flexible pentacene-based organic field-effect transistors with PMMA/PVP double gate insulator layers and the investigation on their mechanical flexibility and thermal stability. RSC Adv. *5*, 95273–95279.
35. Nakamura, K., Hanawa, H., and Horio, K. (2019). Analysis of Breakdown Voltages in AlGaN/GaN HEMTs with Low-k/High-k Double Passivation Layers. IEEE Trans. Device Mater. Reliab. *19*, 298–303.
36. Belkacemi, S., and Hafdi, Z. (2018). High-k Dielectric Based Amorphous Silicon Thin-Film Transistor for Medical Imaging. Int. Conf. Signal, 1–5.
37. Marszalek, T., Gazicki-Lipman, M., and Ulanski, J. (2017). Parylene C as a versatile dielectric material for organic field-effect transistors. Beilstein J. Nanotechnol. *8*, 1532–1545.
38. Wei, T., Fujiwara, K., Kanki, T., and Tanaka, H. (2016). Impact of parylene-C thickness on performance of KTaO3 field-effect transistors with high-k oxide/parylene-C hybrid gate dielectric. J. Appl. Phys. *119*, 1–5.
39. Kondo, M., Uemura, T., Matsumoto, T., Araki, T., Yoshimoto, S., and Sekitani, T. (2016). Ultraflexible and ultrathin polymeric gate insulator for 2V organic transistor circuits. APEX *9*, 061602.
40. Lee, Y.-S., Gasonoo, A., Lee, J.H., Yoon, J.H., Raji, A., Baek, S.Y., Choi, Y., and Lee, J. (2022). Optical and Electrical Characterization of Visible Parylene Films. Materials *15*, 6717.
41. Park, H., Ahn, H., Kwon, J., Kim, S., and Jung, S. (2018). Parylene-Based Double-Layer Gate Dielectrics for Organic Field-Effect Transistors. ACS Appl. Mater. Interfaces *10*, 37767–37772.
42. Nair, S., Kathiresan, M., Mukundan, T., and Natarajan, V. (2016). Passivation of organic field effect transistor with photopatterned Parylene to improve environmental stability. Microelectron. Eng. *163*, 36–42.
43. Ashimine, T., Onoue, T., Yasuda, T., Fujita, K., and Tsutsui, T. (2007). Parylene-C and high-k polymer bilayer gate dielectric for low-operating voltage organic field-effect transistors. Mol. Cryst. Liq. Cryst. *471*, 221–227.
44. Ye, H., Kwon, H.-J., Tang, X., Park, C.E., An, T.K., and Kim, S.H. (2020). Parylene-based polymeric dielectric top-gate organic field-effect transistors exposed to a UV/ozone environment. Org. Electron. *87*, 105942.
45. Tavakoli, M.M., Gharahcheshmeh, M.H., Moody, N., Bawendi, M.G., Gleason, K.K., and Kong, J. (2020). Efficient, Flexible, and Ultra-Lightweight Inverted PbS Quantum Dots Solar Cells on All-CVD-Growth of Parylene/Graphene/oCVD PEDOT Substrate with High Power-per-Weight. Adv. Mater. Interfac. *7*, 1–9.
46. Moss, T., and Greiner, A. (2020). Functionalization of Poly(para-xylylene)s-Opportunities and Challenges as Coating Material. Adv. Mater. Interfac. *7*, 1–13.
47. Werkmeister, F.X., Noever, S.J., and Nickel, B.A. (2015). Sub-monolayer percolation of pentacene on rough parylene-C dielectrics. Org. Electron. *26*, 439–442.
48. Li, X., Baek, S., Kim, K., Lee, H.S., and Kim, S.H. (2019). Surface treatment of Parylene-C gate dielectric for highly stable organic field-effect transistors. Org. Electron. *69*, 128–134.
49. Tszydel, I., Marszalek, T., Ulanski, J., Nosal, A., and Gazicki-Lipman, M. (2016). Applications of parylene films in the manufacture of organic field-effect transistors. Surf. Coat. Technol. *290*, 21–27.
50. Shin, E.-Y., Choi, E.-Y., and Noh, Y.-Y. (2017). Parylene based bilayer flexible gate dielectric layer for top-gated organic field-effect transistors. Org. Electron. *46*, 14–21.
51. Baeg, K.-J., Khim, D., Kim, D.-Y., Koo, J.B., You, I.-K., Choi, W.S., and Noh, Y.-Y. (2010). High mobility top-gated poly(3-hexylthiophene) field-effect transistors with high work-function Pt electrodes. Thin Solid Films *514*, 4024–4029.
52. Naddaka, M., Asen, F., Freza, S., Lellouche, J., Bobrowski, M., Skurski, P., Laux, E., Charmet, J., Keppner, H., and Bauer, M. (2011). Functionalization of Parylene During Its Chemical Vapor Deposition. J. Polym. Sci. A. Polym. Chem. *49*, 2952–2958.
53. Dunn, G., Shen, K., Barzegar, H.R., Shi, W., Belling, J.N., Nguyen, T.N.H., Zettl, A., Barkovich, E., Chism, K., Maharbiz, M.M., and DeWeese, M.R. (2017). Selective Insulation of Carbon Nanotubes. Phys. Status Solidi *254*, 1–5.
54. Rodriguez-Davila, R.A., Bolshakov, P., Young, C.D., and Quevedo-Lopez, M. (2019). Understanding the Effects of Low-Temperature Passivation and Annealing on ZnO TFTs Test Structures. IEEE Int. Conf. Microelectron. Test Struct. *32*, 190–193.
55. Gluschke, J.G., Samuelson, L., Micolich, A.P., Seidl, J., Lyttleton, R.W., Carrad, D.J., Cochrane, J.W., and Lehmann, S. (2018). Using Ultrathin Parylene Films as an Organic Gate Insulator in Nanowire Field-Effect Transistors. Nano Lett. *18*, 4431–4439.
56. Ji, W.-T., Lu, X.-D., Cheng, D.-Y., Sun, N., Chen, L., and Tao, W.Q. (2021). Effect of wettability on nucleate pool boiling heat transfer of a low surface tension fluid outside horizontal finned tubes. Int. Commun. Heat Mass Tran. *125*, 105340.
57. Seidler, N., Lazzerini, G.M., Li Destri, G., Marletta, G., and Cacialli, F. (2013). Enhanced crystallinity and film retention of P3HT thin-films for efficient organic solar cells by use of preformed nanofibers in solution. J. Mater. Chem. C *1*, 7748–7757.
58. Tousignant, M.N., Ronnasi, B., Tischler, V., and Lessard, B.H. (2023). N-Type Single Walled Carbon Nanotube Thin Film Transistors Using Green Tri-Layer Polymer Dielectric. Adv. Mater. Interfac. *10*, 1–8.
59. He, Z., Zhang, Z., Bi, S., and Chen, J. (2020). Effect of Polymer Molecular Weight on Morphology and Charge Transport of Small-Molecular Organic Semiconductors. Electron. Mater. Lett. *16*, 441–450.
60. Dickson, L.E., Cranston, R.R., Xu, H., Swaraj, S., Seferos, D.S., and Lessard, B.H. (2023). Blade Coating Poly(3-hexylthiophene): The Importance of Molecular Weight on Thin-Film Microstructures. ACS Appl. Mater. Interfaces *15*, 55109–55118.
61. Runfang, H., Yangfan, Y., Leilei, L., Jianlong, J., Qiang, Z., Lifeng, D., Shengbo, S., and Qiang, L. (2022). P3HT-based organic field-effect transistor for low-cost, label-free detection of immunoglobulin G. J. Biotechnol. *359*, 75–81.
62. Rajeev, V.R., Paulose, A.K., and Unni, K.N. (2018). Ammonia gas detection using field-effect transistor based on a solution-processable organic semiconductor. Vacuum *158*, 271–277.
63. Ramajothi, J., Ochiai, S., Kojima, K., and Mizutani, T. (2008). Performance of Poly(3-hexylthiophene) Field Effect Transistor With High Dielectric Constant Gate Insulator. Materials, 7–11.
64. Yamamoto, K., Ochiai, S., Wang, X., Uchida, Y., Kojima, K., Ohashi, A., and Mizutani, T. (2008). Evaluation of molecular orientation and alignment of poly(3-hexylthiophene) on Au (111) and on poly(4-vinylphenol) surfaces. Thin Solid Films *516*, 2695–2699.
65. Ren, J., Tao, Y., Li, X., Ma, T., Liu, B., and Lu, D. (2018). Effect of External Electric Field on the Ordered Structure of Molecular Chains and Hole Mobility in Regioregular Poly(3-hexylthiophene) with Different Molecular Weights. Langmuir *34*, 13871–13881.
66. Chang, M., Su, Z., and Egap, E. (2016). Alignment and Charge Transport of One-Dimensional Conjugated Polymer Nanowires in Insulating Polymer Blends. Macromolecules *49*, 9449–9456.

STAR★METHODS

KEY RESOURCES TABLE

REAGENT or RESOURCE	SOURCE	IDENTIFIER
Chemicals, peptides, and recombinant proteins		
Poly (3-hexylthiophene-2,5-diyl)	Sigma Aldrich (Shanghai) Trading Co., LTD	156074-98-5
poly (methyl methacrylate)	Shanghai Maclin Biochemical Technology Co., LTD	9011-14-7
Parylene	Shanxi Demao Hongke trading company	28804-46-8
ITO conductive film	Shenzhen Xinwei Chemical Co., LTD	156074-98-5
Conductive silver paste	Shenzhen Xinwei Chemical Co., LTD	7440-22-4
Deposited data		
P3HT-based organic field effect transistor for low-cost, label-free detection of immunoglobulin G	Runfang et al.[61] (sciencedirectassets.com)	https://doi.org/10.1016/j.jbiotec.2022.09.022
Ammonia gas detection using field-effect transistor based on a solution-processable organic semiconductor	https://www.et-fine.com/10.1016/j.vacuum.2020.109981	https://doi.org/10.1016/j.vacuum.2020.109981
Performance of Poly(3-hexylthiophene) Field Effect Transistor With High Dielectric Constant Gate Insulator	Ramajothi et al.[63]	PROCEEDINGS OF 2008 INTERNATIONAL SYMPOSIUM ON ELECTRICAL INSULATING
Evaluation of molecular orientation and alignment of poly(3-hexylthiophene) on Au (111) and on poly(4-vinylphenol) surfaces	https://www.et-fine.com/10.1016/j.tsf.2007.04.145	https://doi.org/10.1016/j.tsf.2007.04.145
Effect of External Electric Field on the Ordered Structure of Molecular Chains and Hole Mobility in Regioregular Poly(3-hexylthiophene) with Different Molecular Weights	Ren et al.[65] (et-fine.com)	https://doi.org/10.1021/acs.langmuir.8b02838
Alignment and Charge Transport of One-Dimensional Conjugated Polymer Nanowires in Insulating Polymer Blends	Chang et al.[66] (et-fine.com)	https://doi.org/10.1021/acs.macromol.6b01721

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources and reagents should be directed to and will be fulfilled by the lead contact, Qiang Li (liqiang02@tyut.edu.cn).

Materials availability

This study did not generate new unique reagents.

Data and code availability

All data reported in this paper will be shared by the lead contact upon request.

This paper does not report original code.

Any additional information required to reanalyze the data reported in this paper is available from the lead contact upon request.

METHOD DETAILS

Materials and reagents

The poly(3-hexylthiophene-2,5-diyl) (P3HT) used in this experiment, with an average molecular weight of 50,000-75,000, was purchased from Shanghai Haoyang Biotechnology. Poly (methyl methacrylate) (PMMA) (molecular weight 120 kDa), anisole (AR, 99%), and

ortho-dichlorobenzene (AR, 99%) were all procured from Shanghai Maclin BioTech. The conductive silver paste was purchased from Shenzhen Xinwei Chemical Corporation, and Parylene (AR, 99%, molecular weight 208.30) was procured from Shanxi Demeco Hongke Trading Corporation. The ITO conductive film (film thickness: 0.125 mm, sheet resistance: ~40 Ω/cm^2, transmittance: 83%) and PET film (thickness: 100 μm) were both sourced from Shenzhen Regress Technology Corporation.

Solution preparation

100mg of PMMA was dissolved in 10ml of anisole, then the solution was stirred at 800 r/min for 1 h at 50°C using a 78-1 Magnetic Stirrer to obtain 10 mg/ml of PMMA solution. 2.4 mg of P3HT was dissolved in 3 ml of o-dichlorobenzene, and the solution was covered with a double layer of sealing film and aluminum foil. The solution was stirred continuously for 12 h at room temperature in a light-protected and water-avoiding environment using a 78-1 Magnetic Stirrer. Subsequently, it was heated and stirred at 50°C for 1.5 h using an EMS-40 Magnetic Stirring water bath. Finally, an 8 mg/ml P3HT solution was obtained by subjecting it to ultrasonic cleaning at 80°C for 0.5 h using an EQ-300DE CNC Ultrasonic Cleaner.

Device preparation

In this experiment, organic thin-film transistors based on P3HT with a bottom-gate top contact structure were fabricated by covering an ITO conductive film as a gate on a flexible PET substrate. The typical structure of this device is shown in the figure below. A 3×3 cm PET substrate is cut, 1×3 cm ITO conductive film is covered on the substrate, which is successively immersed in ethanol and acetone, and then cleaned by EQ-300DE CNC Ultrasonic Cleaner for 10min each, and the residual solution on the surface is rinsed off with deionized water and blown dry with nitrogen. Utilizing the PTP-1V MLD Deposition equipment at 120°C under a vacuum level of 3×10^{-2} Pa, we deposited a Parylene film with a thickness of 629 nm onto the ITO conductive film over a duration of 10 h. Subsequently, a 500μL solution of PMMA was added dropwise, and the surface was spin-coated at a speed of 1000r/min for 60 s. The resulting structure was then subjected to a 0.5 h annealing process at 90°C in an electrically heated convection oven, leading to the formation of a homogeneous PMMA layer. This preparation process was executed under precise processing conditions and with the aid of the PTP/1V MLD deposition equipment, ensuring uniformity and stability of the Parylene film and PMMA layer on the substrate. Then the semi/finished device, and finally using the EZ4 spin coater in the PMMA film layer at 2000r/min speed 100μL of P3HT solution spin coating 60s, in the V-1515 microcomputer heating platform at 120°C annealing 10 min to get the P3HT semiconductor layer. Two conductive stripes, each with a length of 20mm and spaced 1mm apart, were printed using a Three-axis Hot-melt Automatic Dispensing Machine. Subsequently, they were annealed on a heating platform at 90°C for 10 minutes, resulting in the fabrication of a double-layer dielectric thin-film transistor based on P3HT.

Testing and characterization

In this experiment, the JY-82B Kruss DSA contact angle meter was used to measure the water contact angles of PMMA and Parylene dielectric layers, characterizing the hydrophilicity and hydrophobicity of different dielectric layers. Atomic Force Microscopy (AFM) was employed to characterize the surface height of the films, comparing the roughness and phase images of Parylene/PMMA, PMMA, and Parylene films. The SKYSCAN 1275 three-dimensional X-ray microscope (XRM) was utilized to test the X-ray diffraction patterns of PMMA, Parylene, and Parylene/PMMA, as well as those of P3HT on each of these layers. The 4200-SCS Semiconductor Characterization System was used to measure the output and transfer curves of the OTFTs. Throughout the testing process, the source electrode was continuously grounded and measurements were conducted under atmospheric conditions. The output curves ($I_{DS}V_{DS}$) of the OTFTs were measured at various gate voltages, with the control gate voltages ranging from 0 V to -25 V in -5 V steps. The transfer characteristic curves ($I_{DS}V_{GS}$) were measured under different drain voltages. Additionally, parameters such as the saturation carriers and threshold voltage of the device could be extracted from the saturation region of the transfer curves using a square extrapolation method, aiding in the assessment of device.