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Improved Pulse-Controlled Conductance Adjustment in Trilayer Resistors by Suppressing Current Overshoot

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Abstract: In this work, we demonstrate the enhanced synaptic behaviors in trilayer dielectrics ($HfO_2/Si_3N_4/SiO_2$) on highly doped n-type silicon substrate. First, the three dielectric layers were subjected to material and chemical analyses and thoroughly investigated via transmission electron microscopy and X-ray photoelectron spectroscopy. The resistive switching and synaptic behaviors were improved by inserting a Si_3N_4 layer between the HfO_2 and SiO_2 layers. The electric field within SiO_2 was mitigated, thus reducing the current overshoot in the trilayer device. The reset current was considerably reduced in the trilayer device compared to the bilayer device without a Si_3N_4 layer. Moreover, the nonlinear characteristics in the low-resistance state are helpful for implementing high-density memory. The higher array size in the trilayer device was verified by cross-point array simulation. Finally, the multiple conductance adjustment was demonstrated in the trilayer device by controlling the gradual set and reset switching behavior.

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1. Introduction

Resistive switching memory is very attractive for a wide range of applications due to its various resistive switching characteristics stemming from a number of resistive switching materials by easily tunable resistive switching parameters such as on-resistance, off-resistance, and operation voltage [1–5]. Moreover, its simple structure, such as metal–insulator–metal (MIM) with $4F^2$ (F is feature size), can be scaled down via a lithography process [1–6]. Further, the multiple resistance states triggered by electrical pulses can be used for high-density memory. Finally, the good retention properties, such as NAND flash and high endurance, provide an edge over other competing memory products. The types of resistive switching should be characterized depending on the possible applications, such as in storage class memory, neuromorphic devices, and logic devices. Among them, a neuromorphic device using resistive switching memory is attracting considerable attention [7–10]. To meet the needs of efficient data processing in the era of big data, neuromorphic computing provides a major breakthrough that can replace the existing Von Neumann computing. In particular, neuromorphic systems are specialized in data processing, such as complex pattern recognition. Moreover, they take an energy-efficient approach by carrying out data processing in a parallel manner. In a neuromorphic system, the conductance of the resistive switching memory cell placed on a cross-point array has multiple states and can be updated and controlled by the input pulse from the neuron circuit. The conductance control of resistive switching is similar to the synaptic weight adjustment in biological synapses in the human nervous system.

Resistive switching and artificial synaptic behaviors are observed in many insulators, such as oxide [11–13], nitride [13–15], organic materials [16], and 2D materials [17]. Among them, metal–oxide-based resistive switching memories such as HfO_2 have proven to have the best resistive switching performances in terms of, e.g., endurance, retention, and variability. Excellent resistive switching has been reported when using metal bottom electrodes [18,19]. HfO_2-based resistive switching memory with ITO electrode can also be used for flexible and transparent electronic devices [20]. On the other hand, the HfO_2-based resistive memory with a silicon bottom electrode has not yet been reported as superior to the metal bottom electrode. However, the metal–oxide–semiconductor structure has other advantages, such as self-rectification and low-power operation. The most effective way to enhance resistive switching is to design multiple dielectric stacks [21]. The use of an oxygen reservoir, such as a TiO_x layer, is popular in metal–oxide-based resistive switching memory. Abundant oxygen vacancies are created in the main resistor for resistive switching. A tunnel barrier, such as SiO_2 and Al_2O_3, with a large band gap, can enhance the resistive switching properties by reducing the operation current and increasing the nonlinearity of the I–V curve in the low-resistance state (LRS) [22,23]. The SiO_2 layer can be easily formed when using silicon substrate as the bottom electrode and different methods such as native oxide, thermal oxide, and chemical vapor deposition (CVD). Another advantage of inserting the tunnel barrier with a high band gap is a reduction in the LRS current [21,22]. To employ the advantageous tunnel barrier in resistive switching, the insulating property of the SiO_2 layer is maintained after the forming and set processes. If the excess electric field is applied on the tunnel barrier with a high compliance current, breakdown of the tunnel barrier can occur. Therefore, the use of a careful device stack design is necessary to ensure a stable tunnel barrier layer; for example, the thicknesses of the tunnel barrier and the main resistor are important. In addition, the dielectric constant should be considered to properly distribute the electric field throughout multiple dielectric layers.

In this work, we fabricated a trilayer (HfO_2/Si_3N_4/SiO_2) resistive switching memory device and demonstrated low current switching by suppressing the current overshoot and nonlinear I–V curves in the LRS. The trilayered dielectric stacks were confirmed via high-resolution transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) before electrical characterization. Through a comparative study with a control group without a Si_3N_4 layer, it was verified that the Si_3N_4 layer can relieve the concentration of the electric field in SiO_2. Finally, we demonstrated the improved synaptic behaviors by achieving gradual conductance control in the trilayer structure compared to the device without a Si_3N_4 layer.

2. Materials and Methods

The Ni/HfO_2/Si_3N_4/SiO_2/Si device was prepared as follows: The ion implantation was conducted in the Si substrate to increase the conductivity on the single crystalline Si surface as the bottom electrode. Phosphorus (P) as an impurity was used to form an n-type Si bottom electrode, where the dose and energy were 5×10^{15} cm^{-2} and 40 keV, respectively. The Si lattice damage caused by ion implantation was cured by the annealing process. Next, a 2.5-nm-thick SiO_2 film was deposited via low-pressure chemical vapor deposition (LPCVD) by reacting SiH_2Cl_2 (40 sccm) and N_2O (160 sccm) at 785 °C after removing native oxide through HF cleaning. Then, a 3.5-nm-thick Si_3N_4 layer was deposited via LPCVD by reacting SiH_2Cl_2 (30 sccm) and NH_3 (100 sccm) at 785 °C. After that, a 3.5-nm-thick HfO_2 layer was deposited by atomic layer deposition (ALD) system by reacting tetrakis (ethylmethylamino) hafnium (TEMAH) and ozone (O_3) at 300 °C. Finally, a 100-nm-thick Ni top electrode was deposited by a thermal evaporator and patterned by a shadow mask containing circular patterns with a diameter of 100 µm. A Ni/HfO_2/SiO_2/Si device was prepared as a control device in the same way, except for the Si_3N_4 layer.

The electrical properties were characterized both in DC mode using a Keithley 4200-SCS semiconductor parameter analyzer (Keithley Instrumnets, Cleveland, OH, USA) and in pulse mode using a 4225-PMU ultrafast module (Keithley Instrumnets, Cleveland, OH, USA) During

the measurements, a bias voltage and pulse were applied to the Ni top electrode, while the Si bottom electrode was grounded. XPS depth analysis was conducted with a Nexsa (ThermoFisher Scientific, Waltham, MA, USA) with a Microfocus monochromatic X-ray source (Al-Kα (1486.6 eV)), a sputter source (Ar+), an ion energy of 1 kV, and a beam size of 100 μm $\times$ 100 μm.

3. Results and Discussion

Figure 1a,b respectively shows the schematics and a TEM image of the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device. Single crystalline Si substrate and amorphous HfO$_2$, Si$_3$N$_4$, and SiO$_2$ layers could be observed in the TEM image. In addition, the TEM image provides information about the exact film thicknesses of HfO$_2$ (3.5 nm), Si$_3$N$_4$ (3.5 nm), and SiO$_2$ (2.5 nm). The energy-dispersive X-ray spectra (EDS) line scan was obtained through scanning transmission electron microscopy (STEM) and is shown in Figure S1. Next, the XPS depth profile of HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si was investigated to determine the elements in each layer. Figure 1c shows the XPS spectra Hf 4f of HfO$_2$ as the first dielectric layer [24]; Hf 4f is typically composed of a 4f 5/2 and 4f 7/2 spin–orbit doublet, which are respectively centered at 20 and 18.5 eV. This result is consistent with existing literature about HfO$_2$ on a Si substrate [24]. Figure 1d shows the Si 2p spectra for the Si$_3$N$_4$ layer, SiO$_2$ layer, and Si substrate. The peak intensity that is located at about 99.5 eV is higher at the deeper etching level (level 11) than it is at level 7. This indicates that the Si substrate is more exposed by X-ray beams at the deeper etching level (level 11) [21]. Moreover, the peak point at etch level 11 is shifted to the right compared to that at etch level 7, indicating that the Si–O bond located at 103.5 eV is increased at level 11 [25]. Figure 1e shows the N 1s spectra at level 7 and level 11, where the peak is centered at about 398 eV [26]. The peak intensity at level 11 is much weaker than that at level 7. This result is consistent with the Si 2p result shown in Figure 1d.
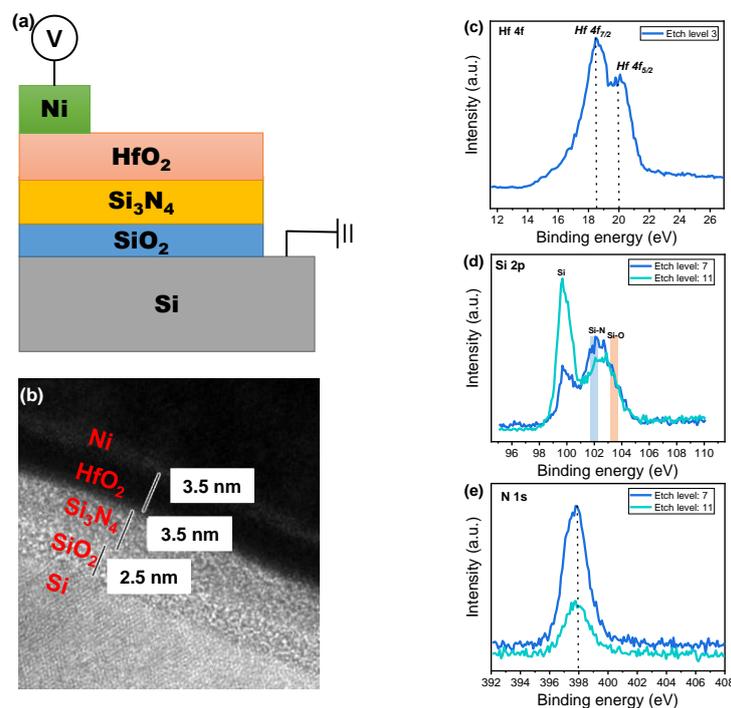

Figure 1. Device configuration and material analysis of the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device. (**a**) Schematic drawing of the device stack; (**b**) TEM image; (**c**) XPS Hf 4f spectra at etch level 3; (**d**) XPS Si 2p spectra at etch levels 7 and 11; and (**e**) XPS N 1s spectra at etch levels 7 and 11.

Figure 2a,b shows the I–V characteristics of the Ni/HfO$_2$/SiO$_2$/Si and Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si devices. For a fair comparison, the compliance current (CC) of 5 μA is applied to both devices. The initial cells are activated with the positive bias DC sweep. The current is significantly increased during the reverse sweep, which indicates that soft breakdown occurs within the dielectrics. The CC

can protect the device from permanent breakdown. Subsequently, the reset process is conducted by the negative bias sweep, causing the state of the device to be changed to the high-resistance state (HRS). This process can be explained by the rupture of the conducting path in dielectrics. Then, the set process follows to make the state of device be the LRS again. The HRS and LRS of the device can be repeatedly switched in the repetitive set and reset process. It should be noted that high current (~10 mA) flows within the $Ni/HfO_2/SiO_2/Si$ device in the LRS. The current is very high despite the fact that 5 µA is applied on the $Ni/HfO_2/SiO_2/Si$ device during the forward and reverse sweep in the LRS under the positive bias. Subsequently, the high LRS current without CC in a negative bias is the real current level. This suggests that current overshoot occurs during the set process, meaning that the LRS current cannot be tightly controlled by CC. An abrupt transition is observed during the reset process, indicating that the conducting path is ruptured at once. The I–V characteristics of the $Ni/HfO_2/Si_3N_4/SiO_2/Si$ device are substantially different from those of the $Ni/HfO_2/SiO_2/Si$ device, as shown in Figure 2b. The LRS current in a negative region is lower than the CC of 5 µA. This implies that the current overshoot is suppressed during the set process at a positive region. The bipolar resistive switching is driven by the temperature and electric field [27–30]. The $Ni/HfO_2/SiO_2/Si$ device shows abrupt reset with high current, indicating that Joule heating is the dominant mechanism of the reset process. On the other hand, the electric field may be more important for the $Ni/HfO_2/Si_3N_4/SiO_2/Si$ device considering the switching at low current.
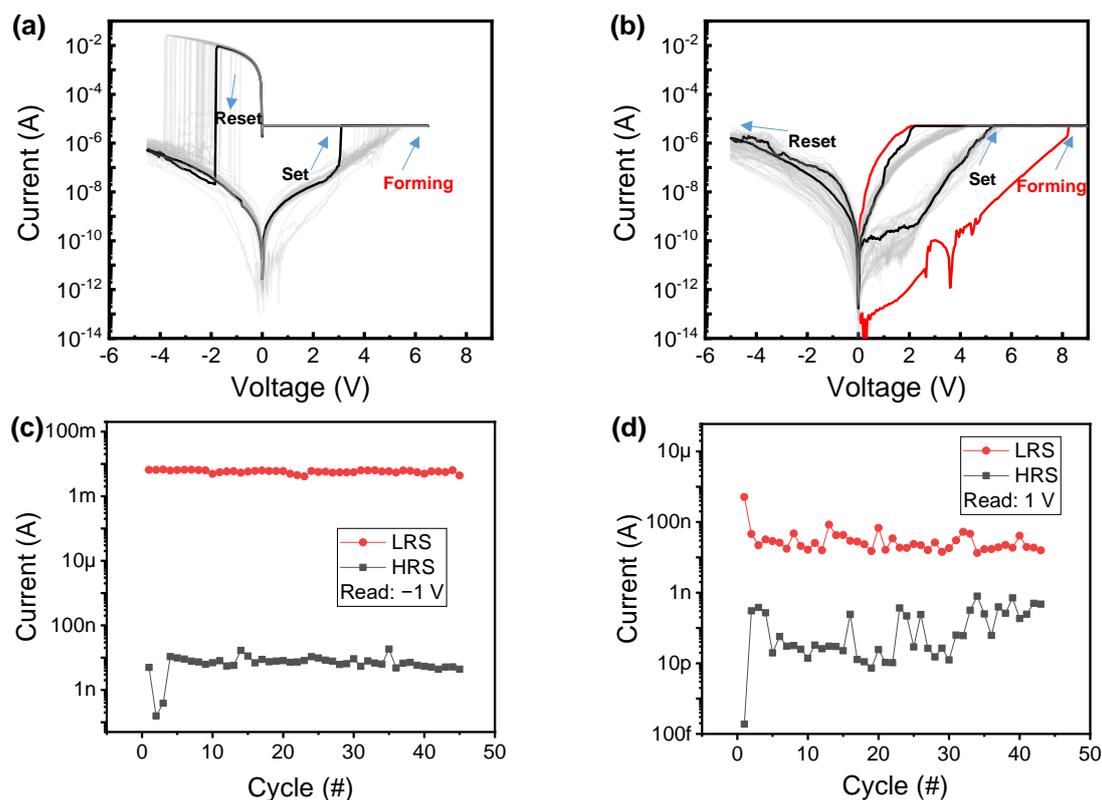

Figure 2. I–V characteristics of the (**a**) $Ni/HfO_2/SiO_2/Si$ device and (**b**) $Ni/HfO_2/Si_3N_4/SiO_2/Si$ device including forming, set, and reset processes; cycling data of I–V characteristics of (**c**) $Ni/HfO_2/SiO_2/Si$ device and (**d**) $Ni/HfO_2/Si_3N_4/SiO_2/Si$ device.

Figure 2c,d shows the cycling trend of the $Ni/HfO_2/SiO_2/Si$ and $Ni/HfO_2/Si_3N_4/SiO_2/Si$ devices, respectively. Time series statistical analysis could provide the indirect information of filament evolution [31,32]. Both HRS and LRS are stable except for the initial few points during the cycling for the $Ni/HfO_2/SiO_2/Si$ device. This indicates that the large size of conducting filament could be uniformly formed and ruptured. On the other hand, the read current of the $Ni/HfO_2/Si_3N_4/SiO_2/Si$

device has larger variation during the cycling, and the read current in the HRS is increased. The larger variation is probably due to the fact that the filaments are formed and ruptured in multiple layers (HfO_2/Si_3N_4/SiO_2), and these formations and ruptures would be quite random processes spatially inside the insulators.

　　Figure 3a shows the statistical distribution of the Ni/HfO_2/SiO_2/Si and Ni/HfO_2/Si_3N_4/SiO_2/Si devices in the LRS and HRS. The LRS resistance of the Ni/HfO_2/Si_3N_4/SiO_2/Si device is much higher than that of the Ni/HfO_2/SiO_2/Si device. However, the variations of the LRS and HRS of the Ni/HfO_2/Si_3N_4/SiO_2/Si device are worsened. Figure 3b shows the ratio between reset current (I_{RESET}) and CC. From this ratio, we can obtain information on how much CC suppresses the overshoot current during the set process. I_{RESET} is rather smaller than CC in the Ni/HfO_2/Si_3N_4/SiO_2/Si device. However, the I_{RESET}/I_{CC} ratio of the Ni/HfO_2/Si_3N_4/SiO_2/Si device is more than 1000. Other advantages of the Ni/HfO_2/Si_3N_4/SiO_2/Si device are its high nonlinear I–V characteristic and its low-current operation. The nonlinearity is defined as the ratio between the current at read voltage (V_{READ}) and the current at half read voltage (1/2·V_{READ}) for the half bias scheme in the cross-point array (Figure S2). Further, the nonlinearity is defined as the ratio between the current at V_{READ} and the current at 1/3·V_{READ} for the 1/3 read scheme. The LRS resistance is the main leakage path in the cross-point array structure when reading the target cell with the HRS. Therefore, the current at 1/2·V_{READ} or the current at 1/3·V_{READ} should be suppressed to reduce crosstalk among the cells. Figure 3c shows the nonlinearity of both devices when applying the 1/2 read scheme and the 1/3 read scheme. The nonlinearities of the Ni/HfO_2/SiO_2/Si device in the LRS are about 2 and 3 for the 1/2 read scheme and the 1/3 read scheme, respectively. This indicates that the LRS follows Ohmic conduction with a slope of 2. The nonlinearity of the Ni/HfO_2/Si_3N_4/SiO_2/Si device in the LRS is substantially higher due to its nonlinear I–V characteristics.
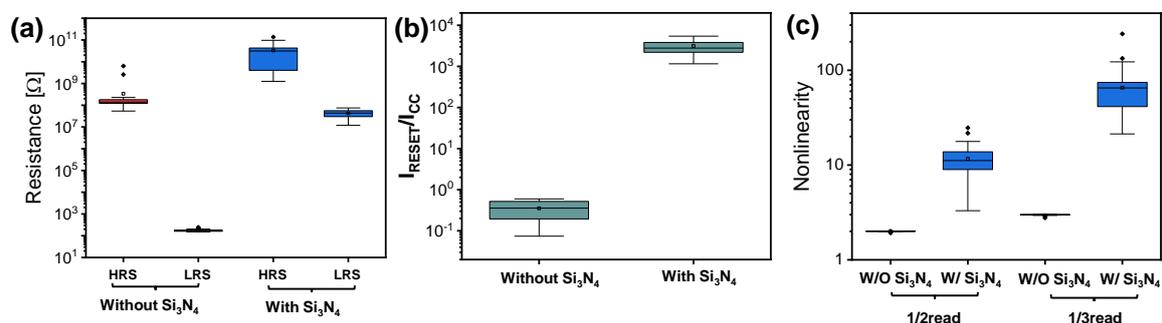

Figure 3. Statistical distributions of (**a**) high-resistance state (HRS) and low-resistance state (LRS) resistance, (**b**) I_{RESET}/I_{CC}, and (**c**) nonlinearity for Ni/HfO_2/SiO_2/Si and Ni/HfO_2/Si_3N_4/SiO_2/Si devices.

　　Figure 4 shows the read margin as a function of the number of word lines for the Ni/HfO_2/SiO_2/Si and Ni/HfO_2/Si_3N_4/SiO_2/Si devices. Here, the 1/2 read scheme and the 1/3 read scheme are applied to a virtual cross-point array without line resistance. The detailed array read schemes are well known in the literature, and we discuss in detail equation and the scheme in Figure S3. The Ni/HfO_2/Si_3N_4/SiO_2/Si device shows higher read margin compared to the Ni/HfO_2/SiO_2/Si device. This is due to the fact that Ni/HfO_2/Si_3N_4/SiO_2/Si has higher LRS resistance and nonlinear I–V curves in the LRS. The read margin at the 1/3 read scheme is also higher than that of the 1/2 read scheme.
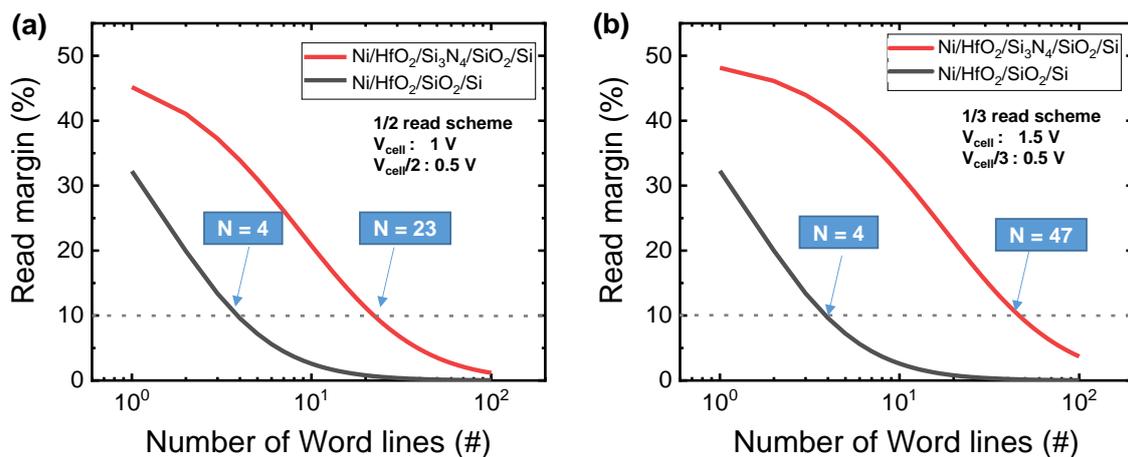
Figure 4. Read margin of Ni/HfO$_2$/SiO$_2$/Si and Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si devices when applying (**a**) 1/2 read scheme and (**b**) 1/3 read scheme in cross-point array.

The conducting path would be formed in the SiO$_2$ layer during the set process for the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device. The electric field is concentrated within the SiO$_2$ layer with consideration of the dielectric constants (HfO$_2$: ~20 and SiO$_2$: ~4). Therefore, high current cannot be avoided in the LRS after the set process. On the other hand, the overshoot current was mitigated in the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device during the set process. This can be explained by the dispersion of the focused electric field of the SiO$_2$ layer due to the Si$_3$N$_4$ layer. The dielectric constant of the Si$_3$N$_4$ layer (Si$_3$N$_4$: ~7) is slightly higher than that of SiO$_2$ and lower than that of HfO$_2$. Therefore, a Si$_3$N$_4$ layer between the HfO$_2$ layer and the SiO$_2$ layer is a good buffer layer to reduce the current overshoot.

Next, we compared the tendency of conductance change as a function of identical pulse during the set and reset process. Figure 5a shows the conductance changes of the Ni/HfO$_2$/SiO$_2$/Si device for potentiation (set process) and depression (reset process), respectively. The pulse amplitude voltages with a pulse width of 450 μs are 6 V and −3.5 V for potentiation and depression, respectively. The conductance values are extracted from the middle point of read pulse (1 V and 450 μs). For potentiation, the conductance value increases abruptly in response to the 18th pulse. The depression curve shows several fluctuations after the first decrease in conductance. Such randomness and abrupt conductance change are not suitable for a hardware-based neuromorphic synaptic device. On the other hand, the conductance values in the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device are gradually controlled by the potentiation and depression pulses (Figure 5b). The voltages of the set pulse and reset pulse are 7 and −4.5 V, respectively, and the pulse width is 450 μs. Further, the read pulse (1 V and 450 μs) is inserted between set pulses or reset pulses to obtain the conductance value. It should be noted that a gradual conductance update is possible when the same pulse is repeatedly applied on the device for potentiation and depression. Moreover, the conductance value of the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device is substantially lower than that of the Ni/HfO$_2$/SiO$_2$/Si device. Therefore, the improved synaptic properties, such as the low energy and multiple conductance, of the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device are beneficial for synaptic applications. The conductance update method of the Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device is suitable for offline learning. To apply it to online learning that provides information by reading conductance values in real time, improvement in variation will be required [33].
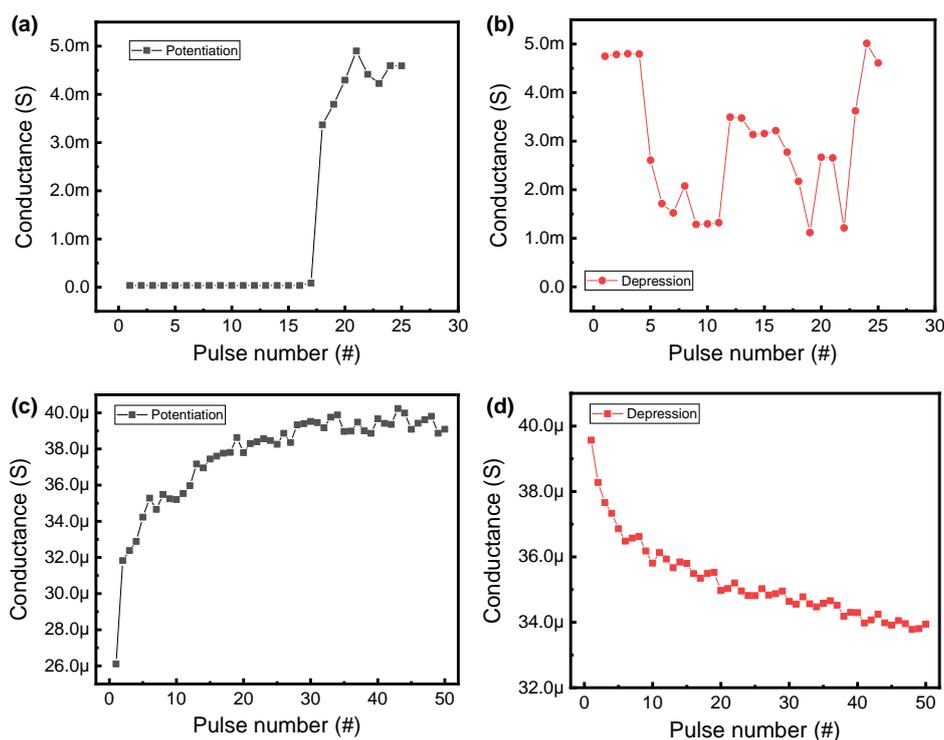
Figure 5. Potentiation and depression characteristics for (**a**,**b**) Ni/HfO$_2$/SiO$_2$/Si device and (**c**,**d**) Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si device.

4. Conclusions

In summary, we fabricated a CMOS-compatible trilayer device (Ni/HfO$_2$/Si$_3$N$_4$/SiO$_2$/Si) and characterized its resistive and synaptic characteristics. The TEM and XPS provide the exact dielectric thickness and chemical information of the trilayer device. The Si$_3$N$_4$ layer could alleviate the concentrated electric field into the SiO$_2$ layer in the trilayer design, so the conducting paths are not formed in all dielectrics in the LRS. This property can reduce reset current and provide a nonlinear I–V curve in the LRS. The high nonlinearity in the trilayer device can enlarge the array size in the cross-point array architecture. Finally, we demonstrated that gradual set and reset switching in a trilayer device can be highly suitable for emulating the synaptic behavior of a biological synapse in the human nervous system by controlling multiple conductance.

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