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Chemical Vapor Deposition Carbon Coating of SiO$_x$ Anode for Li-Ion Batteries: Significance of Carbon Precursor Selection and Deposition Temperature

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ABSTRACT: Owing to the surge in the demand for lithium-ion batteries (LIBs) with high energy density, silicon suboxide (SiO$_x$)-based materials with impressive theoretical capacities have garnered significant attention. However, challenges such as poor electrical conductivity and substantial volume expansion must be overcome. A common strategy for addressing these issues involves coating SiO$_x$ with carbon. During this process, the properties of the carbon layer and SiO$_x$ are strongly affected by the temperature and precursor choice. This study explores the impact of the temperature and precursor selection on the carbon coating layer deposited by chemical vapor deposition (CVD) and the phase of SiO$_x$. Surprisingly, SiO$_x$@C$_2$H$_2$, in which SiO$_x$ was coated with carbon using acetylene at low temperatures, exhibited lower cyclic stability than the uncoated SiO$_x$. In contrast, SiO$_x$@CH$_4$, in which SiO$_x$ was coated with carbon at high temperatures, comprised a vertically grown carbon layer and SiO$_2$ layer with optimal thickness. This configuration stabilized the growth of the solid electrolyte interphase (SEI) layer and enhanced the electrical contact. The optimized SiO$_x$@CH$_4$-1000 (methane-based CVD coating at 1000 °C) demonstrated excellent electrochemical performance, achieving a high capacity of 778 mAh g^{-1} at 0.75 A g^{-1} and a remarkable capacity retention of 92.8% after 100 cycles. This optimized CVD carbon coating process paves the way for industrialization of SiO$_x$-based materials, positioning them for application in next-generation LIBs.
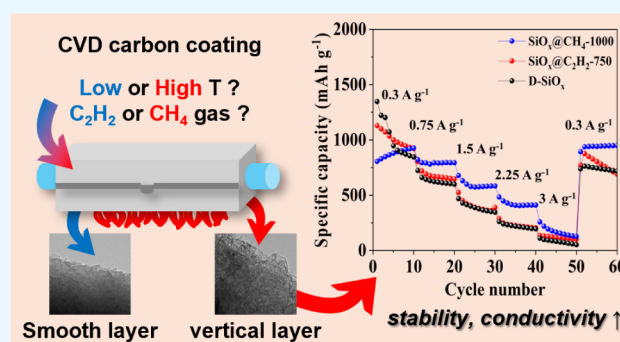
1. INTRODUCTION

Recently, the demand for high-energy-density Li-ion batteries (LIBs) has increased significantly. The adoption of silicon (Si)-based materials is widely recognized as a practical and effective strategy for improving the energy density and specific energy of LIBs.[1−3] This is because of the remarkable theoretical capacity of these materials, which surpasses those of transition metal oxides and organic-based anode materials. The theoretical capacities of silicon dioxide (SiO$_2$), silicon monoxide (SiO), and Si are ∼1963, 2675, and 4200 mAh g^{-1}, respectively. Among Si-based materials, silicon suboxide (SiO$_x$) is considered a promising alternative anode material owing to its excellent cyclic stability and theoretical specific capacity.[4] Because SiO$_x$ is thermodynamically unstable, it readily undergoes phase separation into crystalline Si nanoparticles with nanosized crystal grains and an amorphous SiO$_2$ matrix during annealing. This characteristic results in a high reversible capacity during battery cycling because amorphous SiO$_2$ effectively mitigates volume changes during cycling.[5] However, SiO$_x$ suffers from volume expansion and low conductivity during cycling.[6,7] To overcome these problems, considerable effort has been dedicated to coating the surface of SiO$_x$ with a carbon layer. The objective of this strategy is to mitigate the

volume expansion of SiO$_x$ during cycling, enhance the electrical conductivity, and thereby stabilize the generated solid electrolyte interphase (SEI) layer.[8,9] Notably, chemical vapor deposition (CVD) is an effective large-scale manufacturing method for applying uniform carbon layers to active materials. However, the high temperature required for the CVD carbon coating process remains a significant obstacle that increases the process costs. To address this challenge, researchers have explored various process conditions for reducing the CVD temperature.[10−13] Importantly, the electrochemical and physical properties of SiO$_x$ and the carbon layer change with temperature variations.[14,15]
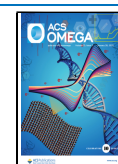
In this study, we explore the effects of the carbon source and temperature on the CVD process. The electrochemical and physical properties of carbon coated SiO$_x$ using acetylene gas at relatively low temperatures and carbon coated SiO$_x$ using

methane gas at high temperatures are evaluated. The use of methane results in the formation of a vertically grown carbon coating layer, whereas the use of acetylene produces a smooth carbon layer. The vertically grown carbon layer increases physical contact points between particles, offering enhanced electron transport pathways and maintaining interparticle contact, even during significant volume changes in the active material. In contrast, the smooth carbon layer reduces the surface area of the active material, which reduces the likelihood of electrolyte decomposition. These morphological and functional differences are determined by the carbon source. Furthermore, variations in temperature induce changes in the degree of SiO_x disproportionation, which affects the cycling stability of SiO_x. The process conditions for coating SiO_x with carbon via CVD are optimized by considering these variables, and thus the findings provide valuable insights into maintaining a balance between enhancing the performance and ensuring the cost-effectiveness of LIBs.

2. EXPERIMENTAL SECTION

2.1. CVD Synthesis of $SiO_x@C_2H_2$ and $SiO_x@CH_4$. Disproportionated SiO_x microparticles (D-SiO_x; Dae Joo Electronic Materials, South Korea) with an average diameter of 5 μm were dispersed in an alumina crucible and placed in a tube furnace. The tube furnace was purged at a flow rate of 300 sccm with Ar gas (99.99 mol %), followed by heating to different temperatures using acetylene at 650, 700, 750, and 800 °C, and methane at 900, 950, 1000, and 1050 °C, at a pressure of 0.1 kPa at a rate of 8 °C min^{-1}. The samples were subsequently annealed in a gaseous mixture of Ar (300 sccm) and acetylene or methane (132 sccm) for 1 h. Thereafter, the gas mixture was replaced with Ar, and the system was purged with Ar for 1 h, followed by cooling to room temperature. The products obtained with acetylene and methane are denoted as $SiO_x@C_2H_2$-X and $SiO_x@CH_4$-X, respectively, where X represents the CVD process temperature.

2.2. Physical Characterization. Field-emission scanning electron microscopy (FE-SEM, S-4300, Hitachi) and field-emission transmission electron microscopy (FE-TEM, JEM-2100F, JEOL) were used to analyze the morphologies of D-SiO_x, $SiO_x@CH_4$, and $SiO_x@C_2H_2$, and their microstructures, respectively. The crystal structures of D-SiO_x, $SiO_x@C_2H_2$, and $SiO_x@CH_4$ were evaluated by X-ray diffraction (XRD, DMAX 2200 V PC, Rigaku, at the Core-Facility Center for Sustainable Energy Materials of KBSI) with Cu−Kα radiation (1.54056 Å). Thermogravimetric analysis (TGA; Diamond TG/DTA, PerkinElmer) was used to estimate the mass loading of the carbon coating layer on SiO_x under an air atmosphere at 30−800 °C and a heating rate of 10 °C min^{-1}.

2.3. Cell Assembly and Electrochemical Measurement. The prepared D-SiO_x, $SiO_x@C_2H_2$, and $SiO_x@CH_4$ active materials, a conducting agent (Super P), and a poly(acrylic acid) (PAA) binder were mixed in a weight ratio of 8:1:1 and dispersed in deionized (DI) water to form a slurry. The obtained slurry was homogeneously coated onto a Cu foil current collector and dried in a vacuum oven at 80 °C for 12 h. A circle with a diameter of 14 mm was punched out and used as the working electrode. The areal mass loading of the prepared electrodes was approximately 2.0 mg/cm^{-2}. Electrochemical measurements were performed in a half-cell configuration using CR2032-type coin cells assembled in an Ar-filled glovebox in which the oxygen and water contents were maintained below 0.1 ppm. Metallic Li was used as the

counter electrode, Celgard 2400 as the separator, 1 M LiPF$_6$ in EC/DEC (1:1 v/v) as the electrolyte, and fluoroethylene carbonate as the electrolyte additive. The galvanostatic charge/discharge cycle performance was evaluated using a battery cycler system (WBCS 3000, WonATech) at a current density of 0.15−3 A g^{-1}. Cyclic voltammetry (CV) was conducted using a potentiostat/galvanostat (SP-150, Bio-Logic) in the range of 0.01−2.0 V (vs Li/Li$^+$) at a scan rate of 0.1 mV s^{-1}. Electrochemical impedance spectroscopy (EIS) was conducted using an electrochemical workstation (Autolab PGSTAT128N, Metrohm) in the frequency range of 1 MHz to 0.01 Hz.

3. RESULTS AND DISCUSSION

TGA was used to confirm the effect of the change in the CVD process temperature and carbon precursor on the amount of the carbon coating deposited. The samples were heated under an air atmosphere from 30 to 800 °C at a rate of 10 °C min^{-1}. Figure 1a,b indicate the TGA curves of $SiO_x@C_2H_2$ and
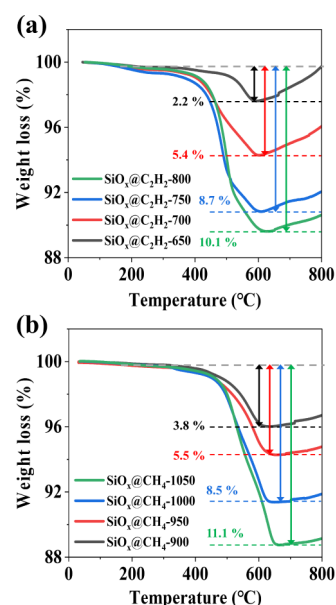
Figure 1. TGA profiles of (a) $SiO_x@C_2H_2$ and (b) $SiO_x@CH_4$, prepared at different deposition temperatures.

$SiO_x@CH_4$ synthesized at different temperatures. The slight weight loss below 200 °C during heating is attributed to the removal of surface water. In contrast, the significant weight loss between 400 and 600 °C indicates the decomposition of the carbon coating layer. Above 600 °C, an increase in weight is observed for all samples due to the oxidation of SiO_x to SiO_2.[16,17] From Figure 1a, the amounts of carbon coating in $SiO_x@C_2H_2$-650, $SiO_x@C_2H_2$-700, $SiO_x@C_2H_2$-750, and $SiO_x@C_2H_2$-800 are estimated to be 2.2, 5.4, 8.7, and 10.1%, respectively. From Figure 1b, the amounts of carbon coating in $SiO_x@CH_4$-900, $SiO_x@CH_4$-950, $SiO_x@CH_4$-1000, and $SiO_x@CH_4$-1050 are estimated to be 3.8%, 5.5%, 8.5%, and 11.1%, respectively. The CVD process using the acetylene precursor requires a 250 °C less temperature for obtaining a similar amount of carbon coating compared to the temperature required with the methane precursor.

Figure 2 shows TEM and energy-dispersive spectroscopy (EDS) mapping images of D-SiO_x, $SiO_x@C_2H_2$, and $SiO_x@CH_4$. In Figure 2a, the TEM image and EDS map of D-SiO_x indicate a smooth surface with a low carbon content. After
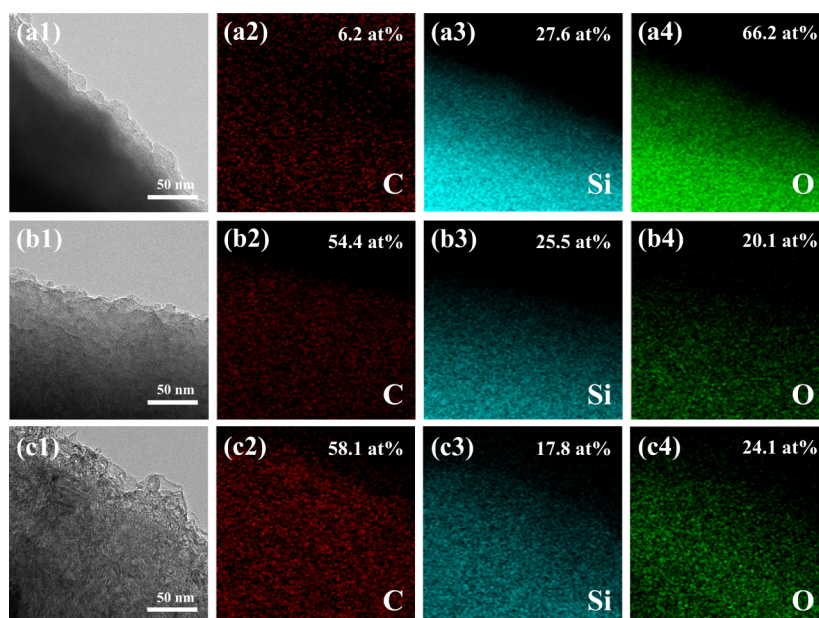
Figure 2. TEM images and EDS maps of (a) D-SiO$_x$, (b) SiO$_x$@C$_2$H$_2$-750, and (c) SiO$_x$@CH$_4$-1000.

CVD using different carbon precursors (Figure 1), EDS mapping reveals that SiO$_x$@C$_2$H$_2$-750 and SiO$_x$@CH$_4$-1000 exhibit similar carbon contents of 54.4% and 58.1%, respectively. The carbon layer of SiO$_x$@C$_2$H$_2$ has a relatively smooth surface (Figure 2b). Despite the similar amount of carbon deposited on the surface from both carbon precursors, the carbon layer grown on SiO$_x$@CH$_4$ exhibits a vertically grown structure (Figure 2c). In addition, Figure S1 shows the thickness of the carbon layer of D-SiO$_x$, SiO$_x$@C$_2$H$_2$-750, and SiO$_x$@CH$_4$-1000. The thickness of the carbon layer for SiOx@C$_2$H$_2$ and SiO$_x$@CH$_4$ is 25 and 33 nm, respectively. Due to the vertically grown carbon layer, SiO$_x$@CH$_4$ shows a thicker carbon layer than SiO$_x$@C$_2$H$_2$.

Due to its unstable triple bond, the decomposition energy (ΔH) of acetylene is lower than that of methane. The ΔH values for the decomposition of acetylene and methane are presented in the following equations:

$$CH_4 \rightarrow CH_3 + \dot{H} \cdots \rightarrow C + 2H_2 \quad \Delta H = 75.6 \text{ kJ mol}^{-1}$$
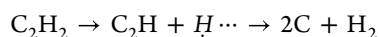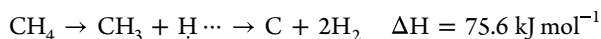
$$C_2H_2 \rightarrow C_2H + \dot{H} \cdots \rightarrow 2C + H_2$$
$$\Delta H = -54.3 \text{ kJ mol}^{-1}$$

Therefore, the deposition of carbon via CVD proceeds at a relatively low temperature with acetylene compared to that with methane because of the low decomposition energy of acetylene.[18] Figure S2 shows the morphological characteristics of D-SiO$_x$, SiO$_x$@C$_2$H$_2$, and SiO$_x$@CH$_4$. Similar to the polyhedral particles of D-SiO$_x$ (Figure S2a), the particles of SiO$_x$@C$_2$H$_2$ (Figure S2b−e) and SiO$_x$@CH$_4$ (Figure S2f−i) are also polyhedral with comparable diameters. Owing to the deposition of the carbon layer on SiO$_x$, the surfaces of SiO$_x$@C$_2$H$_2$ and SiO$_x$@C$_2$H$_4$ become rough. As the deposition temperature increases for both carbon precursors, the surface roughness becomes more pronounced. The TEM images of SiO$_x$@C$_2$H$_2$ and SiO$_x$@CH$_4$ (Figure S3) show distinctively different morphologies of the carbon-coated layers. The SiO$_x$@C$_2$H$_2$ samples have a relatively smooth carbon layer (Figure S3a−d), whereas the SiO$_x$@CH$_4$ samples have vertically grown

carbon layers, except for SiO$_x$@CH$_4$-900 (Figure S3e−h). The vertically grown carbon layer on SiO$_x$@CH$_4$ promotes better electrical contact, stabilizing the formation of the SEI layer during cycling.[4,19,20] Therefore, compared to acetylene, the utilization of methane as a carbon precursor is expected to enhance the electrochemical performance of the composite. The properties of the carbon coating layer were evaluated using Raman spectroscopy (Figure 3a,b). In the Raman spectrum, the peaks at 480 and 520 cm^{-1} are attributed to amorphous and crystalline Si, respectively.[21] Under high
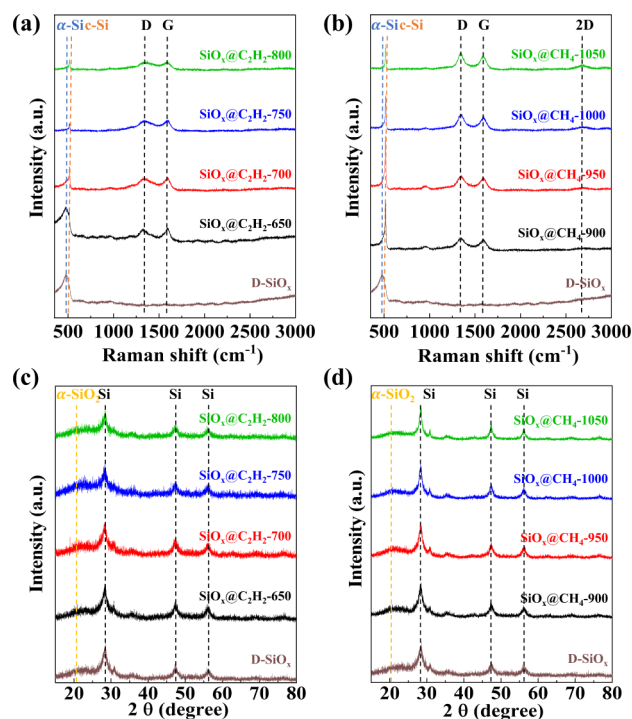
Figure 3. Physical characterization of D-SiO$_x$, SiO$_x$@C$_2$H$_2$, and SiO$_x$@CH$_4$ synthesized at different CVD temperatures: (a, b) Raman spectra and (c, d) XRD patterns.

temperatures, such as during the CVD process, the crystallinity of silicon increases, and the grain size grows, with these effects being more pronounced at higher temperatures.[22] This trend is evident in the behavior of D-SiO$_x$, where the amorphous silicon originally present is still observed in SiO$_x$@C$_2$H$_2$-650 at 650 °C. However, at higher temperatures, the amorphous silicon in D-SiO$_x$ transforms significantly into crystalline silicon, with the crystalline Si peak intensity increasing as the temperature rises. As the amount of carbon coating on SiO$_x$@ C$_2$H$_2$ and SiO$_x$@CH$_4$ increases, the intensity of the Si peak exhibits a decreased intensity. Distinctive peaks associated with graphene (D, G, and 2D bands) are detected for SiO$_x$@C$_2$H$_2$ and SiO$_x$@CH$_4$, revealing the state of the carbon coating layer. The 2D band is detected only for the samples treated at >950 °C. Typically, an I_G/I_{2D} ratio surpassing 1.3 suggests the existence of three or more graphene layers.[23] The I_G/I_{2D} values calculated for SiO$_x$@CH$_4$-950, SiO$_x$@CH$_4$-1000, and SiO$_x$@ CH$_4$-1050 are 1.66, 1.65, and 1.52, respectively (Figure 3b). Therefore, SiO$_x$@CH$_4$-950, SiO$_x$@CH$_4$-1000, and SiO$_x$@CH$_4$-1050 samples exhibit multilayered graphene structures with almost the same number of graphene layers. Conversely, the I_D/I_G ratios of SiO$_x$@C$_2$H$_2$ and SiO$_x$@CH$_4$ are comparable (Table S1). This suggests that the properties of the carbon layers are almost the same. The XRD patterns of D-SiO$_x$, SiO$_x$@C$_2$H$_2$, and SiO$_x$@CH$_4$ reveal broad peaks, indicating the presence of amorphous SiO$_2$ (Figure 3c,d) in the 2θ range of 18−26°. The (311), (220), and (111) peaks of crystalline Si in the XRD patterns of D-SiO$_x$, SiO$_x$@C$_2$H$_2$, and SiO$_x$@CH$_4$ are assigned to the partial disproportionation of SiO into Si and SiO$_2$.[5] This process contributes to the improved cyclic stability by inducing embedding of the Si particles in the SiO$_2$ matrix, thereby mitigating volume expansion. With an increase in the CVD process temperature, the disproportionation reaction is promoted, leading to a higher intensity of the characteristic Si peak and a decrease in the intensity of the peak of amorphous SiO$_2$.[21,24] This phenomenon can be confirmed by the change in the size of the Si crystallites in the SiO$_x$ matrix. The size of the Si crystal grains in the SiO$_x$ matrix was calculated using the following equation:

$$L = \frac{K\lambda}{\beta \cdot \cos\theta}$$

In this equation, L represents the crystal size, K represents the Scherrer factor, λ represents the X-ray wavelength, β represents the full-width-half-maximum value of the specific XRD peak, and θ represents the Bragg diffraction angle. The calculated Si crystal sizes are given in Table S2. In SiO$_x$@CH$_4$, phase separation progressed more extensively than in D-SiO$_x$ due to the high temperature during CVD, resulting in larger Si crystal sizes (the average Si crystal sizes were 6.5 and 8.1 nm for SiO$_x$@C$_2$H$_2$ and SiO$_x$@CH$_4$, respectively). Conversely, in the case of SiO$_x$@C$_2$H$_2$, the lower CVD temperature prevented further phase separation, resulting in Si crystal sizes similar to those observed for D-SiO$_x$.[14,25,26]

Half-cell tests were conducted to investigate the effects of different carbon precursors and CVD temperatures on cycling performance (Figure 4). As shown in Figure 4a, the cycling performance of the SiO$_x$@C$_2$H$_2$ electrodes improves with an increase in the CVD temperature; however, the capacity fading is significant compared to that of the SiO$_x$@CH$_4$ electrodes (Figure 4b). After 100 cycles, SiO$_x$@C$_2$H$_2$-650, SiO$_x$@C$_2$H$_2$-700, SiO$_x$@C$_2$H$_2$-750, and SiO$_x$@C$_2$H$_2$-800 afford capacities of 38, 34, 57, and 178 mAh g^{-1}, respectively. After 100 cycles
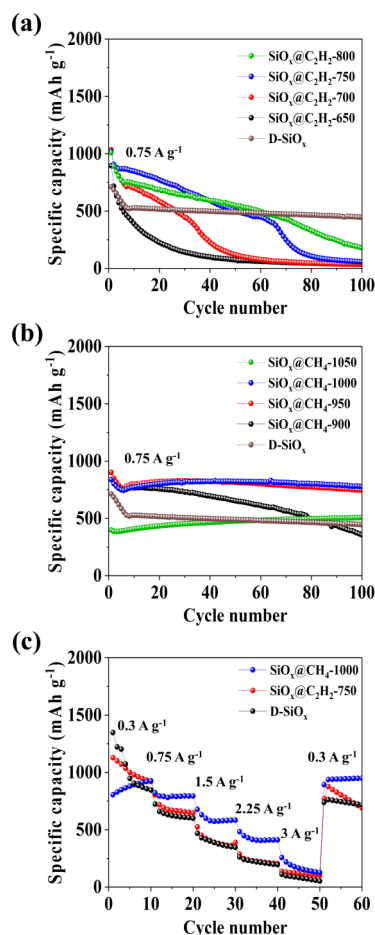
Figure 4. Cycling performance at 0.75 A g^{-1} for 100 cycles: (a) SiO$_x$@C$_2$H$_2$ and (b) SiO$_x$@CH$_4$ synthesized at different CVD temperatures. (c) Rate performance of D-SiO$_x$, SiO$_x$@C$_2$H$_2$-750, and SiO$_x$@CH$_4$-1000 at 0.3−3.0 A g^{-1}.

(Figure 4b), the discharge capacities of SiO$_x$@CH$_4$-900, SiO$_x$@C$_2$H$_2$-950, SiO$_x$@C$_2$H$_2$-1000, and SiO$_x$@C$_2$H$_2$-1050 are 356, 746, 778, and 508 mAh g^{-1}, respectively. The cycling stability of SiO$_x$@CH$_4$ improves with increasing CVD temperature. SiO$_x$@CH$_4$-1050 affords a low capacity but maintains good capacity retention due to the thick SiO$_2$ layer formed during the high temperature process. However, the capacity gradually increases as cycling continues because SiO$_x$@CH$_4$-1050 overcomes the overpotential barrier.[27] SiO$_x$@CH$_4$-1000 exhibits the highest performance among all of the samples after 100 cycles because of the appropriate amount of the vertical carbon coating layer and disproportionation of SiO$_x$. To further confirm the remarkable capacity retention of SiO$_x$@CH$_4$-1000, a comparison of the reported Si-based electrode is shown in Table S3. It is demonstrated that the capacity retention of SiO$_x$@CH$_4$-1000 is competitive. Figure 4c shows the rate performances of D-SiO$_x$, SiO$_x$@C$_2$H$_2$-750, and SiO$_x$@CH$_4$-1000 at various current densities. The discharge capacity of SiO$_x$@CH$_4$-1000 is higher than that of D-SiO$_x$ and SiO$_x$@C$_2$H$_2$-750 at different rates, excluding the initial 0.3 A g^{-1}. Moreover, when the current density returns to 0.3 A g^{-1}, SiO$_x$@CH$_4$-1000 shows excellent capacity retention and nearly fully recovers its capacity, in contrast to D-SiO$_x$ and SiO$_x$@C$_2$H$_2$-750. The enhanced performance of SiO$_x$@CH$_4$ can be attributed to the following reasons: Despite the comparable amount of carbon coating, the utilization of

methane as the carbon precursor results in the vertical growth of the carbon layer. This vertical carbon layer enhances the electrical conductivity, with numerous contact points, and stabilizes the growth of the SEI layer,[19,20] collectively contributing to improved long-term stability. By heat-treating at the same temperature of 1050 °C with acetylene and methane, we have excluded the effects of silicon disproportionation, allowing us to focus solely on the impact of carbon layer morphology. As shown in Figure S4, although the large surface area of the vertically grown carbon layer leads to a lower initial capacity, $SiO_x@CH_4$-1050 demonstrates significantly enhanced stability over 100 cycles compared to D-SiO_x and $SiO_x@C_2H_2$-1050. Additionally, the high deposition temperature causes further disproportionation of SiO_x, and the appropriate thickness of the SiO_2 layer stabilizes the surface of SiO_x.[27] The degree of disproportionation of SiO_x and the relative thickness of the SiO_2 layer are shown in Figure S5 and Table S4. The XPS depth profiles indicate the Si^{4+} peak of $SiO_x@CH_4$ dominates, with a ratio of Si^{4+}/Si^0 5.96, compared to $SiO_x@C_2H_2$, which is only 3.30. It means that the thicker SiO_2 matrix was formed on the surface of $SiO_x@CH_4$, resulting in improved performances. As shown in Figure S6a−c, the Coulombic efficiency of $SiO_x@C_2H_2$-750 is approximately 90% at the 36th cycle; thereafter, the specific capacity decreases significantly. In contrast, D-SiO_x and $SiO_x@CH_4$-1000 exhibit high Coulombic efficiencies during long-term cycling.

CV was performed to evaluate the electrochemical properties of D-SiO_x, $SiO_x@C_2H_2$, and $SiO_x@CH_4$ at a scan rate of 0.1 mV s^{-1}. They exhibited cathodic peaks in the range of 0.01−0.2 V and anodic peaks at 0.3−0.5 V (Figure 5), indicating the lithiation and delithiation of SiO_x. As the number of cycles increased, the anodic and cathodic currents of all samples increased due to the activation of the materials during lithiation and delithiation.[28] This activation process is due to significant volume changes in silicon, which modify lithium-ion channels and expose more active silicon sites. When these changes occur positively—enhancing ion transport and increasing the accessibility of active silicon—they improve battery performance, a phenomenon referred to as activation. The process occurs gradually over multiple cycles as repeated lithiation and delithiation progressively optimize the structure of the Si and SiO_2 matrix mixture, enhancing the overall effectiveness and stability of the active silicon. Compared with D-SiO_x and $SiO_x@C_2H_2$-750, the redox current for $SiO_x@CH_4$-1000 was significantly lower. This can be attributed to the high annealing temperature of $SiO_x@CH_4$-1000; under these conditions, significant phase separation occurred and a thick insulating SiO_2 layer was formed.[20,29] The CV profile of $SiO_x@CH_4$-1000 in the third cycle indicates a small redox potential difference (ΔE_p: 0.50 V), with high redox currents after five activation cycles (Figure S7), indicating that the redox reaction occurs more actively and faster than in the other samples.[27] This reduction in overpotential is not related to the activation of silicon but results from the influence of the carbon coating layer. In the case of SiO_x-CH_4-1000, the vertically grown carbon layer creates a conductive network that lowers the electrical resistance and enhances the charge transfer, thereby improving the overall conductivity. As a result, redox reactions are accelerated, and the rate capability of the electrode is improved, minimizing energy losses during cycling. It is important to note that this effect is independent of silicon activation and is solely due to the enhanced electron transport provided by the carbon coating.
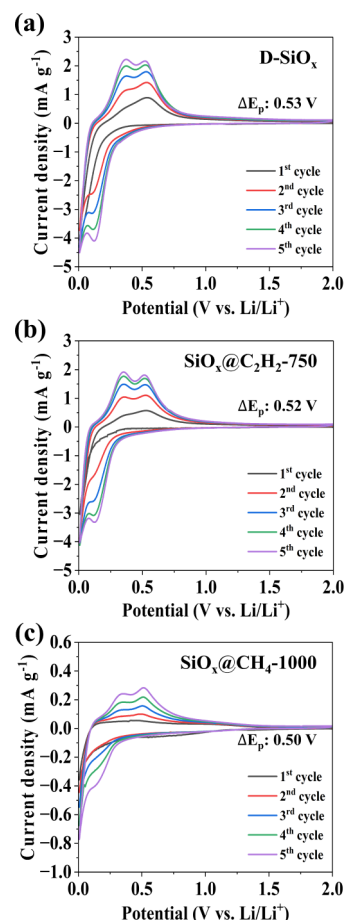

Figure 5. Cyclic voltammograms of (a) D-SiO_x, (b) $SiO_x@C_2H_2$-750, and (c) $SiO_x@CH_4$-1000 in the potential range of 0.01−2.0 V (vs Li/Li$^+$) at a scan rate of 0.1 mV s^{-1}.

EIS was used to study the electrochemical kinetics of the electrodes. Figure 6 shows the Nyquist plots of D-SiO_x, $SiO_x@$
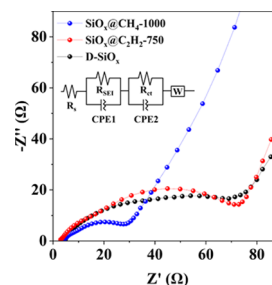
Figure 6. Nyquist plots and the corresponding equivalent circuit of D-SiO_x, $SiO_x@C_2H_2$-750, and $SiO_x@CH_4$-1000 after five activation cycles.

C_2H_2-750, and $SiO_x@CH_4$-1000 after the activation cycles and the corresponding equivalent circuits. The detailed resistance values obtained from the fitted curves are given in Table S5. D-SiO_x exhibits the highest SEI resistance (R_{SEI}) and charge transfer resistance (R_{ct}) of 31.14 and 67.26 Ω, respectively, owing to the large volume expansion and intrinsically low electrical conductivity of SiO_x. The R_{ct} of $SiO_x@CH_4$-1000 (29.08 Ω) is lower than that of $SiO_x@C_2H_2$-750 (66.76 Ω), indicating that the vertically grown carbon layer on $SiO_x@CH_4$-1000 significantly improves the electrical conductivity
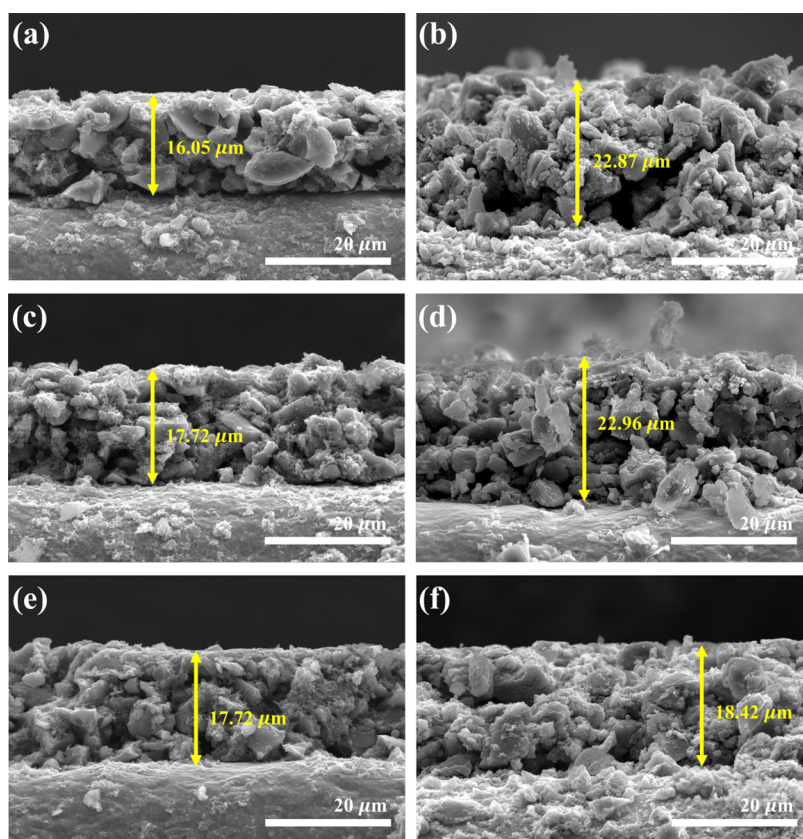
Figure 7. Cross-sectional SEM images (a) before and (b) after 30 cycles for D-SiO$_x$, (c) before and (d) after 30 cycles for SiO$_x$@C$_2$H$_2$-750, and (e) before and (f) after 30 cycles for SiO$_x$@CH$_4$-1000.

compared to the smooth carbon layer on SiO$_x$@C$_2$H$_2$-750. The lowest R_{SEI} value for SiO$_x$@CH$_4$-1000 (3.23 Ω) indicates that the vertical carbon layer effectively stabilizes the surface and prevents the subsequent growth of the SEI layer. In accordance with Figure 6, the Nyquist plots of D-SiO$_x$, SiO$_x$@ C$_2$H$_2$-750, and SiO$_x$@CH$_4$-1000 after 100 cycles (Figure S8) indicate that SiO$_x$@CH$_4$ has the lowest resistance value. Additionally, the Nyquist plots of all D-SiO$_x$, SiO$_x$@C$_2$H$_2$, and SiO$_x$@CH$_4$ electrodes are shown in Figure S9. As shown in Figure S9b, the SiO$_x$@CH$_4$ samples generally exhibit lower resistance compared to D-SiO$_x$ and SiO$_x$@C$_2$H$_2$. It demonstrates that the vertically grown carbon layer on the surface of SiO$_x$@CH$_4$ serves as a buffer layer, unlike the smooth carbon layer of SiO$_x$@C$_2$H$_2$.

The SEM images in Figure 7 show the structural durability of the electrodes after 30 cycles. After cycling, the electrode thickness of D-SiO$_x$ (Figure 7b) increases significantly compared to that of the carbon-coated SiO$_x$ samples, such as SiO$_x$@C$_2$H$_2$ (Figure 7d) and SiO$_x$@CH$_4$ (Figure 7f). The expansion rates of D-SiO$_x$, SiO$_x$@C$_2$H$_2$-750, and SiO$_x$@CH$_4$-1000 are 42.5%, 29.6%, and 3.9%, respectively, demonstrating that the vertically grown carbon layer on SiO$_x$@CH$_4$-1000 acts as a more effective buffer than the smooth carbon layer on SiO$_x$@C$_2$H$_2$-750.

4. CONCLUSIONS

To achieve improved performance and cost-effective anodes for LIBs, carbon-coated SiO$_x$ was synthesized via CVD using two distinct carbon precursors, acetylene and methane. Because of its unstable triple bond, acetylene has a low decomposition energy, allowing deposition of the carbon

coating even at relatively low temperatures. The samples synthesized using acetylene as a precursor exhibited a similar content of coated carbon at temperatures 250 °C lower than those using methane precursors. However, the SiO$_x$@C$_2$H$_2$ samples synthesized using the acetylene precursor at a low temperature (below 800 °C) exhibited low cycling stability due to two drawbacks: the inhibition of the further phase disproportionation of SiO$_x$ and the hindered vertical growth of the carbon coating layer. In contrast, the disproportionation of SiO$_x$ at high temperatures influenced the cycling stability of SiO$_x$@CH$_4$, resulting in the formation of a thick SiO$_2$ layer. In addition, SiO$_x$@CH$_4$ exhibited high electrical conductivity due to the vertically grown carbon layer, which increased electrical contact between particles, stabilized SEI layer growth, enhanced electron transport pathways, and thereby lowered cell overpotential. The optimized SiO$_x$@CH$_4$-1000 electrode showed remarkable cycling performance over 100 cycles, with the highest specific capacity of 778 mAh g^{-1}, resulting from the vertically grown carbon layer and the optimized thickness of the SiO$_2$ layer, which alleviated the volume change. These findings provide insights into the synthesis and design of carbon-coated SiO$_x$-based anodes for high-capacity LIBs.

■ ASSOCIATED CONTENT

ⓢ Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.4c06951.

> TEM and SEM images of D-SiO$_x$, SiO$_x$@C$_2$H$_2$, and SiO$_x$@CH$_4$ at different CVD temperatures; Si 2p XPS depth profiles, Coulombic efficiency, cyclic voltammo-

grams, Nyquist plots with equivalent circuits, and resistance measurements for D-SiO$_x$, SiO$_x$@C$_2$H$_2$-750, and SiO$_x$@CH$_4$-1000; calculated I_D/I_G and I_G/I_{2D} values, crystal sizes of silicon, and electrochemical properties of Si-based electrodes under varying synthesis conditions; Si oxidation states and Si^{4+}/Si^0 ratios from XPS depth profiles (PDF)

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