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Letter

# Semiconductor Epitaxy in Superconducting Templates

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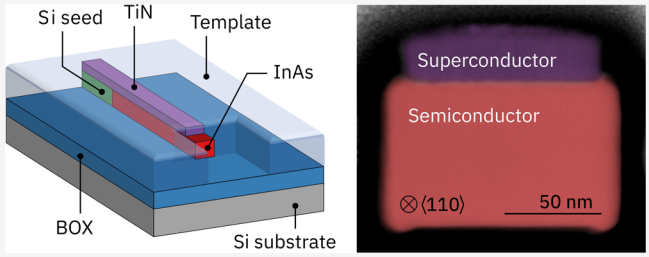
**ABSTRACT:** Integration of high-quality semiconductor−superconductor devices into scalable and complementary metal-oxide-semiconductor compatible architectures remains an outstanding challenge, currently hindering their practical implementation. Here, we demonstrate growth of InAs nanowires monolithically integrated on Si inside lateral cavities containing superconducting TiN elements. This technique allows growth of hybrid devices characterized by sharp semiconductor−superconductor interfaces and with alignment along arbitrary crystallographic directions. Electrical characterization at low temperature reveals proximity induced superconductivity in InAs via a transparent interface.




**KEYWORDS:** *Semiconductor−superconductor hybrids, semiconductor epitaxy, template-assisted selective epitaxy, indium arsenide (InAs), titanium nitride (TiN)*

Hybrid semiconductor−superconductor nanostructures are promising candidates for next generation quantum devices as gate-tunable couplers,[1,2] superconducting qubits,[3,4] Andreev qubits[5−8] and qubits based on Majorana zero modes.[9,10] Their applications rely on highly transparent semiconductor−superconductor interfaces, a milestone first achieved by the epitaxial growth of Al on InAs nanowires (NWs)[11,12] and later on 2D electron gases.[13,14] In recent pioneering approaches, large gap elemental superconductors such as Nb, Ta, V, Sn, and Pb[15−19] were coupled to semiconductor NWs via transparent interfaces. These approaches allow exquisite control of the hybrid interface and are compatible with elaborate shadow epitaxy techniques,[20] but they are challenging to scale and difficult to integrate in a complementary metal-oxide-semiconductor (CMOS) architecture.

Here we demonstrate a different approach in which the order of semiconductor epitaxy and superconductor deposition is reversed. A crystalline semiconductor is grown inside an insulating $SiO_2$ template cavity which features integrated superconducting elements, resulting in flat semiconductor−superconductor hybrid interfaces. This technique is scalable and CMOS compatible, as it is based on the template-assisted selective epitaxy (TASE) platform[21−24] where III−V semiconductors are grown inside insulating cavities. In recent years the TASE approach enabled dense integration of III−V nanowires on Si,[21] growth in branched geometries,[25] and ballistic transport over hundreds of nanometers.[26] Since our approach involves formation of a superconductor−semiconductor interface, we refer to it here as hybrid-TASE.

In this work we introduce hybrid-TASE with InAs nanowires (NWs) and the superconductor TiN. Nanowires are aligned laterally on the substrate and grown along arbitrary crystallographic directions. We investigate the hybrid interface by scanning transmission electron microscopy (STEM) and present a detailed study of InAs epitaxy in various templates. Finally, we present tunneling spectroscopy of a proximitized hybrid-TASE NW.

We based the fabrication of hybrid-TASE templates on commercial Si wafers that featured a 150 nm thick buried-oxide (BOX) layer and a 40 or 70 nm thin crystalline silicon-on-insulator (SOI) top layer. The SOI layer had a (110) orientation, different from the (001) SOI layers used in previous work.[21−26] This allowed us to laterally integrate III−V nanostructures along different directions on a single chip, such as ⟨100⟩, ⟨110⟩, ⟨111⟩, ⟨112⟩, and even lower symmetry directions.

Figures 1a−f show simplified schematics of the hybrid-TASE process flow, while Figures 1g−i show scanning electron microscope (SEM) images of a typical device at three fabrication steps, respectively. A detailed description of the process flow is reported in the Methods section. In the first step, the SOI layer was metallized by sputtering of a 25 nm

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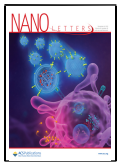





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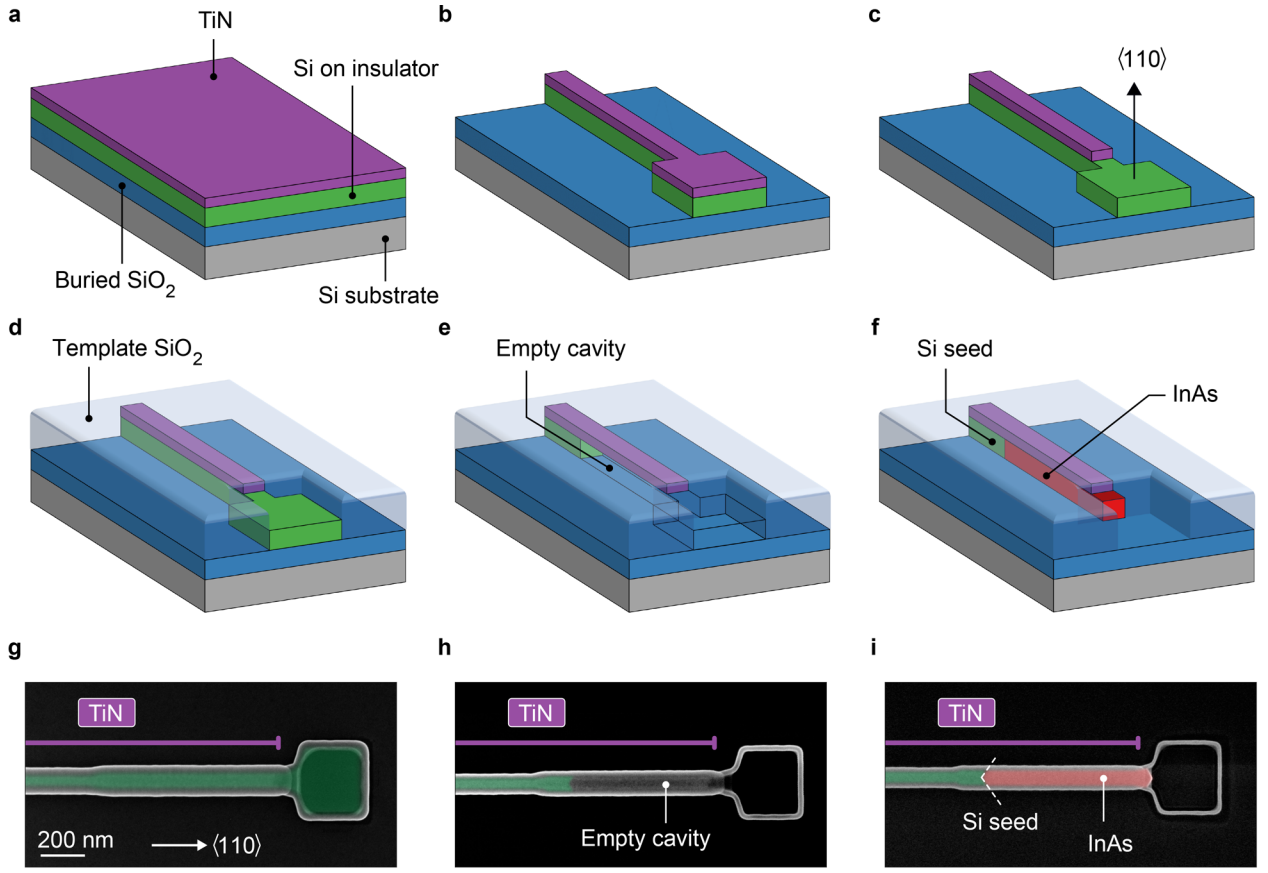


**Figure 1.** Deterministic hybrid-TASE nanowire growth inside a lateral template. (a) A silicon-on-insulator wafer consisting of a thin Si layer (green) separated from the Si substrate (gray) by a buried $SiO_2$ layer (blue) is metallized with a 25 nm thick film of TiN. (b) Self-aligned TiN/SOI bilayer structures are patterned. The structure terminates in a square. (c) TiN is etched from this square. (d) Devices are covered in a conformal 40 nm template $SiO_2$ layer (light blue). $SiO_2$ is locally etched to expose the Si square at the wire end. The TiN stripe remains protected. (e) Selective etching of the SOI creates a cavity formed by template $SiO_2$ and the TiN stripe. A segment of Si remains at the end of the cavity. (f) The surface of the Si segment acts as a seed for epitaxial growth of InAs nanowires (red). InAs nanowires are guided by the template cavity, and an interface to TiN is formed during InAs epitaxy. (g, h, i) Top-view SEM micrographs of the fabrication steps in subfigures d, e, and f, respectively. Regions of Si (green) and InAs (red) are false colored, and they are located below the TiN stripe and $SiO_2$ template layer. The extent of the TiN stripes integrated into the template is indicated by purple lines. Dashed lines in i indicate Si {111} seed facets.

thick layer of TiN (Figure 1a). The TiN layer was polycrystalline with a typical grain size of approximately 5 nm. Self-aligned TiN/SOI bilayer nanowires were dry etched in a single step (Figure 1b), and TiN was locally wet etched from one end of the wire (Figure 1c), leaving the underlying SOI unaffected. The patterned structures were covered in a conformal 40 nm thick $SiO_2$ template, which was locally etched at the template termination (Figures 1d and g). Selective wet etching of the SOI resulted in hollow cavities with sidewalls of $SiO_2$, the BOX layer as floor, and TiN as the ceiling. The length of the cavity was determined by the SOI etching time (Figures 1e and h). Cavities formed in this way terminated in a crystalline Si surface originating from the original SOI layer, serving as a nucleation seed for InAs heteroepitaxy. InAs nanowires were grown inside the template structures via metal−organic chemical vapor phase epitaxy (MOVPE) (Figures 1f and i) using trimethylindium (TMIn) and tertbutylarsine (TBAs) as precursor species. The height and width of the resulting InAs nanowires were determined by the SOI layer thickness and template width, respectively. The NW length was determined by the cavity length and growth time. We reached a yield of about 50%, meaning that half of the InAs nanowires generally nucleate at the Si seed and radially expand to the template sidewalls.

Our choice of TiN as the superconductor was motivated by its compatibility with the hybrid-TASE process flow. In particular, TiN can be etched selectively to Si and $SiO_2$ while it is not attacked by typical Si and $SiO_2$ etchants. This property is crucial for the patterning of hybrid-TASE templates. TiN is chemically stable and has a melting point much higher than the temperatures reached during template fabrication and semiconductor epitaxy. Furthermore, the TiN surface exposed inside our templates allowed selective InAs growth with respect to the Si seed, as we will outline below. These requirements exclude materials commonly used such as Al; however, we envision that the hybrid-TASE technique can be generalized to other nitride superconductors with similar refractory properties such as NbN, VN, and TaN.

We investigated the structural quality of our nanowires by high-resolution scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDX) at 200 kV on lamellae prepared across and along the nanowire axis via focused ion beam techniques. Figure 2a presents an annular dark field (ADF)-STEM cross-sectional view of a hybrid-TASE nanowire similar to the device shown in Figure


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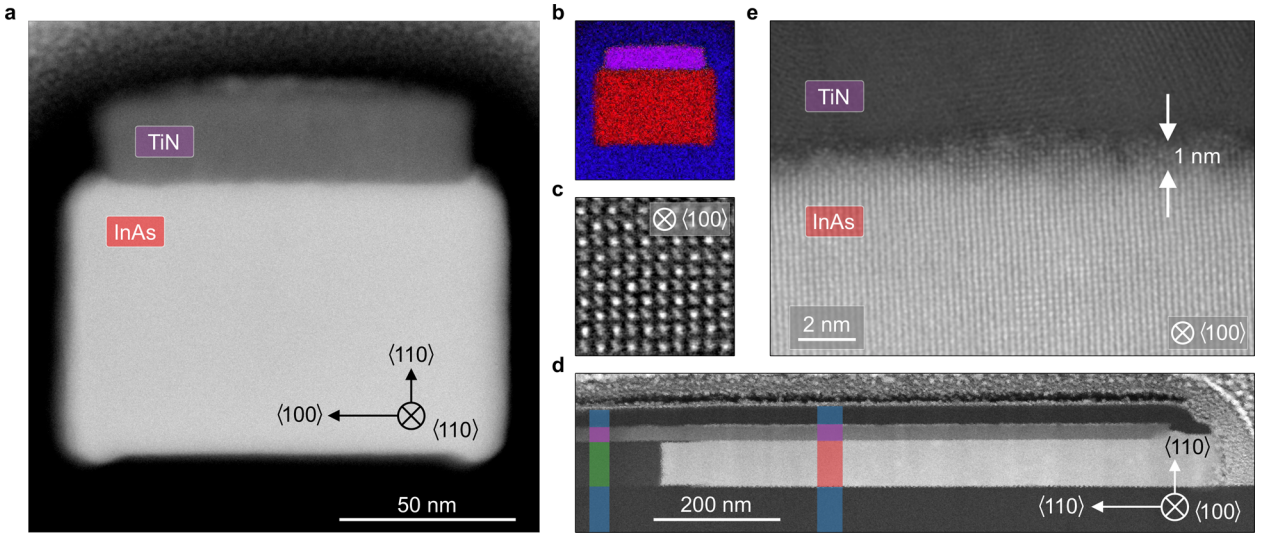


**Figure 2.** Structural study of hybrid-TASE nanowires and the InAs/TiN hybrid interface using STEM. (a) Transversal cross section of a hybrid-TASE nanowire similar to that of Figure 1i. The ⟨110⟩ aligned InAs nanowire features a rectangular cross section and is grown inside a hybrid template formed of TiN and $SiO_2$. (b) EDX elemental mapping of the cross section shown in part a with In (red), Ti (purple), and Si (blue). The frame size is 160 nm × 160 nm. (c) High-resolution STEM image of InAs along the ⟨100⟩ zone axis. The frame size is 2.3 nm × 2.3 nm. (d) Overview of the InAs crystal of part c imaged along the ⟨100⟩ zone axis. The cut is performed along the axis of the device in Figure 3e. The Si seed and the InAs nanowire form an interface at the InAs nucleation site, and a stripe of TiN covers both materials. Colored boxes indicate $SiO_2$ (blue), Si (green), InAs (red), and TiN (purple), respectively. (e) Typical zoom-in on the hybrid interface formed by TiN and InAs shown in part d. The interface roughness between polycrystalline TiN and the InAs single-crystal is approximately 1 nm.

1i. The InAs crystal (bright) exhibits a rectangular cross section with a flat interface to TiN. [We attribute the slightly rounded corners and the expansion of the InAs crystal beyond the width of the TiN segment to an enlargement of the $SiO_2$ template during a final HF etch prior to InAs epitaxy (see the Methods section).] EDX elemental mapping shown in Figure 2b highlights the elemental distribution of the templated nanowire with In (red), Ti (purple), and Si (blue). A representative high-magnification ADF-STEM image of the InAs crystal along the ⟨100⟩ zone axis is presented in Figure 2c. Figure 2d shows the view along the ⟨100⟩ zone axis, obtained by cutting the device illustrated by the SEM image in Figure 3e. Colored boxes in Figure 2d highlight the material stack with $SiO_2$ (blue), Si (green), InAs (red), and TiN (purple), respectively. The Si seed, discussed in more detail below, is visible on the left-hand-side of Figure 2d as a vertical interface. We investigated the interface between TiN and InAs by recording high-resolution ADF-STEM images of this region along the growth axis. A typical example is shown in Figure 2e. The interface between InAs and polycrystalline TiN shows an interface roughness on the order of 1 nm; furthermore, EDX elemental line profiles (see the Supporting Information) indicate a small amount of contamination. A lower bound for the roughness of the hybrid interface was set by the initial SOI layer roughness of 0.3 nm rms, which is likely to increase during processing prior to TiN deposition (see the Methods section). We also point out that the lamella thickness of ∼80 nm might cause the observed interface roughness to appear larger. In previous studies, the roughness of metal top surfaces was found to promote detrimental parasitic nucleation during semiconductor epitaxy.[27] In contrast, our approach utilizes the pristine and freshly exposed TiN back surface, which allows selective growth in geometries with high aspect ratio.

The morphology of the Si seed from which III−V epitaxy started is detailed in Figure 3. Figure 3a shows a high-resolution ADF-STEM image of the interface between Si and InAs from the device presented in Figure 2d. As visible in Figure 1i, the Si seed terminates into {111} facets, inclined with respect to the nanowire axis. The projection of such V-shaped facets onto the ⟨100⟩ viewing plane of the TEM micrograph results in decreased contrast close to the Si/InAs interface. Similarly, the native $SiO_2$ layer on Si appears to extend over InAs. The Supporting Information provides schematics of the seed and an ADF-STEM overview image of the seed region.

The epitaxial relation between the Si seed and the grown InAs NW is evidenced by fast Fourier transforms (FFTs) of the Si seed (Figure 3b), the Si/InAs heterointerface (Figure 3c), and the InAs nanowire (Figure 3d) along the ⟨100⟩ zone axis. [The FFTs are computed from an overview image of the seed area larger than the frame shown in Figure 3a. More FFTs computed along the nanowire length are reported in the Supporting Information.] The analysis shows a clear transition from the diamond cubic crystal structure of Si to the zinc blende crystal structure of InAs. The mismatch in lattice constant between Si and InAs is resolved in Figure 3c as double peaks in the FFT. The alignment between the two peaks demonstrates the epitaxial relation between the two materials, confirming InAs nucleated from Si and not from TiN. Detailed comparison of the alignment of the SOI and InAs crystal revealed a rotation of ∼1° along the ⟨100⟩ zone axis. This is expected in TASE epitaxy where rotations of up to 3° are observed.[23] EDX data of the seed interface, as well as further FFTs of the InAs crystal which confirm that its epitaxial relation is maintained along the full NW, are presented in the Supporting Information.

The key concept of hybrid-TASE epitaxy, that is the formation of a hybrid interface during semiconductor growth, required the InAs crystal to radially expand to the template walls. We achieved this using a high V/III precursor ratio of 150 and a nominal temperature of 550 °C to promote growth of {110} facets deep inside cavities, where the local V/III ratio


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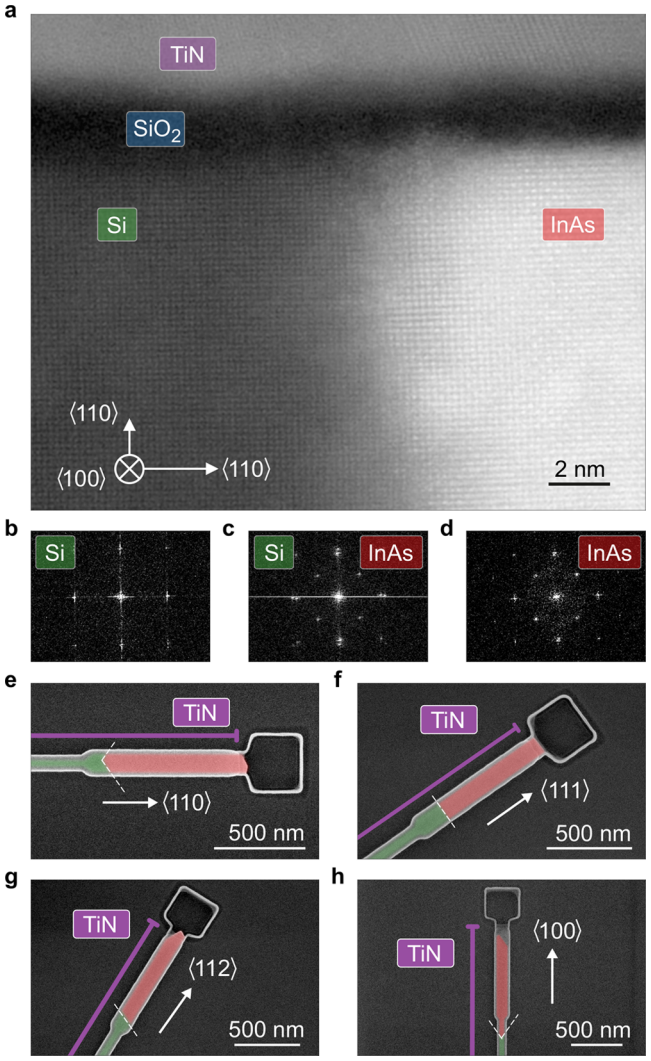


**Figure 3.** Nucleation and growth uniformity of InAs hybrid-TASE. (a) Detailed view of the seed area of Figure 2a imaged along the ⟨100⟩ zone axis. The {111} facets of the seed are inclined with respect to the zone axis (see text). (b, c, d) Fast Fourier transforms of the Si seed layer, the heteroepitaxial interface of Si and InAs, and the InAs NW, respectively. Parts b and d highlight the single-crystalline structure of the Si seed and hybrid-TASE grown InAs; double spots in part c are testament to different lattice constants of the materials. (e) Top-view false color SEM micrograph of a hybrid-TASE NW oriented along the ⟨110⟩ direction. The entire length of the InAs wire is covered by a TiN stripe (purple line). (f, g, h) As in part e but with templates oriented along the ⟨111⟩, ⟨112⟩, and ⟨100⟩ directions, respectively. Si {111} seed facets are indicated by dashed lines.

was reduced due to the differing diffusion mechanisms of the precursor species.[22] Furthermore, these conditions enabled an isotropic growth rate along a plethora of orientations. We present devices grown in hybrid templates along the ⟨110⟩, ⟨111⟩, ⟨112⟩, and ⟨100⟩ direction in the false colored SEM micrographs of Figures 3e–h. Further examples along lower symmetry directions, which are challenging to grow using standard approaches,[28] are shown in the Supporting Information. Such NWs are interesting for the investigation of spin–orbit interaction along low-symmetry crystallographic directions.[29−31] Independently of the wire direction, all devices featured {111} seed facets which were oriented perpendicular to the wafer surface, while their alignment with respect to the InAs NW axis changed depending on the template orientation. The formation of {111} facets is a consequence of the anisotropic Si wet etch, which favors the formation of {111} facets. In the particular case of ⟨111⟩ aligned templates, this resulted in a single seed and growth facet, perpendicular to both the wafer plane and the wire axis (Figure 3f). Finally, we observed that the presence of a TiN layer impacted the growth dynamics of our nanowires. In particular, hybrid-TASE nanowires displayed an axial growth rate which was up to 4 times higher than that of wires grown with the standard TASE method. Further epitaxy experiments at decreased precursor flow indicated an increased V/III ratio inside hybrid-TASE templates compared to TASE, likely due to enhanced surface diffusion of the precursors on the TiN surface. An enhanced surface diffusion could originate from a higher reactivity of the TiN surface compared to $SiO_2$, which would result in a higher sticking coefficient and a decreased desorption of precursor species. [We are grateful to Reviewer 1 for pointing out that a higher sticking coefficient could be the origin of the enhanced growth rate when a TiN surface is present.] In the Supporting Information we provide a detailed discussion of the altered growth dynamics in hybrid templates.

We performed electrical characterization of the hybrid TiN/InAs interface by means of finite bias spectroscopy on the device of Figure 4a. It featured a total length of 1.16 $\mu$m and a cross section of 50 nm × 80 nm. We altered step 3 of the hybrid-TASE process flow (Figure 1c) such that TiN was etched on a 560 nm long segment, allowing for a normal metal probe to be integrated after InAs growth. We also patterned side gates and tunneling gates on either side of the wire. Both the normal contact and the gates (yellow in Figure 4a) were fabricated by evaporation of Ti/Au and lift-off. On the seed side of the wire, the TiN layer branched off to bonding pads. [This specific device was grown with a precursor ratio of V/III = 70.] The Si substrate (Figure 1a) was metallized on the backside by evaporation of Ti/Pt and used as a global back-gate.

Measurements were performed by a low-frequency lock-in technique at the temperature 20 mK. A voltage bias $V_{DC} + V_{AC}$ was applied at one end of the nanowire while the resulting voltage difference $V$ and current to ground $I$ were measured via a differential voltage amplifier and a low-impedance IV converter, respectively. As the Si handle-wafer became insulating below 10 K, we used the back-gate voltage $V_{BG}$ to define the operating point of the device at 14 K (see the Supporting Information) and subsequently cooled down the device to mK temperatures. Devices prepared in this way showed remarkable electrical stability over several days of measurements.

Data presented in Figure 4b was obtained by applying a voltage $V_{g2}$ to two tunneling gates (see Figure 4a) and recording the differential conductance $G$ as a function of the source-drain voltage $V_{SD}$. Three distinct regimes are identified, based on the normal state transmission of the tunneling probe (see line cuts in Figures 4c–e). At $V_{g2} = -1.1$ V the conductance at small $V_{SD}$ was enhanced, a hallmark of Andreev reflection (Figure 4c). The conductance spectrum at $V_{g2} = -3.375$ V highlights discrete subgap states (Figure 4d). Further decreasing the transmission, at $V_{g2} = -3.75$ V, we measured an induced superconducting gap of $\Delta^* = 220$ $\mu$eV (Figure 4e). These findings are consistent with a transparent semiconductor–superconductor interface, with electronic transport governed by Andreev reflection.[11,14,32] The induced super-


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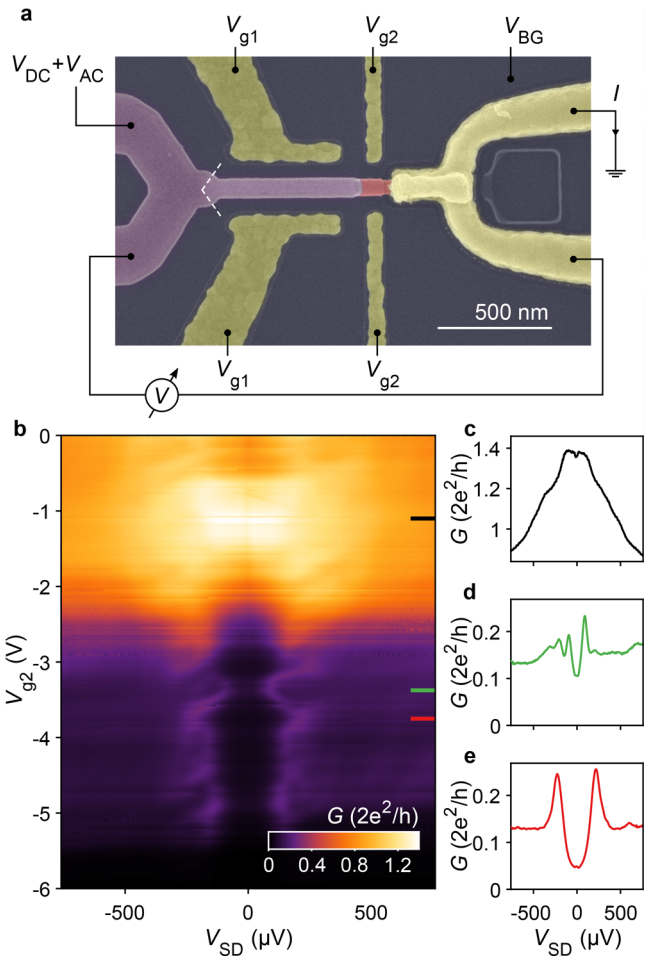


**Figure 4.** Finite bias spectroscopy of a hybrid-TASE tunnel junction. (a) False colored SEM micrograph of a hybrid-TASE device where InAs (red) is grown inside a template with an integrated TiN segment and contacts on one side (purple). Normal contacts and gates (yellow) are patterned with lift-off. Dashed lines indicate the InAs nucleation site below TiN. (b) Finite bias spectroscopy of a hybrid-TASE tunnel contact formed by tuning the tunneling gate voltage $V_{g2}$ at $V_{BG} = -15$ V and with the side gate voltage $V_{g1} = 0$ V. (c, d, e) Line cuts of the data in part b at $V_{g2} = -1.1$ V, $V_{g2} = -3.375$ V, and $V_{g2} = -3.75$ V, respectively.

conducting gap Δ* depended on the specific gate tuning, and we achieved the highest value of Δ* = 300 μeV at $V_{BG} = 0$ V and $V_{g1} = -5$ V. For bulk TiN the expected superconducting gap is Δ = 500 μeV.[33] A possible cause for the reduced superconducting gap in our device is degradation of TiN during fabrication. In the Supporting Information we present measurements on reference TiN nanowires which were exposed to different steps of the hybrid-TASE fabrication. Patterned reference NWs showed a critical temperature of 3.5 K while wires encapsulated in a $SiO_2$ template and annealed at 600 °C for 30 s exhibited a reduced $T_C$ of 2.8 K. In contrast, the $T_C$ values of TiN wires encapsulated in a $SiN_x$ template did not decrease after annealing at 600 °C for 30 min, simulating conditions during InAs epitaxy. To avoid degradation of the superconductor during high-temperature processing, future devices could, therefore, use a $SiN_x$ template dielectric, as routinely employed in selective-area grown devices.[34]

Our approach to semiconductor−superconductor device fabrication is complementary to existing methods, which are based on the in situ growth of elemental superconductors on semiconductors at low temperatures. Furthermore, hybrid-TASE enables new semiconductor−superconductor material combinations. In particular, TASE was already demonstrated for semiconductors such as GaAs, InSb, and GaSb.[21−23] Future hybrid devices might employ superconductors which are chemically similar to TiN but characterized by higher critical temperatures and magnetic fields, such as NbN and VN, making the hybrid-TASE platform particularly interesting for applications requiring high magnetic fields. The compatibility of hybrid-TASE with standard CMOS fabrication can furthermore enable 3D integrated[21] cryogenic qubit control electronics at few K temperature such as amplifiers and multiplexers with low power dissipation, beyond the offerings of Si CMOS.[35]

We presented epitaxy of InAs nanowires on Si inside superconducting TiN/$SiO_2$ lateral cavities, a scalable and CMOS compatible approach to semiconductor−superconductor hybrids. We demonstrated InAs growth in a large variety of crystal directions and observed enhanced growth rates in the presence of exposed TiN. Transport spectroscopy revealed proximity induced superconductivity in the semiconductor, with a transparent hybrid interface.

## METHODS

**Marker Fabrication.** Before patterning the hybrid-TASE templates, we defined markers for optical and electron-beam lithography. First, we deposited a 30 nm layer of $SiO_2$ via plasma-enhanced chemical vapor deposition and then a 100 nm layer of W via sputtering. Using electron-beam lithography, we exposed markers on a AR-N 7520.17 negative tone and transferred the pattern into W by reactive ion etching (RIE) in $N_2/SF_6$ plasma, using the $SiO_2$ layer as the etch stop. After removing the resist, we encapsulated the markers in 300 nm $SiO_2$ grown with plasma-enhanced chemical vapor deposition using tetraethyl orthosilicate as precursor. The wafers were annealed at 750 °C for 30 s, and device areas were defined via optical lithography and buffered hydrofluoric acid (BHF) etching by exposing the SOI layer in regions where hybrid-TASE templates will be patterned.

**Fabrication of Templates with Integrated TiN Segments.** Wafers were cleaned in concentrated piranha solution (sulfuric acid and hydrogen peroxide 2:1) followed by a rinse in ultrapure water and cleaning in a 600 W oxygen plasma. The native $SiO_2$ layer formed in this way was thick enough to protect the back face of the TiN layer during wet etching of Si, greatly enhancing the fabrication yield. We will comment on the importance of this $SiO_2$ layer in more detail below.

We sputtered a 25 nm thick layer of TiN on the entire wafer via DC reactive magnetron sputtering (Figure 1a).

We patterned Si/TiN bilayer nanostructures via inductively coupled HBr plasma etching. For this purpose we defined a 50 nm thick layer of hydrogen silsesquioxane (HSQ) negative tone resist as the etch mask, using electron-beam lithography. After etching, HSQ was removed in diluted hydrofluoric acid. Typical Si/TiN wires patterned in this fashion were 2 μm long and had a width ranging from 40 to 100 nm. The lithographically defined width corresponds to the width of InAs nanowires grown inside hybrid-TASE templates. Si/TiN wires terminated in a square, as shown in Figure 1b.

To ensure adhesion of a 80 nm AR-P 6200.04 positive tone resist layer on TiN, we encapsulated the structures in a 5 nm $SiO_2$ layer deposited via oxygen plasma-enhanced atomic layer


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deposition (ALD). Using electron-beam lithography, we defined regions for TiN etching and etched the exposed ALD grown $SiO_2$ layer in BHF. We selectively removed TiN in a wet-etch solution of $H_2O$, $H_2O_2$, and $NH_4OH$ (5:2:1) at 65 °C[36] as indicated in Figure 1c.

The resist was removed with organic solvents, and a 40 nm layer of $SiO_2$ was deposited using oxygen plasma-enhanced ALD at 300 °C. This $SiO_2$ layer will guide the growth of III−V structures, and we refer to it as the $SiO_2$ template. To reduce the template etch rate in diluted HF, we annealed devices at 600 °C for 30 s in $Ar/H_2$ atmosphere. Using electron-beam lithography on a 80 nm layer of AR-P 6200.04 positive tone resist, openings in areas where TiN had been etched previously were defined. We transferred the openings into the $SiO_2$ template using RIE in $Ar/CHF_3$ plasma and BHF etching. In this way, the Si square at the end of each wire was exposed. Importantly, the exposed area did not overlap with TiN segments on top of the sacrificial Si wire; that is, TiN features remained protected by $SiO_2$. This situation is sketched in Figure 1d.

The exposed Si square allowed us to selectively etch the sacrificial Si structures, creating cavities formed by template $SiO_2$ and TiN. We etched Si in a 2% tetramethylammonium hydroxide (TMAH) solution at 80 °C. The cavity length was determined by the etching time, which was chosen such that a segment of Si remained, as shown in Figure 1e. Typical Si etching times to achieve a back etch of 1.2 $\mu$m ranged from 12 to 15 min. We found that the presence of a native $SiO_2$ layer below TiN as mentioned above was crucial to achieve consistent Si etching results. Without this layer, Si etch rates were reduced drastically, potentially due to interaction between TMAH and TiN. Because TMAH etches Si anisotropically, residual Si segments exhibited typical {111} facets as seen in Figure 1h. The facets were oriented perpendicular to the (110) wafer surface.

**InAs Epitaxy inside Hybrid-TASE Template Cavities.** Prior to MOVPE semiconductor growth, we immersed the templates in diluted hydrofluoric acid $H_2O$:HF 20:1. The etching served two purposes as it both removed the native $SiO_2$ protection layer below the TiN segments and etched native $SiO_2$ from the Si {111} seed facets while creating hydrogen terminated facets. At the same time, the inner template dimensions increased slightly. This effect can be seen in Figure 2a, where the InAs nanowire was approximately 20 nm wider than the TiN region.

We promptly transferred chips into a MOVPE growth reactor where they were annealed at 600 °C for 5 min under TBAs flow. $H_2$ was used as carrier gas, and InAs growth started as we introduced TMIn into the reactor. InAs growth was performed at a pressure of 60 Torr at temperatures of either 550 or 600 °C and V/III ratios between 70 and 150. Typical growth times ranged from 9 to 11 min. The dynamics of InAs epitaxy in hybrid-TASE templates are described in the Supporting Information.

**Device Contacting and Gates Patterning.** After InAs growth, we spun a double layer of PMMA 669.04 (300 nm) and AR-P 672.03 (100 nm) resist and patterned device contacts with electron-beam lithography. After resist development in methyl isobutyl ketone (MIBK) and isopropanol (IPA) with ratio 1:2, we etched the $SiO_2$ template with BHF in exposed regions and passivated the InAs surface by immersion in 2% ammonium sulfide solution prior to evaporation of Ti (10 nm) and Au (150 nm). After lift-off in dimethyl sulfoxide (DMSO), we spun a single layer of AR-P 672.03 (100 nm) and patterned gate structures via electron-beam lithography. The resist was developed in MIBK:IPA (1:2), and layers of Ti (5 nm) and Au (20 nm) were evaporated prior to lift-off in DMSO. After etching of native $SiO_2$ in BHF, we metallized the Si handle-wafer by evaporation of Ti (5 nm) and Pt (40 nm). During these steps, devices on the chip were protected by a 6.2 $\mu$m thick layer of AZ 4562 optical resist.

## ■ ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c03133.

Hybrid-TASE epitaxy along low-symmetry directions, epitaxy dynamics in hybrid-TASE templates, EDX analysis of hybrid-TASE interfaces, seed morphology, single-crystallinity, electrical tuning via a back-gate, measurement of the TiN superconducting gap (PDF)

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### Notes

The authors declare no competing financial interest.

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