Comment

https://doi.org/10.1038/s41467-025-59162-x

Chern networks: reconciling fundamental physics and device engineering

Matthew J. Gilbert

A rift has occurred within the scientific community between two formerly close-knit fields: condensed matter physics and electronic device engineering. What started as a union to understand the fundamental optical and electrical properties of semiconductors has been split by divergent interests. While the partnership has produced revolutionary changes in the way that information is processed and consumed by an increasingly interconnected society, now the two disciplines rarely speak to one another. As the years have passed, condensed matter physics has become enamored with delicate electronic effects in increasingly complex materials and geometries to the detriment of realistic applications. Meanwhile, device engineering has remained steadfastly focused on room-temperature performance and overall efficiency, prizing incremental improvement over potential disruptive advances using alternative materials and physics. Recent advances in topological electronic systems—in particular those exploiting Chern insulators—while elegant, prompt a necessary reexamination of the device engineering needs and the associated metrics with the goal of establishing a commonality within the blooming field of topological electronics. The purpose of this Comment is to initiate such a reexamination in the hopes that, with a better understanding of future device needs, perhaps the two areas may reunite to usher in the next electronic revolution via the use of topological phenomena.

The onset of the Chern evolution

An uncontroversial observation concerning the trajectory of topological condensed matter research, is that the bifurcation into fundamental and applied categories has been accelerating[1,2]. The previous acknowledgment of applications in publications has been a slight reference to a specific use case at the end of the abstract and a second time in the concluding statements. This has been replaced by detailed and precise demonstrations of topological phenomena, with the specific intention of investigating the potential role of topological matter in future device technologies. Perhaps one of the most recent and elegant demonstrations of such applied topological research comes in the form of Chern networks[3–6]. Generally speaking, a Chern network, as shown schematically in Fig. 1, refers to the electrical and/or magnetic control of dissipation-free 1D chiral edge state propagation between non-local electrical contacts within a heterogeneous device design. To be clear, the definition of the quantum anomalous Hall (QAH) effect is a state in which the longitudinal resistivity disappears, $\rho_{xx} = 0$, while at the same time the Hall resistivity becomes exactly quantized as $\rho_{xy} = h/e^2$ in the absence of a net magnetic flux penetrating the device structure[7,8]. By controlling the sign of the applied perpendicular magnetic field, or ultimately an applied electric field as illustrated in Fig. 1(A), the chirality of the edge state may be controlled. The roots of 1D chiral edge transport in the presence of broken time-reversal symmetry may be traced directly back to the foundational work by Haldane[9]. Nevertheless, the functional physical principle behind Chern networks is the successful exploitation of the bulk–boundary correspondence between fabricated device regions that possess *any* discrepancy between regional (first) Chern numbers. Therefore, the idea of being able to use applied electromagnetic fields to alter the direction and destination of dissipationless edge current flow provokes images of a clear topological means to guide the transmission of information within interconnected and arbitrarily complex device geometries, as shown in Fig. 1B. In a short amount of time, the evolutionary arc that connects the early efforts in the fabrication of a Chern network using antiferromagnetic $MnBi_2Te_4$ layers grown via molecular beam epitaxy (MBE) immersed within a strong, but non-quantizing, magnetic field[3] to the most recent use of magnetically-doped topological insulators created via an in-situ MBE mask that function without the need for continuous application of an external magnetic field[6], it is clear that continued refinement of Chern networks will produce quantized topological transmission of current between non-locally connected contacts. While the continued improvement of Chern networks may be a forgone conclusion, the more pertinent questions, asked from a more applied perspective, are two-fold: (1) what device need is being addressed? (2) how does the successful implementation of the Chern network compare with other proposed device engineering solutions? Questions about the form of future electronic device

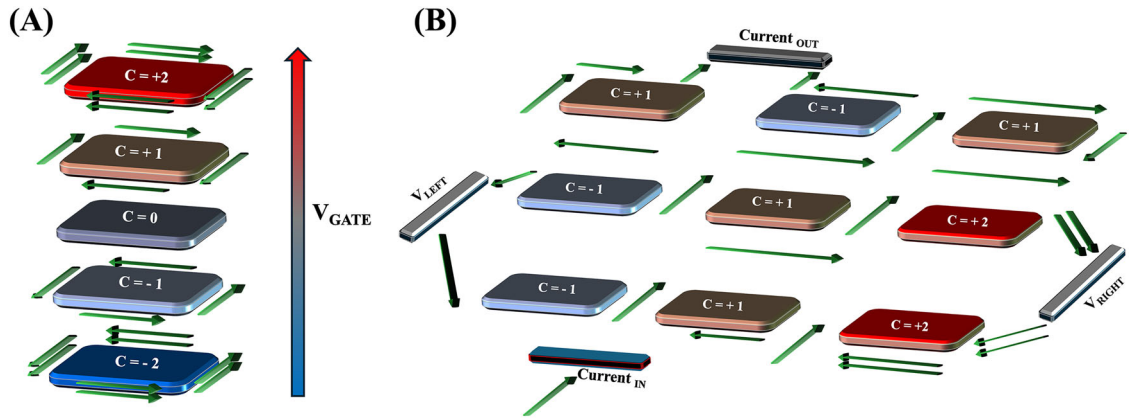

Fig. 1 | Schematic Illustration of a Chern Network. A Illustration of an electrostatically tunable Chern insulator, otherwise known as the quantum anomalous Hall insulator, shown as evolving from a Chern number of $C = -2$ to $C = +2$ as tuned by an external gate voltage, V_{GATE}. As the value of the Chern number changes, the number and chirality of the edge states propagating about the periphery of the system, as shown by the associated directional arrows. **B** An illustration of a Chern network where multiple externally tunable Chern insulators, each containing regions of distinct Chern number, are brought into close proximity to one another. The interactions change the overall direction of the flow of information in an externally controllable manner allowing for potentially complex designs. Current is input into the system and, given the pattern of Chern numbers in the network, the propagating current is directed into different remotely located voltage probes before exiting the network.

technologies have been a topic of heavy debate for many years. To be more specific, the most quoted proposed solution that Chern networks are cited to address is the issue of power consumption. Currently, traditional electronic information processing is accomplished using highly interconnected complementary metal-oxide-semiconductor (CMOS) device technologies. It is well-known that within CMOS, most of the power input to a chip is consumed when the state of the device is being altered either from the “off" state to “on" state or vice versa. Given the sheer number of power dissipating transistors that comprise current microelectronic chip designs—134 billion in the Apple M2 Ultra[10]—it is unsurprising that even the most energy efficient device solutions will dissipate a significant amount of energy in the course of normal operation. To this end, the semiconductor industry, and device engineers more broadly, are keenly aware of the power dissipation issue and have actively sought alternative “Beyond CMOS" device technologies using new physical principles and materials. If, indeed, the Chern network or another forthcoming solution proposes a device for practical consideration then there exist well-established device metrics that may be found in the International Roadmap of Devices and Systems (IDRS) against which these proposed devices must be benchmarked[11–13]. In this Comment, I point to some of the issues related to size, temperature, and performance that may hinder Chern networks as a viable technological solution by device engineers, and I ask questions that require the attention of both physics and engineering researchers. In doing so, my goal is to take one step towards normalizing and applying the relevant figures of merit, where appropriate, to prod the nascent dialog between condensed matter physics and device engineering towards joint solutions that address real-life performance needs.

The size problem

In the quest to find stronger overlap between device engineering and condensed matter physics through applied topological electronics, it is legitimate to ask to what extent the work done in applied topology originating in condensed matter addresses an identified need within device engineering. In an attempt to resolve the question with regards to the Chern network, consider first the basic building block of the Chern network—the QAH insulator—from an engineering perspective. From the perspective of condensed matter physics, one of the features of the QAH insulator is the fact that the conduction is performed completely at the interface between two regions of differing Chern numbers. From the device engineering perspective, one of the largest faults of the QAH insulator is that the conduction is performed only along a thin section of the system. To have such a wide area of the 2D bulk between the counter-propagating edge states of potential chip space left unused is unacceptable in high-performance circuit design. On the other hand, it is impossible to have only one single chiral edge state without the associated 2D bulk to support the 1D holographic edge state. Therefore, the edge state topology is only protected while there is sufficient separation between the counter-propagating edge states so as to forbid the scattering of quasiparticles from one chiral edge into the anti-chiral partner localized on an opposing edge within the device structure. The application related question of minimum device size becomes a vital one that condensed matter has started to address. To this point, in recent work, the confinement of the QAH insulator edge state has been examined in MBE grown topological insulator (TI) devices comprised of 3 quintuple layers (QLs) of Cr-doped $(Bi,Sb)_2Te_3$ with 4 intervening QLs of undoped $(Bi,Sb)_2Te_3$. Quantum transport measurements on these layers have been systematically conducted as a function of applied magnetic fields and gate voltages over a wide range of QAH insulator widths from $w = 300\ nm$ to $w = 10\ \mu m$ with a minimum width of $w_{min} = 72\ nm$[14]. The results illustrate how the penetration of the edge state into the bulk, perhaps aided by the presence of bulk disorder, limits the width to be $w \approx 72\ nm$ given a decay length of the edge state into the bulk of $L_{edge} \approx 36\ nm$. For comparative purposes, using the IRDS 2022 edition, the width of center-to-center distance for the first metal interconnect line, or pitch, in production year 2022 CMOS-based logic devices was already at 24 *nm*. Additionally, the CMOS logic technology is based on FinFET architecture, in which a nanoribbon of semiconductor is contacted on

three sides to form conducting channels, that may then be stacked to form the eventual multi-billion transistor application. Put in this perspective, Chern networks would need to be scaled in size to well below currently accessible dimensions to be competitive either as logic or interconnect implementations. Furthermore, in the context of multi-billion device applications, the presence of a comparably large resistance of $R_{chern} = 25.8\,k\Omega$ per Chern device is noteworthy. The fundamental resistance implies that significant, compared to CMOS, energy will be dissipated in Chern networks not just during switching events, but during steady-state operation. Such limitations portend questions about the overall power efficiency of large multi-device Chern networks as they are scaled by number and not only size.

The thermal problem

From an engineering perspective, temperature is a vital quantity. Naturally, if the intended application is to be within the context of, for example, superconducting electronics[15], then the energy scales of the system are expected to be small and, therefore, a path to functionality at room temperature, here defined to be $T_{RT} = 300\,K$, need not exist. However, if conventional computing, memory or spintronic applications are the goal, then there must necessarily be a path—regardless of the circuitry—that ends with room-temperature operation. To date, there are two separate paths that have been explored as a means to implement the QAH effect within topological materials. The first and most successful approach is to use magnetic dopants to fabricate compounds such as Cr-doped $(BiSb)_2Te_3$ or V-doped $(BiSb)_2Te_3$[6,16,17]. Indeed, such material systems have demonstrated the QAH effect, albeit with two caveats. First, the observation of the QAH effect is at very low temperatures, typically below $T \leq 200\,mK$ despite observed Curie temperatures that are on the order of $T_C \approx 20K$[17]. The second caveat is that the longitudinal resistance $\rho_{xx} \approx 0$ only at the lowest system temperatures and in the presence of the smallest excitation currents. The difficulty in obtaining quantized transport in magnetically doped topological materials indicates that the magnetic exchange gap, Δ_{EX}, that is opened by the ferromagnetic orientation of the dopant ions is very small compared to the system thermal energy[18,19]. Furthermore, the non-quantized transport at the edge of the system dictates that the system is not topological and indicates the existence of an alternative conduction path via the bulk[16,17].

Nevertheless, opportunities exist to make progress towards greater thermal stability in Chern networks. Rather than appealing to an overall ferromagnetic state mediated by magnetic dopants, an alternative that may lead to higher resilience to thermal effects may be proximity-induced magnetism. From a naive perspective, the existence of a multitude of magnetic materials boasting Curie temperatures that are greater than T_{RT} and topological materials that host topological phases at temperatures greater than T_{RT} accommodates the possibility of engineering a high-temperature QAH insulator phase[20,21]. To this end, there have been a number of significant studies that have paired magnetic materials with high Curie temperatures and topological materials[21–24]. At this time, however, while there are clear signatures of induced magnetism in the target topological material, there is no clear evidence of a Chern insulator produced via proximity coupling of disparate magnetic and topological materials. Yet one of the most compelling implications resulting from the experimental and subsequent theoretical work[25] is that the presence of an overall long-range magnetic phase—either ferromagnetic or antiferromagnetic—may be irrelevant to the ability to instill high-temperature proximity-coupled phases within an adjacent topological material. In this context, if high-temperature operation is to be optimized, then the choice of magnetic materials should not be predicated on the energy scale associated with T_C but rather based on two criteria: (1) the median physical distance between the magnetic atoms within the host magnetic material and the surface of the topological material, and (2) the magnitude of the magnetic moment associated with the magnetic atoms in the host magnetic material.

The performance problem

When considering applied topology from both the condensed matter and device engineering perspectives, there is no larger separation between the disciplines as when considering the performance expectation gap between condensed matter perception and device engineering reality. Within condensed matter physics literature, the Chern network is a virtual panacea that is poised to cure the real engineering problems surrounding the reduced performance enhancements obtained by the inexorable shrinking of CMOS implementations of semiconductor logic devices. However, the performance degradation obtained with device scaling is well understood by the device engineering community and routinely updates the metrics by which they measure the performance of semiconductor logic and the constituent devices[12]. Furthermore, device engineering has recognized the need to find disruptive technologies that will enhance the performance of key components of digital information processing[11]. Thus, any proffered solution must be benchmarked against current CMOS on these key figures of merit (FoM). For instance, the use of topological materials, and even Chern networks, has long been proposed as a methodology to overcome the rise in the resistance of copper interconnects with continued scaling due to grain boundary and surface scattering[12]. Benchmarking the use of topological materials as interconnects has, indeed, shown benefits over copper with the caveat being that such topological benefits only become appreciable when the interconnect diameters are scaled below $6nm$ in width and ignores the question of how one would integrate these interconnects into the CMOS fabrication process to replace Cu[26]. In light of this, we apply basic benchmarking to the Chern network to determine where, as of now, this scientific development sits amongst other current and proposed technologies on two key FoM: subthreshold slope and drive current. Thus, to make a comparison between the Chern network performance and the 2022 generation, or $3nm$-node logic device specifications, we use an analogy with the edge channel current to represent the drain current, I_{DS}, with the backgate voltage being the same as the gate-to-source voltage, V_{GS}.

Subthreshold slope. We begin with the subthreshold slope (S_{sub}), which is a FoM that quantifies the amount of power that is required to change the current flow by one order of magnitude:

$$S_{sub} = \left[\frac{\partial log_{10}(I_{DS})}{\partial V_{GS}}\right]^{-1}. \quad (1)$$

Subthreshold slope is one of the primary measures for overall comparison of effectiveness of current modulation via an external applied electric field. For a standard CMOS transistor, the subthreshold slope is limited by thermionic emission of carriers over the potential barrier that separates the origin of carriers within a transistor, i.e., the source, from the point where the injected carriers are extracted, i.e., the drain. The fundamental limit for CMOS transistors is $S_{sub} = 60\,mV/dec$ and state of the art transistors operate very close to this fundamental limit at between $S_{sub} = 75 - 82\,mV/dec$ in the 2022 production line[12].

A simple calculation using published data indicates that the Chern network, currently, has a subthreshold slope of $S_{sub} = 333.45\ mV/dec$[5]. While the calculated S_{sub} may be improved over successive iterations, the major difficulty is that these measurements are carried out at 20 mK and not at room temperature. Further, the voltages that are applied to the gate to modulate the conduction are several orders of magnitude larger than in the state-of-the-art CMOS transistor. However, the expressly low temperature operation may be advantageous in certain applications due to the inability of CMOS devices to operate at low temperatures due to dopant freeze-out—or the state where the thermal energy imparted to the dopant atoms is insufficient for them to become ionized. Therefore, Chern networks may find utilization in applications such as superconducting spintronics for alternative forms of low-temperature logic[27,28].

Drive Current. The reality of the highly interconnected architecture of CMOS is that the successful operation of one isolated device is of questionable value. While such singular demonstrations are important as a means of determining basic proof of concept, it is crucial to ensure that a path exists for one singular device concept to be capable of producing sufficient current to drive subsequent stages of device architecture. In logic core devices produced for the 2022 3 nm technology node, the main MOS architecture is the FinFET, which consists of a thin Si nanoribbon that is surrounded on three sides by a metal gate[12]. Therefore, when the device is turned on by inverting the surface beneath the gate, three conductive channels are produced resulting in an on-state current of between $I_{on} = 65 - 88\ \mu A$ per device with a corresponding off-state current of $I_{off} = 0.1 - 10\ nA/\mu m$[12]. Given the topological nature of the current flow in the Chern network, it is natural to expect the Hall current to be quantized. Using the same topological argument, the longitudinal current may flow without dissipation, however, there is an associated active device resistance that is fundamentally limited to h/e^2. For comparative purposes, consider the drive current density within a Chern network, $J_{on}^{CN} = e^2 V_{on}/hL_{edge}$, with V_{on} being the drive voltage. Chern networks are currently incapable of approaching the current density in a CMOS transistor, $J_{on}^{CMOS} = 874\ \mu A/\mu m$. However, additional iterations of Chern networks using different magnetic and/or topological materials may show increased current density by increasing the topological gap size, Δ_{EX} in the Chern network. Increases in Δ_{EX} effectively reduce the size of L_{edge}, thereby, increasing the resultant current density in a Chern network.

Nonetheless, the consequences of such low current flow within the device structure may best be understood by considering the device concepts of static and dynamic fan-out. Fan-out is defined as the number of logic-gate inputs that may be driven by the output of a given logic gate without degradation of the logical state. While the static—or resistive DC component—of fan-out may be improved by better mitigation of contact resistances in Chern networks, the dynamic—or AC capacitive component—is more pernicious. The speed at which a signal moves through logic gates is limited by the charging time of the inherent capacitance of the logic gates, leading to propagation delays. Propagation delays may be, in part, overcome by using higher input currents to charge the next logic gate, via

$$I_{input} = C_{logic}\frac{\partial V_{logic}}{\partial t}. \quad (2)$$

In Eq. (2), I_{input} is the input current fed into the logic element from a previous logic stage, C_{logic} is the capacitance and V_{logic} is the voltage of the current logic gate, respectively. Eq. (2) indicates that by increasing the current fed into subsequent logic stages from previous stages, the voltage across the current logic stage increases faster thereby increasing the speed of signal propagation. Cast in this light, the small output current from the Chern network will produce significant delays in signal propagation if integrated within a CMOS framework.

Towards reconciliation

The advances put forth in the recent series of Chern network experiments represent a glimpse of the functionality and the variability of topological materials and responses. Given the difficulties discussed, namely scaling, temperature and performance, it is unlikely that such systems will find a home in next-generation CMOS technologies. However, while the specific expression of topological behavior may not impact the device architecture landscape, the important lessons learned within these impressive works must serve as the basis for continued exploration of topological materials from the applied or device perspective.

To me, the overarching question germane to both perspectives is "Does the presence of topology matter for enabling new technologies?". Nevertheless, many open questions remain from both the fundamental and applied perspectives. From the applied perspective, questions remain around fundamental device properties, such as understanding the electrostatic and transport properties of deposited metals on topological materials, as this relates directly to the device contact resistance—a crucial parameter in any application[15,29]. From the fundamental perspective, an intriguing question surrounds the importance of crystallinity to device performance. Put another way: is it necessary to have perfectly crystalline topological materials to be able to exploit topological functionality? When considering time-reversal invariant topological materials, like $(Bi,Sb)_2Se_3$, the topological nature is protected by the inversion of band ordering that is brought about by the strength of the spin–orbit interaction. However, amorphous materials, characterized by randomized hopping strengths and positions of atoms within a material possessing neither long-range or short-range order, constructed from atoms with strong spin–orbit interactions, have been shown to possess the same topological features[30,31]. Therefore, perhaps the consideration of a cheaper quasi-crystalline topological system may be able to produce similar behavior at lower cost and effort[32], if the presence of a topological surface state is the critical requirement for device implementations.

Regardless, my perspective remains that the goal of topological technologies should be to replace functionality at the system level rather than at the level of individual devices. As we begin to look towards bringing the areas of condensed matter physics and device engineering closer, I believe that by starting the dialogue by examining some of the recent condensed matter successes and open device engineering questions to be addressed, we may collectively move towards a viable topological technology.

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Received: 1 September 2024; Accepted: 10 April 2025;
Published online: 25 April 2025

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Acknowledgements

I acknowledge support from the Army Research Office under contract number W911NF-23-2-0090

Competing interests

The author declares no competing interests.

Additional information

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Peer review information *Nature Communications* thanks the anonymous reviewers for their contribution to the peer review of this work.

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