APPLIED SCIENCES AND ENGINEERING

Thermionic junction devices utilizing phonon blocking

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Electrothermal elements are used in various energy harvesters, coolers, and radiation detectors. The optimal operation of these elements relies on mastering two competing boundary conditions: the maximization of the electrothermal response and the blockade of lattice (phonon) thermal conduction. In this work, we propose and demonstrate that efficient electrothermal operation and phonon blocking can be achieved in solid-state thermionic junctions, paving the way for new phonon-engineered high-efficiency refrigerators and sensors. Our experimental demonstration uses semiconductor-superconductor (Sm-S) junctions where the electrothermal response arises from the superconducting energy gap and the phonon blocking results from the acoustic transmission bottleneck at the junction. We demonstrate a cooling platform where a silicon chip, suspended only from the Sm-S junctions, is cooled by ~40% from the bath temperature. We also show how the observed effect can be used in radiation detectors and multistage electronic refrigerators suitable for cooling of quantum technology devices.

INTRODUCTION

Control of heat flux at small length scales is crucial for numerous solid-state electronic devices and systems. In addition to the thermal management of information and communication devices (*1*), the mastering of heat transfer channels down to the nanoscale also enables, e.g., new memory components (*2*), high-sensitivity detectors and sensors (*3*–*5*), energy harvesters (*6*), and compact electronic refrigerators (*7*). These devices typically use electrothermal elements, the operation of which is based on the correlation between heat/energy and charge carrier currents and requires minimization of the thermal conductance to the bath and maximization of the electrothermal response. Well-known examples of these elements are thermoelectric materials (*8*, *9*) and thermionic junctions (*6*, *10*). The former are based on diffusive phonon and electron transport along a thermoelectric lead, whereas the latter rely on local energy filtering of electrons by an energy barrier. The ultimate limit of electrothermal elements is reached in molecular junctions (*11*, *12*).

In thermionic junctions, the most energetic thermally excited electrons are emitted through vacuum or short solid barrier (*10*) (Fig. 1A). The physical principle of a thermionic junction is therefore quite general, and thermionic operation can be observed in electrical and electrothermal properties of various devices, such as p-n and Schottky diodes (*13*), vacuum barrier components (*6*, *14*), quantum dots (*15*), metallic single-electron devices (*16*), and superconducting tunnel junctions (*17*–*21*) (Fig. 1B). Common to all these thermionic devices is that the electron flow is capable to cool the cold reservoir below the bath temperature (hot reservoir), provided that there is sufficient thermal isolation. These electronic refrigerators have vast applications in cooling of electronics and different sensors, and Peltier refrigerators based on diffusive thermoelectrics are well-known off-the-shelf components dedicated for this task (*22*). In the opposite case, the flux of energy through the elements results in electronic response, an effect that is broadly used in energy harvesters (*8*) and thermal radiation detectors (*3*).

In all-solid electrothermal devices, phonons introduce a detrimental heat flow channel that hinders the overall cooling in refrigerators

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and the total electrothermal response in harvesters and detectors. Because of this, for example, in the field of thermoelectric devices, considerable efforts have been devoted in the investigations of phonon engineering approaches to reduce the phonon heat flow (*8*, *9*). Promising approaches include developing new materials and scaling the cross-sectional dimensions of the thermoelectric leads down to the nanometer scale to reduce the phonon mean free path.

In thermionic junctions connecting different reservoirs (Fig. 1A), thermal isolation has been considered to be difficult to achieve through the junction itself due to apparent strong phonon transmission over short distances. Typical thermal isolation schemes of thermionic devices include superlattices, vacuum (gas) barriers (*6*, *8*), and small electron-phonon coupling occurring at low temperatures (*17*). Reduced electron-phonon coupling has been broadly used, especially in superconducting junction thermionic coolers based on normal metal–insulator–superconductor (NIS) (*19*, *20*) and semiconductor-superconductor (Sm-S) tunnel junctions (*21*). NIS coolers with the normal metal electrode working as a cold finger have been used in refrigeration of different payloads (*23*–*25*) at low temperatures. In general, superconducting junction coolers can provide a compact and highly attractive alternative for cryo-liquid–based cooling stages, and these refrigerators would revolutionize technology fields relying on low-temperature devices. A topical example is the emerging field of quantum technologies (*26*), where the cooling of electronics, sensors, and/or quantum computation/simulation cores is often the basic functional requirement. Control schemes for quantum bits (qubits) can use, e.g., classical dissipative cryo–CMOS (complementary metal-oxide semiconductor), which is at a higher temperature stage above 1 K with respect to the sub–1 K qubits (*27*). These arrangements would benefit substantially from compact electronic refrigerator cooling only the qubits to the lowest temperature. Thus, there is apparent need for the low-temperature electronic junction coolers, but the engineering of the electron-phonon coupling has proven to be such a difficult challenge that new approaches for achieving good thermal isolation and, thereby, efficient cooling are called for.

In this work, we pursue a new method for achieving thermal isolation in thermionic junctions. We demonstrate that a single solid interface can operate both as an efficient thermionic element and a heat transfer barrier for phonons (Fig. 1A). We use Sm-S tunnel junctions where the thermionics is controlled by the superconducting
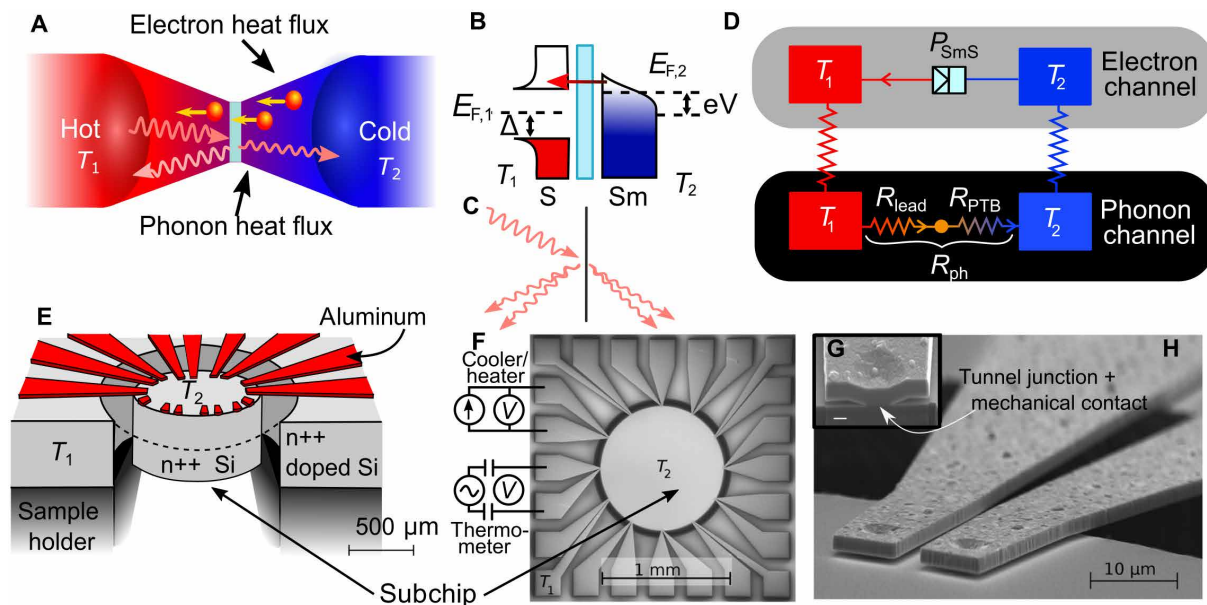
Fig. 1. Cooling scheme. (**A**) Conceptual image of particle fluxes through solid-state thermionic barrier/interface connecting hot and cold reservoirs. The interface suppresses phonon heat flow between the reservoirs and acts as a thermionic junction that governs electron transport. (**B** and **C**) Electron (B) and phonon (C) interfaces between the reservoirs. Electron transport is limited by the energy gap of the superconducting lead and phonon transport by the phonon thermal boundary resistance R_{PTB}. (**D**) Simplified heat resistance network of our system presenting the electric heat flow/power (P_{SmS}) of the Sm-S junctions and the thermal resistance between the hot and cold reservoirs (R_{ph}), which depends on R_{PTB} and lead thermal resistance (R_{lead}). For a more detailed version, see fig. S7. (**E**) Artistic image of the experimental cooling platform. The subchip is physically supported by 24 Sm-S junctions connected to the aluminum leads, which mediate the heat conduction between the main chip and subchip. The large size of the subchip ensures that its electrons and phonons share the same temperature. (**F**) Scanning electron micrograph of a sample with Ø 1-mm subchip. One pair of Sm-S junctions is biased with alternating current (ac) and used as a thermometer, whereas one or more of the other pairs are biased with direct current (dc) and used as heaters or coolers. The measurement setup is further discussed in Materials and Methods, sections S1 and S2, and fig. S1. (**G** and **H**) SEM images of the cross section of a tunnel junction (G) and two superconducting leads (H), showing that the superconducting leads are mechanically connected to the subchip only via the Sm-S tunnel junctions (indicated by white arrow), with diameters between 1.5 and 3 μm.

energy gap and voltage bias (19–21) (Fig. 1B). The phonon thermal boundary resistance (R_{PTB}) at the junction provides the phonon blockade (Fig. 1, C and D), which is enhanced in some of our samples also by the thermal resistance provided by the superconducting leads. The Sm-S junctions are used to support, thermally isolate, and electrically refrigerate a piece of silicon chip, referred to as the subchip (Fig. 1, E to G). This approach is in strong contrast to previous works of superconducting tunnel junction coolers with suspensions, where cold fingers are used instead (24, 25, 28, 29). Our suspended junctions provide substantial cooling of ~40% from the bath temperature at sub-kelvin temperatures. The cooler and the overall electrothermal performance can be substantially enhanced by using phonon engineering methodologies (30, 31). For example, we demonstrate by simulations that these approaches combined with cascaded refrigeration stages can enable cooling even from ~1.5 to below 0.1 K, which is one of the long-standing goals of electronic refrigeration, paving the way in replacing cryo-liquid–based refrigeration stages by solid-state ones, e.g., in the field of quantum technologies. Electrothermal elements are important also for sensor applications, and we discuss how to use the introduced methodology to enhance the performance of thermal photodetectors.

RESULTS
Electrothermal operation and electronic cooling
The fabrication of our Sm-S (Si-Al) junctions follows the procedures of (32). The subchip is released from the main chip using deep reactive

ion etching and hydrogen fluoride (HF) vapor etching (see Materials and Methods for details). Scanning electron micrographs of one of the devices are shown in Fig. 1 (F to H). In this letter, we show data on three devices (S1 to S3) with parameters as given in Table 1. In contrast to the others, S1 had silicon oxide between the aluminum leads and the subchip, which decreased R_{PTB} and, thus, yielded information on the thermal resistance of the Al leads.

An Sm-S (or NIS) junction can function as a thermionic element due to the energy filtering property of the superconductor, which originates from the superconducting energy gap Δ of the quasiparticle (electron) density of states (Fig. 1B) (19, 20). At small bias voltages ($V \leq \Delta/e$, where e is the elementary charge), only the most energetic electrons of the subchip can overcome the gap and tunnel to the superconductor, which is equivalent to cooling. A similar effect is obtained at the opposite bias when quasiparticles tunnel to the lowest unoccupied states of the subchip. Here, we use a simple model for the Sm-S junction cooling power (for a more rigorous approach, see section S4)

$$P_{SmS,cool}(T_2) \approx \frac{\Delta^2}{e^2 R_T} 0.59 \left(\frac{k_B T_2}{\Delta}\right)^{\frac{3}{2}} - \frac{1}{2}\frac{V_{opt}^2}{R_{gap}} \qquad (1)$$

where R_T is tunneling resistance, and T_2 is the temperature of the subchip. The first term in Eq. 1 is the ideal cooling power, which is valid at optimal voltage (33) $V_{opt} \approx (\Delta - 0.66 k_B T_2)/e$, when $T_2 \leq T_S \ll \Delta/k_B$ (20). Here, k_B is the Boltzmann constant, and T_S is the temperature of the superconductor. The latter term is an approximate

Table 1. Sample parameters and literature values for thermal boundary resistance. Here, A is the area of a tunnel junction, d is the diameter of the subchip, $R_A = R_T A$ is the characteristic junction resistance, and R_T is the junction resistance. Thermal resistance prefactors (α) are the values obtained from the fits of Fig. 2, whereas α_{AMM} and α_{DMM} correspond to theoretical R_{PTB} (35).

Sample	A μm^2	d μm	$R_A = R_T A$ $\Omega \mu m^2$	α $K^4/\mu W$	α_{AMM} $K^4/\mu W$	α_{DMM} $K^4/\mu W$	Max cooling %	Max cooling mK
S1	2.0/137*	300	538	4.5	–	–	15 (@ 140 mK)	22 (@ 166 mK)
S2	7.5	1000	476	5.6	6.5	8.8	40 (@ 170 mK)	83 (@ 244 mK)
S3	3.2	300	1945	29	16	21	29 (@ 173 mK)	56 (@ 220 mK)

*Sample S1 had silicon oxide between leads and subchip, and therefore, the effective area of the phononic heat contact, 137 μm^2, is larger than the junction area 2.0 μm^2.

model for heating due to the finite subgap resistance $R_{gap} = R_T/\gamma$ of nonideal tunnel junctions (γ is the dimensionless leakage parameter), which can originate, e.g., from quasiparticle states within Δ (34) or traps and dopants in Sm-S junctions (32). This leakage can be obtained from the I-V curves at low temperatures (see section S2).

The electronic refrigeration results with the suspended Sm-S junctions fabricated directly on the subchip are presented in Fig. 2A. Direct refrigeration of both electrons and phonons of the macroscopic subchip is enabled by large degenerately doped subchip and the phonon transport and transmission bottlenecks between the subchip and the main chip. The former assures negligible thermal resistance between electrons and phonons, and the latter brings in the thermal isolation. Note that this is in strong contrast to previous works, in which the NIS junctions on the substrate at bath temperature refrigerated directly only the electrons of the normal metal, and the phonons in the immediate vicinity of the junctions stayed essentially at bath temperature due to the weak electron-phonon coupling (17). Refrigeration of the phonon system of a payload with earlier NIS junction coolers has required an indirect method based on high (low) thermal conductivity of the electron (phonon) system of a normal-metal cold finger combined with electron-phonon coupling near the payload (23–25).

Our best-performing sample is S2 (subchip with 1-mm diameter and 0.4-mm height). Its maximal absolute and relative temperature reductions are 83 mK (at 244 mK) and 40% (at 170 mK), respectively. The cooling power for this sample is about 2 pW/μm^2 at 300 mK, which is of similar magnitude as those achieved with the most efficient NIS junctions (28). The calculated curves of Fig. 2A are obtained by finding the subchip temperature T_2 that satisfies the equation $P_{SmS,cool}(T_2) = (T_1^4 - T_2^4)/(4\alpha)$, where the right-hand side is the heat leak from the main chip (temperature T_1) to the subchip (see Eq. 2 in Materials and Methods and discussion in the next section). The values for parameter α (see Table 1) are determined from the thermal resistance measurements of Fig. 2B, and parameters for $P_{SmS,cool}$ (Eq. 1) are obtained from separate I-V curve calculations (see section S2). The obtained temperatures fit the experimental data well when the subgap leakage resistance is taken into account.

It should be noted that similar cooling performance has been achieved earlier with NIS coolers using the traditional normal-metal cold finger approach. These previous results include, for example, refrigeration of a $(250 \ \mu m)^3$ cube from 320 to 225 mK (25) and a 1.9-cm^3 copper stage from 290 to 256 mK (24) and refrigeration of phonons in 1×1 mm^2 silicon nitride membrane from 305 down to 200 mK (28) and in suspended nanowires from about 100 to 42 mK (29). However, our approach, where electron cooling and thermal

coupling/leakage to the environment take place through the junctions, simplifies the refrigerator design and provides important benefits. These are, for example, substantial enhancement of the total cooling power (no areal limitations due to the absence of cold fingers) and a similar structure as with thermoelectric coolers operating at elevated temperatures. Our approach is particularly important for enabling practical multistage refrigerators (see section on "Future prospects" for details).

Characterization of heat transfer

The heat flux from the main chip to the subchip can be represented by the total thermal resistance R, the measurement results of which are shown in Fig. 2B. The heat flows mainly via the superconducting leads and tunnel junctions. Quasiparticle backflow from the superconductor is also notable in some cases (see sections S3, S4, and S8). Electronic heat leakage through the tunnel junction is effectively blocked by the superconducting energy gap and the tunneling resistance. In addition, the thermal coupling between the electron and phonon systems in the superconductor is suppressed at low temperatures. Therefore, we view the system as two (phononic) thermal resistances in series: the Al-Si interface and the aluminum lead, as shown in Fig. 1D. The effect of increased electron-phonon coupling at higher temperatures is further discussed in section S6.

The thermal resistance, R, of Fig. 2B was measured by biasing a set of the cooler junctions above Δ, which results in heating P_{SmS}. Then, $R = \delta T/P_{SmS}$, where $\delta T = T_2 - T_1$ is the measured temperature difference (see Materials and Methods and section S5). The experimental data follow closely the fitted lines with T^{-3} dependence, which is expected for both the thermal boundary resistance of the Al-Si interface (35) and the phonon thermal resistance arising from polycrystalline aluminum wires (36), which can be described by the Debye model.

Table 1 compares the fitted prefactors, α, of thermal resistance $R(T) = \alpha T^{-3}$ to the expected thermal boundary resistance (R_{PTB}) based on acoustic mismatch (AMM) and diffusive mismatch (DMM) models (35). The former is based on ballistic transmission of acoustic waves limited by the AMM due to different material properties of Al and Si, whereas the latter is based on diffusive scattering at the interface. The phonon thermal resistance of the aluminum leads, R_{lead}, can be of the same order of magnitude as R_{PTB}, but it depends on phonon mean free path, which is not well known. However, R_{PTB} is proportional to the interface area between the subchip and leads, whereas R_{lead} is the same in all samples. We summarize the results as follows (for detailed analysis and discussion, see sections S5 to S7): (i) Because of the large interface area (see Table 1), the thermal
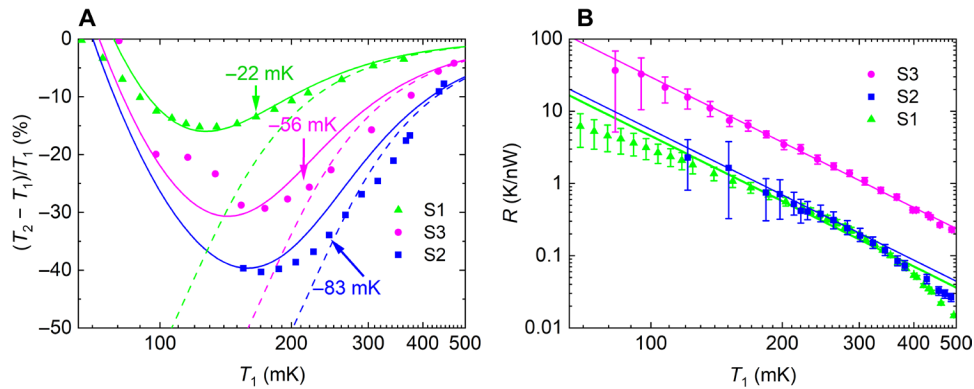
Fig. 2. Measurement results. (**A**) Relative difference between the subchip temperature T_2 and bath temperature T_1 for samples S1, S2, and S3 at optimal cooling voltage with 22, 20, and 22 cooler junctions, respectively. The largest absolute temperature reduction is indicated by arrows. Refrigeration is modeled by setting the heat leak (T^{-3} fits of B) in balance with the cooling power produced by ideal Sm-S junctions (dashed curves) or by Sm-S junctions that have finite subgap leakage (solid curves). (**B**) Thermal resistance between the subchip and its environment for samples S1, S2, and S3, and T^{-3} fits (solid lines). Error margins are dominated by the uncertainty of simulation parameters and by measurement uncertainty (see section S8 for details).

resistance of sample S1 constitutes mainly from that of the leads. (ii) The thermal resistance of sample S3 is dominated by the phononic interfacial thermal resistance resulting in that R is close to the AMM and DMM values. (iii) The thermal resistance of S2 is close to both that of S1 and the theories for R_{PTB} and is likely to have contributions from both R_{PTB} and R_{lead}. We cannot rule out near-field heat transfer effects (*37*) either: S2 has the largest surface area, and the thermal photon wavelength exceeds the subchip to main-chip distance by several orders of magnitude. (iv) At higher temperatures, thermal resistances decrease below the fits for samples S1 and S2. This originates most likely from the increased electron-phonon coupling in the leads, which creates an additional heat conduction channel (see section S6).

Future prospects

The cooling power of Sm-S junctions can be increased to allow larger payloads simply by increasing the number of junctions. However, the enhancement of the electrothermal performance, i.e., reduction in achievable minimum temperature, requires the increase in cooling power compared with the heat leak from the environment. In addition to limiting the heat flow, this can also be done by decreasing the subgap leakage and/or tunneling resistance (see Eq. 1). Note that our coolers had $\gamma \approx 4 \dots 5.5 \times 10^{-3}$, but $\gamma \sim 10^{-4}$ has been achieved in (*32*). Furthermore, we estimate that the characteristic junction resistance can be decreased to about $100\ \Omega\mu m^2$. Figure 3A shows that, using these parameters and the thermal resistance of sample S3, maximum relative refrigeration of about 80% can be achieved with Al-Si junctions in a narrow temperature range. These junctions are already close to the regime where the refrigeration is limited by γ at low temperatures and mainly by the superconductor temperature, T_S, at high temperatures instead of the phonon transport, which means that R_{PTB} is a sufficient thermal barrier for Al-based refrigeration.

The applicable cooling regime depends on the critical temperature of the superconductor, $T_c \approx \Delta/1.764 k_B$. A vanadium-based ($T_{c,V} = 5.4\ K$) cooler has been experimentally demonstrated to yield improved performance over aluminum ($T_{c,Al} = 1.2\ K$) at higher temperatures (*38*). However, the cooling power follows $P \propto \Delta^2 f(T/T_c)$, where f is a function independent of Δ (see Eq. 1), whereas the heat leaks follow $\dot{Q} \propto \alpha T^4 \propto \alpha \Delta^4 (T/T_c)^4$ (see Eq. 2 in Materials and Methods), which have a different Δ dependence when T is scaled with T_c. Therefore,

in Fig. 3A, V-Si junctions are in the regime where refrigeration would benefit from improved thermal isolation.

Nanoscale effects of phonon heat conduction are actively studied for, e.g., improved thermal barriers, higher efficiency of energy harvesting, and thermal management of nanoscale electronics (*30, 31*). Our concept can notably benefit from phonon engineering methodology, where phonon transport is further suppressed, e.g., at the subchip by using a superlattice close to the tunnel junctions or at the tunnel junction interface by weakening chemical bonding (*30*). However, the most straightforward and practical approach is to constrict the superconducting lead by multiple nanowires (*29*). When the diameter of the nanowire is reduced, the phonon mean free path and thermal resistivity scale with the diameter, but the electrical normal-state resistivity is affected very little (*39*). In this diffusive limit, increasing R_{ph} by factor of 20 would move the vanadium line in Fig. 3A to the regime of sufficient phonon heat blockade. Without scattering, the upper (lower) limit of thermal resistance (conductance) is set by the thermal conductance quantum $G_0 = 1/R_0 = \pi^2 k_B^2 T/3h$, where h is the Planck constant (*40, 41*). Note, however, that the thermal conductance can even be a fraction of G_0 when scattering is introduced [see, e.g., (*29*)]. Figure 3B shows simulations where heat leak follows the thermal conductance quantum model $\dot{Q} \propto G_0 T \propto \Delta^2 (T/T_c)^2$ and, thus, has the same Δ dependence as the cooling power. The scattering effects are incorporated in the effective number of thermal conductance quanta, N (see Fig. 3), which can be lower than unity.

Figure 3C collates the simulation data on improved junctions and improved thermal resistance. The figure also shows cooling simulations obtained by cascading devices with superconductors with different Δ (V- and Al-based junctions). We envision that the cascaded cooler should follow the scheme shown in Fig. 3D, which is closer to the one used in commercial thermoelectric coolers than in typical NIS cascade coolers (*42, 43*). Our simulations demonstrate the effects of two levels of improved R_{ph}: when it is increased by factor 10 and when it reaches the thermal conductance quantum limit. As a result, V-based refrigeration is markedly improved, whereas an Al-based device is only slightly affected. These simple models omit quasiparticle effects, but section S9 shows that temperature reduction of about 50% per refrigeration stage can be achieved up to about 1.5 K also when quasiparticles are taken into account.
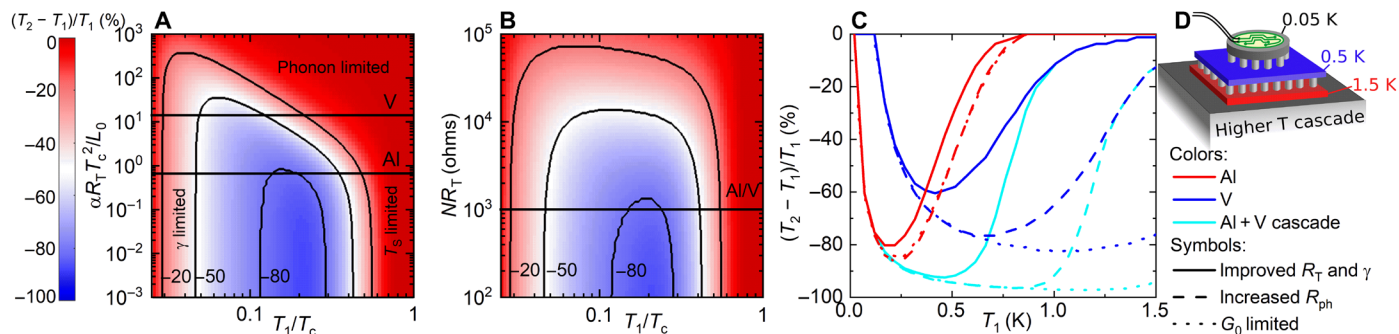
Fig. 3. Future prospects. (**A** and **B**) The achievable relative temperature reduction with any superconductor with critical temperature T_c when $\gamma = 10^{-3}$. The horizontal lines are calculated with $R_A = 100 \ \Omega\mu m^2$. (A) Cooling against R_{PTB}. The y axis is normalized with Lorentz number, L_0. Black horizontal lines show values for aluminum-based ($T_{c, \ Al} = 1.184$ K) and vanadium-based ($T_{c, \ V} = 5.38$ K) junctions, when parameters of S3 are used for R_{ph}, and correspond to the solid lines in (C). (B) Constriction-limited cooling as a function of NR_T, where N is the effective number of thermal conductance quanta in the constriction, and it incorporates the possible effects of scattering/low transmission (i.e., N can be even below unity). The black horizontal line corresponds to the dotted lines in (C) and is calculated when N equals 10 quanta per tunnel resistance of $R_T = 100$ ohms. (**C**) Refrigeration efficiency of aluminum-based (red), vanadium-based (blue), and their cascade-based (cyan) coolers as a function of temperature. The tunnel junction parameters are as in (A) and (B). In the cascade, vanadium-silicon junctions (having much higher optimal cooling temperature than Al-Si junctions) are used to refrigerate aluminum down to a temperature at which Al-Si junctions operate effectively, and Al-Si junctions refrigerate the actual payload to the minimum temperature. The solid lines indicate a case where R_{ph} is the same as in S3. The dashed lines present a situation where R_{ph} is increased by factor 10, and the dotted lines present the temperature reduction when R_{PTB} is as in S3, but R_{lead} is increased by the constriction as in (B). (**D**) Artistic image of a cascaded cooler.

In addition to compact coolers, electrothermal elements can be used in thermal photodetectors monitoring continuous intensity (bolometers) and single photons/energy pulses (calorimeters) (*5, 18, 44–46*). Let us focus here on THz bolometers, where the energy flux of the incoming photons is converted to a temperature rise of an absorber. Sensitivity of a bolometer is characterized by noise equivalent power (NEP), which describes the minimum detectable power (in 1-Hz bandwidth), and it includes all electronic and thermal/phonon noise components (see section S10 for details). In the case of the technology described in this work, a bolometer can be constructed, for example, by using the phonon-blocked junction as the detector and thermal isolation, when the photon-generated heat flows to the bath, similarly as in Fig. 1 (from 2 to 1, 2 being the absorber), creating an electrical signal that is used for detecting the radiation. In this configuration, the S electrodes form an antenna that couples THz radiation into the Sm absorber, and the Sm-S junctions are biased to cool the Sm island similarly to (*44, 45*), where the bolometers work against the volumetric electron-phonon coupling. With V-Si junctions with similar phonon engineering methodologies as in Fig. 3C (the dashed lines), we find NEP of $\sim 30 \ aW/Hz^{1/2}$ (see section S10), which is enough, e.g., for all ground-based THz radio astronomy observations, which are limited by the background of the atmosphere. Another approach is to have S-Sm-S bolometer (*45*) on the cascade platform reaching 0.3 K (0.1 K) from a bath temperature of $\sim$1.5 K. This leads to a THz bolometer that has NEP of $\sim 3 \ aW/Hz^{1/2}$ (0.1 $aW/Hz^{1/2}$) at 0.3 K (0.1 K; see section S10). Note that an NEP of 0.1 $aW/Hz^{1/2}$ is enough even for high-sensitivity space-based radio astronomy observations. This sensitivity has been available only with bulky sub–1 K cryostats, which increase the detrimental payload of space missions.

DISCUSSION

In summary, we have proposed and demonstrated efficient thermionic operation and phonon transfer blocking in solid-state junctions.

We used Si-Al Sm-S junctions, where the thermionic operation arises from the superconducting gap, and the phonon transfer blocking naturally occurs because of phonon thermal boundary resistance. The ultimate figure of merit of a thermionic junction is its ability to cool a thermal mass below the bath temperature, and we demonstrated relative cooling of 40% of a millimeter-scale suspended silicon chip. We suggested, supported by simulations, phonon engineering methods to reach cooling from above 1 K to sub–1 K temperatures, which can enable replacing cryo-liquid–based refrigeration stages by solid-state ones, for example, in the field of quantum technologies. Phonon-isolated thermionic junctions can also be used in thermal energy harvesting and different thermal photodetectors, which have vast applications from chemical sensing to security and radio astronomy. Here, we showed by simulations how to use the junctions in the realization of ultrasensitive photodetectors. Molecular junctions exhibit strong phonon isolation, and these could be used in realizing the ultimate scaled-down limit of the thermionic concepts discussed in this work.

MATERIALS AND METHODS
Sample fabrication

We used 400 ± 15 μm thick (100) highly doped n-type (red phosphorous) 150-mm silicon wafers, with resistivity 1.1 to 1.7 milliohm·cm as a substrate. The surface conductivity of the wafer was further increased by implanting $4 \times 10^{15} \ cm^{-2}$ 27-keV phosphorous ions to reduce the Schottky barrier between Al and Si. Low-pressure chemical vapor deposition with tetraethyl orthosilicate was used to deposit a 476-nm-thick SiO_2 film, and the wafers were annealed at 950°C to densify the oxide and to activate the implanted ions as well as to heal the implantation damage. Ultraviolet (UV) stepper lithography, reactive plasma etching, and wet etching were used to pattern contact holes through the oxide. Silicon–silicon oxide–aluminum tunnel junctions were fabricated as described in (*32*). The thickness of the sputter-deposited aluminum film was 1000 nm, and it was patterned with UV lithography and chlorine-based reactive

plasma etching to form the electrodes. AlOx hard mask was prepared to the backside of the wafer. The hard mask was patterned with UV lithography, and it was used for etching through the wafer (Bosch process) to release the subchips. The deposited silicon oxide on top of the wafer acted as an etch stop layer. Last, the excess silicon oxide was removed with HF vapor to finalize the release.

Measurement setup
The samples were cooled in a dilution refrigerator with the minimum temperature of about 20 mK. Each sample had, in total, 24 Sm-S junctions. One pair of junctions was used as a thermometer, and 1 to 11 pairs as coolers. Because of the limited number of cables in the cryostat, some Sm-S junctions were biased using a common cable. Since the resistance of the cabling between the sample and the measurement equipment was large (around 1240 ohms per cable) compared with the junction tunneling resistance (from 50 to 620 ohms), the cooler voltages were determined by four-probe measurements when necessary. Unused junctions were left floating. The schematics of the measurement setup is presented in fig. S1 of section S1.

Thermometry
Since the Sm-S junction is sensitive to temperature, its current-voltage (*I-V*) characteristics can be used for thermometry. However, since the subchip is entirely conductive, but has finite resistivity, the cooler/heater bias voltages can cause a voltage gradient to the subchip, which adds to the voltages over the thermometer junctions. We used alternating current (ac) measurements for reading the temperature to be sure that we only detect the voltage over the thermometer junctions. Furthermore, ac methods allow us to galvanically isolate the instrumentation used for thermometry from the subchip and to decrease thermometer-induced heat loads and voltage gradients (see section S1 for details).

In the measurement, a pair of Sm-S junctions was capacitively coupled to the measurement setup and biased with ac ($f = 21.11$ Hz). The resulting ac voltage was measured with a precision voltmeter. The signal was then Fourier transformed, and the peak at drive frequency was recorded. We used a "virtual lock-in" technique based on a precision multimeter instead of a conventional lock-in amplifier since the multimeter has guarding and grounding options that help to avoid ground loops (including those arising from stray capacitances) that are typical for lock-in amplifier-based setups. Furthermore, Fourier transform analysis provides extra information from the noise spectrum, which helps to detect potential problems arising, e.g., from minor mistakes in measurement circuits. See [47] for details.

Each Sm-S thermometer was calibrated against a standard ruthenium oxide thermometer, which, in turn, had been calibrated against a Coulomb blockade thermometer [48]. The measurement configurations are further discussed in section S1 and fig. S1.

Cooling measurements
With samples S1 and S3, 22 of 24 Sm-S junctions were used as coolers and the remaining pair as a thermometer. With S2, we used only 20 junctions for cooling. When possible, cooler junctions were biased as S-Sm-S pairs to keep the subchip at virtual ground.

The optimal bias voltage for cooling depends on temperature. Therefore, each cooler needs to be adjusted both when bath temperature is changed and after additional cooling is provided

by the other cooler junctions (see fig. S4 of section S4 for details). Because of the limited number of cryostat lines, not all S-Sm-S junction pairs could be biased individually, but some of them were used as sets of one to three pairs. Because of this and variation in sample parameters, the optimum voltage of the voltage source was different depending on the cooler.

The optimization scheme for multiple coolers was iterative for S1 and S2: First, the optimum voltage was measured for each cooler, while others were at zero voltage. Then, the procedure was repeated multiple times, but now, the inactive coolers were biased to voltages, which had given the maximum temperature reduction in the previous step. The optimization scheme for S3 was otherwise similar as for S1 and S2, but the bias was optimized separately for each junction instead of pairs of junctions, and the subchip was not at virtual ground.

Thermal resistance measurements
The total thermal resistance between subchip and its environment was measured by heating the subchip electrically with Sm-S junctions and recording its electron temperature increase. For samples S1, S2, and S3, the numbers of junctions used for heating were 2, 4, and 6, respectively. Most heat currents, $\dot{Q}$, originating from a single process, follow

$$\dot{Q} = \frac{1}{\alpha n}\left(T_1^n - T_2^n\right) \qquad (2)$$

where *n* is a constant. Adding more processes can be done by summation. When temperature differences are small, this simplifies to $\dot{Q} = \alpha^{-1} T^{n-1} \delta T$, which gives the thermal resistance $R = \delta T / \dot{Q} = \alpha T^{-n+1}$. In equilibrium, the same amount of heat is inserted and removed from the subchip, and thus, $\dot{Q}$ is equal to the heating or cooling power of Sm-S junctions, which can be written as [20]

$$P_{\mathrm{SmS}}(V, T_2, T_S) = \frac{\Delta^2}{e^2 R_T}\int_{-\infty}^{\infty}d\epsilon(\epsilon - eV/\Delta)\,n(\epsilon, \gamma)\,[f(\epsilon, T_S) - f(\epsilon - eV/\Delta, T_2)] \qquad (3)$$

Here, $f(\epsilon, T_i) = [1 + \exp(\epsilon\Delta/k_B T_i)]^{-1}$ is the Fermi function at temperature T_i, and $n(\epsilon, \gamma) = \mathrm{Re}\,[(\epsilon + i\gamma)/\sqrt{(\epsilon + i\gamma)^2 - 1}]$ is the density of states where nonzero dimensionless leakage parameter γ describes nonidealities in the junctions [33]. The method described in section S3 was used to determine T_S, and other parameters of Eq. 3 were obtained from the *I-V* characteristics (section S2). Thermal resistance is calculated as a linear fit to the P_{SmS} versus ΔT data. In the analysis, we used only data where $|eV| \geq 2\Delta$ and $\Delta T \leq 20$ mK…40 mK. An example plot of the measurement results and further discussion on thermal resistance analysis are presented in section S5 and fig. S5.

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