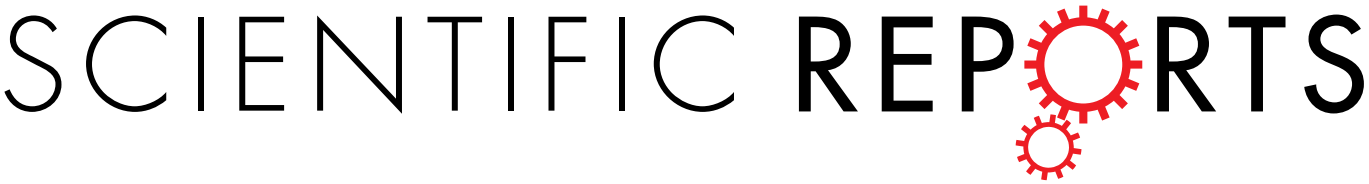

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Electric-field-controlled interface dipole modulation for Si-based memory devices

Received: 3 October 2017
Accepted: 17 May 2018
Published online: 31 May 2018

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Various nonvolatile memory devices have been investigated to replace Si-based flash memories or emulate synaptic plasticity for next-generation neuromorphic computing. A crucial criterion to achieve low-cost high-density memory chips is material compatibility with conventional Si technologies. In this paper, we propose and demonstrate a new memory concept, interface dipole modulation (IDM) memory. IDM can be integrated as a Si field-effect transistor (FET) based memory device. The first demonstration of this concept employed a HfO_2/Si MOS capacitor where the interface monolayer (ML) TiO_2 functions as a dipole modulator. However, this configuration is unsuitable for Si-FET-based devices due to its large interface state density (D_{it}). Consequently, we propose, a multi-stacked amorphous HfO_2/1-ML TiO_2/SiO_2 IDM structure to realize a low D_{it} and a wide memory window. Herein we describe the quasi-static and pulse response characteristics of multi-stacked IDM MOS capacitors and demonstrate flash-type and analog memory operations of an IDM FET device.

Emerging memory devices with various mechanisms have been investigated in an effort to replace Si-based NAND flash memories, which are the most common type of digital storage device, *e.g.*, resistive random access memories (ReRAMs), phase change memories (PCMs), ferroelectric tunnel junctions (FTJs), and ferroelectric field-effect transistors (FeFETs)[1–8]. The advantages of these new devices are a faster operation speed and a higher endurance than a conventional flash memory. Material compatibility with conventional Si device technologies provides a competitive advantage to realize mass production. In particular, Si metal-oxide semiconductor (MOS) FETs used for flash memories are promising building blocks as they provide a high-density three-dimensional memory-cell platform, which can reduce the development cost.

In a flash memory, the electric charge accumulated in the gate stack structure of the MOSFET is read out as the channel current. Similarly, FeFETs utilize the spontaneous polarization of a ferroelectric material integrated in the MOS structure. In particular, ferroelectric HfO_2 is a promising material in terms of Si material compatibility because Hf-based gate oxides are employed in advanced Si complementary MOS devices[7,8]. Various elaborate methods have been proposed to fabricate orthorhombic HfO_2 that acts as a ferroelectric, including doping with Zr, Si, Al, Y, Gd, La, or Sr, and controlling the thermal budget of pure HfO_2 films[9–12]. Indeed, a flash-type memory operation of HfO_2-based FeFET arrays fabricated with an advanced Si-CMOS platform has been demonstrated[8]. Therefore, it is worthwhile to explore HfO_2-based memory materials that are compatible with Si CMOS technology.

Many recent studies have focused on the continuous conductance changes of memory devices because such a change should realize high-efficiency low-power neuromorphic computing[13–17]. The spike-timing-dependent plasticity (STDP) is the most common biological synaptic learning rule. In STDP, the synaptic weight varies with the time difference between presynaptic and postsynaptic neuron spikes. In electronic memory-based synapse devices, electrical pulses (*e.g.*, pulse number, voltage amplitude, width, and polarity) control the conductance change and are utilized to emulate the STDP behavior. As examples, the electric-field-controlled conductive filament in a ReRAM device, the thermally controlled amorphous/crystalline phase change in a PCM device, and the field-controlled ferroelectric domain growth in the FTJ and FeFET devices have been utilized for the STDP operation[13–17]. From the viewpoint of Si-MOS compatibility, HfO_2-FeFET devices are advantageous[17], and the new memory device proposed in this paper has similar advantages.

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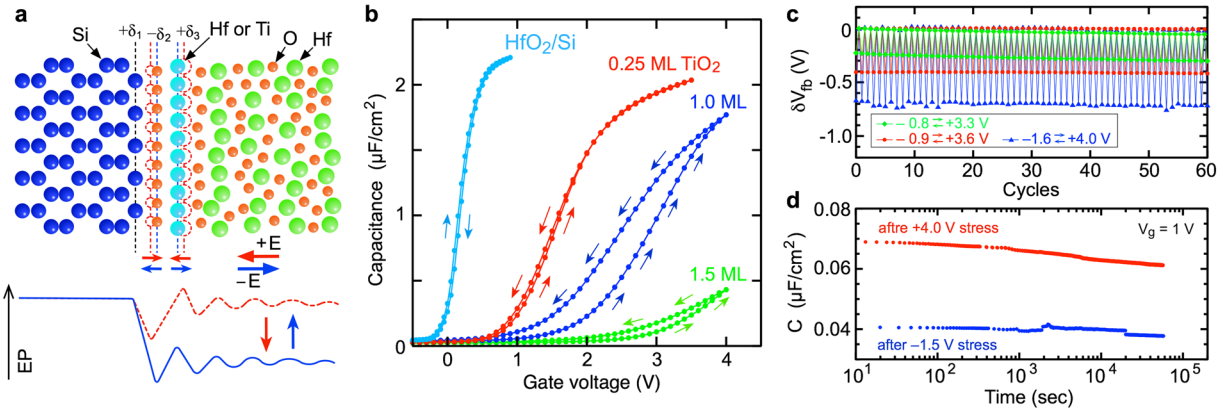

Figure 1. Interface dipole modulation (IDM) concept and experimental demonstration at the HfO_2/Si interface. (**a**) Schematic illustration of dipole formation and IDM operation at the HfO_2/Si interface. Large interface dipoles are observed from the HfO_2/Si structures, which are reasonably explained by the bond polarity mechanism, from ref.[29]. The IDM operation utilizes this mechanism. Dipole strength changes due to the atomic displacement induced by the electric field. (**b**) Effect of the interface TiO_2 layer on the high-frequency capacitance-voltage (*C*-*V*) curves of the 5.5-nm-thick HfO_2/Si MOS capacitors fabricated on n-type Si substrates. Double sweep measurements were performed in the voltage ranges between −1.0 V and the positive voltages shown in this figure. Counterclockwise hysteresis suggests that the IDM behavior appears for the HfO_2/1-monolayer (ML) TiO_2/Si structure. (**c**) Cyclic operation of the HfO_2/1-ML TiO_2/Si IDM device under various voltage sweep conditions. (**d**) Retention characteristics of the HfO_2/1-ML TiO_2/Si IDM device. Large and small capacitance states measured at +1.0 V are plotted as a function of time after applying a stress voltage.

Herein firstly, a new memory concept, interfacial dipole modulation (IDM) occurring at HfO_2/Si and HfO_2/SiO_2 interfaces, is explained and demonstrated. Then the flash-type memory operation and pulse-induced gradual current change of Si-FET-based IDM device are reported.

Controlling interfacial dipoles affects the interface band alignment and is indispensable in the development of semiconductor devices. Thus, dipole formation at a solid/solid interface is well researched. Numerous dipole formation mechanisms have been proposed for metal/semiconductor, semiconductor/semiconductor, and oxide/semiconductor interfaces. These mechanisms are roughly classified into two models: charge transfer due to the interface states and electric polarization of the interface chemical bonds[18–22]. Recently, the interface dipoles formed in HfO_2-based stack structures are well studied because they are related to threshold voltage control of the HfO_2/Si MOSFETs[23–27]. However, the dipole formation in the gate stack structures including the oxide/oxide interfaces is complicated compared to the above interfaces. As the simplest structure, we previously reported that a large dipole (>0.5 V) is formed at the HfO_2/Si interface[28], and proposed a bond polarity mechanism in which positive and negative alternating charged atoms produce a large potential difference between the HfO_2 and Si sides, as shown in Fig. 1a [29,30]. In this model, the polarizations of the interfacial Si-O and O-Hf bonds largely affect the total potential difference because these interface regions have small predicted local dielectric constants compared to Si and HfO_2. This is easily predicted from microscopic dielectric responses based on the chemical gradient[31]. Thus, interface chemical bonding largely influences MOSFETs operations, depending on the strength of interface dipole[32].

The IDM concept originates from the above dipole formation mechanism at the HfO_2/Si interface. If the electric field induced by the gate voltage changes the position of the interface atoms, the interface dipole is supposed to be modulated (Fig. 1a). Since similar switchable interfacial metal-oxygen bonds have been predicted for metal/ferroelectric oxide interfaces using first principles calculations[33], we expect that the IDM operation occurs at the HfO_2/Si interface if an appropriate interface bonding is constructed. The IDM-integrated FET (IDM FET) is expected to behave like FeFET. However, the operation mechanism is completely different. Although switching of spontaneous polarization in a ferroelectric film is utilized in FeFETs, modulation of the dipoles induced in the atomic-scale interface region dominates IDM operation.

The double swept capacitance-voltage (*C*-*V*) trace of the conventional HfO_2/Si MOS capacitor in Fig. 1b does not show any evidence of the IDM operation. A small clockwise hysteresis takes place, indicating charge trapping around the HfO_2/Si interface[34]. Meanwhile, a counterclockwise hysteresis appears when a monolayer-thick TiO_2 is inserted at the HfO_2/Si interface. A particularly large hysteresis (>0.5 V) occurs at the 1-ML TiO_2 interface. A counterclockwise hysteresis indicates charge movement inside the gate stack structure, that is, ferroelectric polarization inversion[6] or an IDM operation. Since the HfO_2 layer is amorphous (Supplementary Fig. S1a), the ferroelectric effect can be excluded.

The hysteresis width strongly depends on the insertion of monolayer TiO_2. It may be reasonable to consider that some structural change of the interface TiO_2 produces a large potential change between the Si and HfO_2 sides. In this manuscript, we call the interface 1-ML TiO_2 a dipole modulator. The fundamental memory function, cyclic modulation, and two-states retention are obtained (Fig. 1c and d). The modulation width strongly depends on the sweep voltage range, and reaches about 0.7 V. This value is comparable to the intrinsic interface dipole observed for the HfO_2/Si interface[28–30]. The long retention can exclude the effect of electron and/or hole

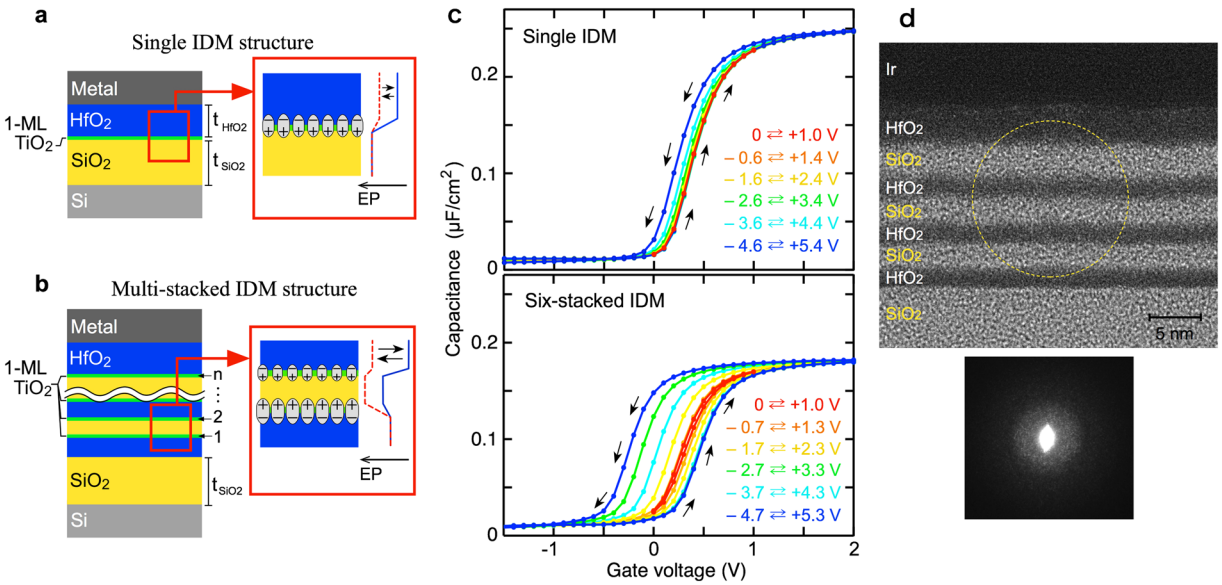

Figure 2. HfO_2/SiO_2-based IDM structures and *C-V* hysteresis curves. (**a** and **b**) Schematic illustration of single and multi-stacked HfO_2/1-ML TiO_2/SiO_2 MOS structures. According to the IDM mechanism, the modulation by the TiO_2 modulators at two facing interfaces are superimposed and enhanced. (**c**) *C-V* curves observed from single and six-stacked IDM MOS capacitors fabricated on n-type Si substrates. The former consists of 3-nm-thick top HfO_2 and 10-nm-thick bottom SiO_2 layer, while the latter consists of 3.5-nm-thick top HfO_2, 1.8-nm-thick inner SiO_2, 1.8-nm-thick inner HfO_2, and 10-nm-thick bottom SiO_2 layers. Small counterclockwise hysteresis appears in a single IDM structure and an obviously large hysteresis appears in the six-stacked IDM structure. (**d**) Transmission electron microscopy (TEM) image and electron diffraction (ED) pattern of the six-stacked IDM structure. These results indicate that all oxide layers are amorphous. Note that it is difficult to distinguish between SiO_2 and TiO_2 in the TEM image.

trapping around the interface because the typical interfacial-charge trapping shows a much shorter response[34,35]. On the other hand, the *C-V* curve for the 1-ML TiO_2 sample is stretched towards a positive bias, indicating that the interface state density (D_{it}) is larger than that of non-TiO_2 interface. Actually, D_{it} of the $HfO_2/TiO_2/Si$ IDM structure is estimated to be about $2 \times 10^{13}\,cm^{-2}\,eV^{-1}$ around the mid-gap energy (Supplementary Fig. S2). This is easily predictable since an electrically switchable TiO_2 layer likely includes large amounts of unstable bonds. Thus, the HfO_2/Si IDM structure is not suitable for FET-based memory devices.

We then explored HfO_2/SiO_2-based IDM structures to solve the interface state problem since inserting a SiO_2 layer should separate the charge traps created around the TiO_2 modulator from the Si surface. Experimental and theoretical studies have been conducted on dipole formation at HfO_2/SiO_2 interfaces. The proposed mechanisms are somewhat complicated compared to those for metal/semiconductor, oxide/semiconductor interfaces, etc. However, most mechanisms for dipole formation at HfO_2/SiO_2 interfaces are based on charge transfer occurring at the HfO_2/SiO_2 interface such as an electronegativity effect around interfacial Hf-O-Si bonding and the movement of oxygen atoms[24–27]. Therefore, we expect an IDM operation in the HfO_2/SiO_2 stack structure when some of the charged atoms around the HfO_2/SiO_2 interface are moved by the gate bias. The HfO_2/1-ML TiO_2/SiO_2 IDM structure (Fig. 2a) exhibits a hysteresis *C-V* curve without displaying stretched-out characteristics (Fig. 2c). Actually, D_{it} estimated for this MOS structure is comparable to that of conventional SiO_2/Si interface ($D_{it} < 1 \times 10^{11}\,cm^{-2}\,eV^{-1}$ around the mid-gap energy, Supplementary Fig. S2c). The *C-V* curve shows a counterclockwise hysteresis as well as the features of the above HfO_2/Si IDM structure. It is obvious that carrier injection from the Si substrate is not the origin of hysteresis. Meanwhile, carrier injection from the gate electrode, that is, carrier trapping by interface TiO_2 potentially results in a counterclockwise hysteresis. However, this mechanism should also be excluded because the hysteresis characteristic is independent of the thickness of the top HfO_2 layer, as explained below. On the other hand, the hysteresis window is obviously small (<0.2 V) and insufficient for memory applications. This probably originates with the difference in the intrinsic dipole strength; that is, the dipole of the HfO_2/SiO_2 interface is reported to be smaller than that of the HfO_2/Si interface[26,28]. One reason for this smaller dipole may be due to disordered chemical bonding at amorphous HfO_2/SiO_2 interfaces.

Amorphous materials can be easily stacked (Fig. 2b). Thus, multi-TiO_2 modulators can be integrated in the same MOS structure. Here, we consider two types of IDM behavior: the upper-HfO_2/lower-SiO_2 and the upper-SiO_2/lower-HfO_2 interfaces. Under an electric field induced by a positive gate bias, the former and the latter dipoles are predicted to increase and decrease, respectively. Under the opposite electric field, the opposite dipole modulations occur. This means that the TiO_2 modulations occurring at two facing interfaces are superimposed and contribute to the enhanced memory window. In fact, a larger hysteresis is observed from the six-stacked HfO_2/1-ML TiO_2/SiO_2 IDM structure (Fig. 2c). Thus, the multi-stacked IDM structure is preferable for memory application.

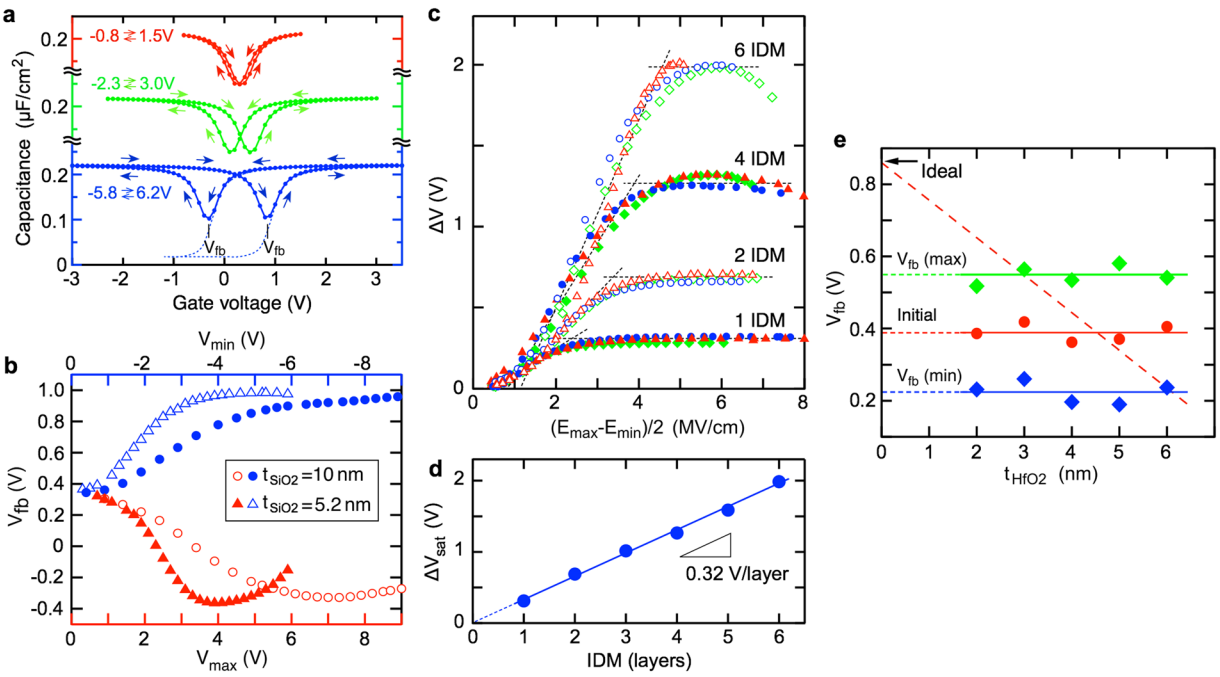

Figure 3. Hysteresis *C-V* characteristics of HfO_2/SiO_2 IDM MOS capacitors. (**a**) *C-V* curves of the four-stacked IDM MOS capacitor consisting of 3.5-nm-thick top HfO_2, 1.8-nm-thick inner SiO_2, 1.8-nm-thick inner HfO_2, and 10-nm-thick bottom SiO_2 layers. Double sweep measurements are performed at 5 kHz under weak light illumination. Sufficient electric fields for both positive and negative bias ranges are produced in the oxide layers. (**b**) Bias dependence of the flat-band voltage (V_{fb}) observed from the four-stacked IDM MOS capacitor. Sample with a thin bottom SiO_2 layer (5.2 nm) exhibits a V_{fb} shift in the lower voltage range compared to a thick bottom SiO_2 layer (10 nm). This difference is almost canceled out in the electric field dependence (Supplementary Fig. 3a), suggesting that the IDM operation is a field driven process. (**c**) Dependence of the modulation width on electric field. Modulation width (ΔV) is the difference between the V_{fb} values of the forward and backward voltage sweeps. (**d**) Dependence of the saturation modulation width, ΔV_{sat}, on the number of IDM layers. The TiO_2 modulator has an ability to modulate the interface dipole by 0.32 V. (**e**) Dipole modulation width of a single IDM structure as a function of HfO_2 thickness. Initial V_{fb}, maximum V_{fb}, and minimum V_{fb} values are not affected by the top HfO_2 thickness (t_{HfO2}). This result suggests that the change in the interface dipole dominates the observed voltage shifts.

The transmission electron microscopy (TEM) image and electron diffraction pattern (Fig. 2d) exhibit that the HfO_2 layers are amorphous. Therefore, the effect of ferroelectric HfO_2 can also be eliminated, even for a multi-stack HfO_2/SiO_2 IDM structure. In general, the formation of a ferroelectric HfO_2 film requires annealing at a temperature above 450 °C and the thinnest HfO_2 film employed in their experiments is 5 nm[7–12,17,36,37]. The annealing temperature of the six-stacked IDM structure shown in Fig. 2d is 350 °C, and the thickness of internal HfO_2 layer is 1.8 nm. It was reported that HfO_2 crystallization hardly occurs when the film thickness becomes thin[38]. Thus, we can reasonably conclude that our IDM structure does not include crystalline HfO_2. In addition, the memory window of the single HfO_2/1-ML TiO_2/SiO_2 IDM structure is independent of the HfO_2 film thickness, as mentioned below. This means that, rather than bulk HfO_2 (*i.e.*, a ferroelectric effect), the interface is a major component in the IDM operation. On the other hand, the HfO_2/SiO_2 interface shown in the TEM image has atomic-scale roughness, indicating that various bonding configurations probably exist at this interface. In the IDM operation, the charge displacement component perpendicular to the interface is considered to contribute to the potential change. The atomically rough interface is probably disadvantageous for the IDM operation. Consequently, if an atomically abrupt interface is formed, the memory window should be further enhanced.

The hysteresis *C-V* curves show that the voltage shift in the forward sweep is smaller than that in the backward sweep (Fig. 2c). This tendency is mainly due to the depletion of minority carriers in the negative voltage range. That is, the Si depletion layer prevents the generation of a sufficient electric field in the oxide layers. To investigate the IDM behavior in both polarity ranges, lower-frequency *C-V* curves were measured under a weak light illumination, which generates sufficient minority carriers. Approximately symmetric shifts of the flat-band voltage (V_{fb}) are observed for both polarities (Fig. 3a and b).

In the case of backward sweeping (*i.e.*, after positive bias stress), the turn-back behavior is recognized for the thinner bottom SiO_2 sample, suggesting that electron injection from Si into the IDM structure through the bottom SiO_2 layer occurs similar to a flash memory[39]. The V_{fb} shift of the thinner bottom SiO_2 sample occurs in the lower voltage region compared to the thicker bottom SiO_2 sample. However, the plot as a function of the electric field agrees well with the observations (Supplementary Fig. S3a). Various IDM structures with different bottom SiO_2 layers (5–10 nm) show consistent electric-field dependences (Fig. 3c). This result suggests that the dipole

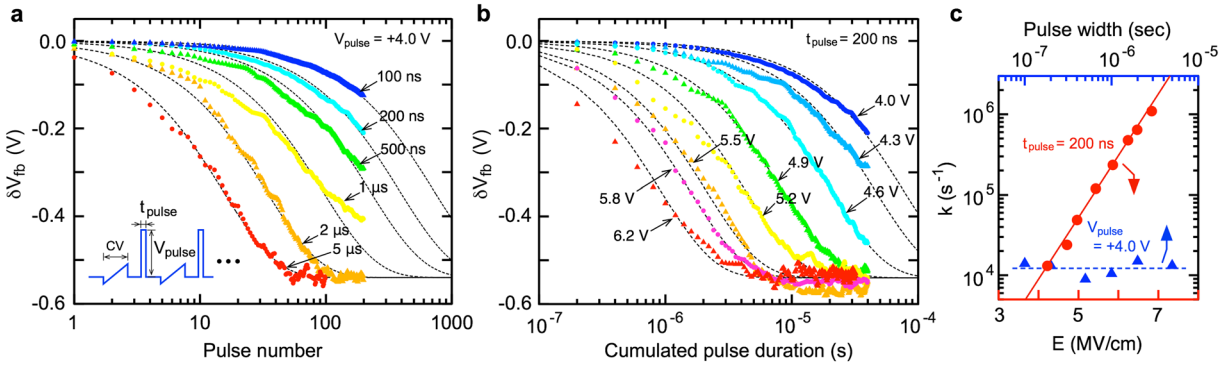

Figure 4. Pulse response characteristics of the four-stacked HfO_2/SiO_2 IDM MOS capacitor. IDM MOS capacitor consists of 3.5-nm-thick top HfO_2, 1.8-nm-thick inner SiO_2, 1.8-nm-thick inner HfO_2, and 5-nm-thick bottom SiO_2 layers. (**a**) V_{fb} shift with various pulse widths and pulse voltage of +4.0 V. The plotted δV_{fb} values show the voltage shifts from the initial V_{fb}. (**b**) V_{fb} shifts with various pulse voltages and a pulse width of 200 nsec. Dotted lines in Fig. 4a,b show the fitting curves based on the random bond breakage/repair model. (**c**) Reaction rate (k) as functions of electric field and pulse width.

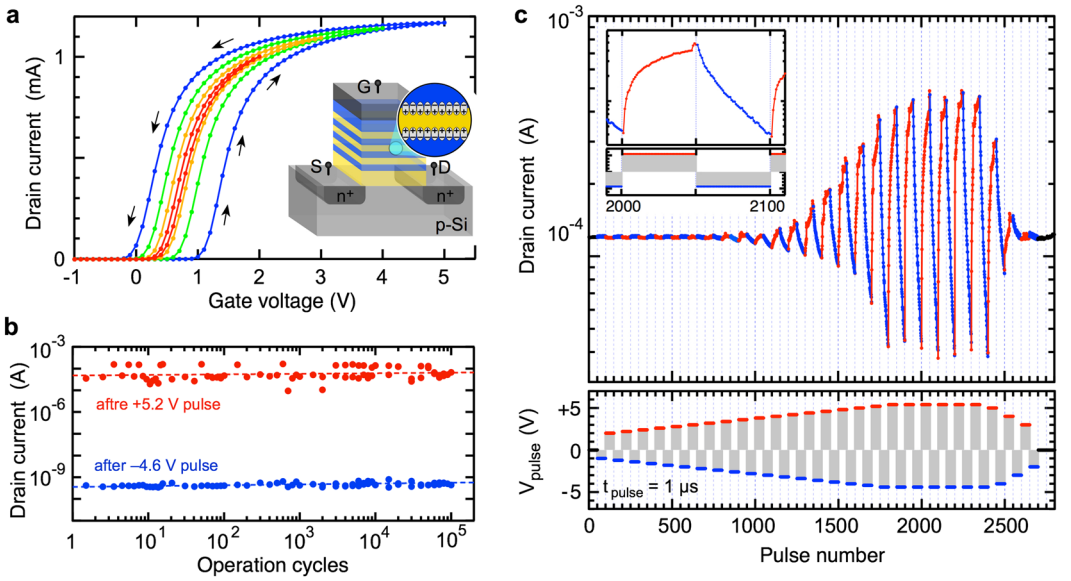

Figure 5. Operation of six-stacked HfO_2/SiO_2 IDM FET. IDM FET consists of 3.5-nm-thick top HfO_2, 1.8-nm-thick inner SiO_2, 1.8-nm-thick inner HfO_2, and 5-nm-thick bottom SiO_2 layers. (**a**) Drain current *vs.* gate voltage ($I_d - V_g$). The drain current of the IDM FET were measured at $V_{ds} = 0.3$ V in various gate voltage ranges: $-1\,V \rightleftarrows +2\,V$, $-2\,V \rightleftarrows +3\,V$, $-3\,V \rightleftarrows +4\,V$, and $-4\,V \rightleftarrows +5\,V$. (**b**) Cyclic switching characteristics. Small and large I_d states are switched by alternatively applying 100-μsec pulses at +5.2 V and −4.6 V. (**c**) Pulse-induced continuous current change. Drain current is monitored at $V_{ds} = +0.3$ V and $V_g = +0.3$ V by applying 1-μsec pulses with various gate voltages. Interface dipoles hardly respond to low absolute voltage pulses ($-2.5\,V < V_{pulse} < +3.5\,V$) and become sensitive to the increase in the absolute voltage outside this range.

modulation is an electric field driven phenomenon. The saturated hysteresis in the high electric field region (*i.e.*, the maximum modulation width) is roughly proportional to the number of IDM layers, assuming the average estimated modulation capability of a single IDM layer is 0.32 V.

It is worth describing the behavior of a single IDM structure to understand the observed hysteresis characteristics. The initial V_{fb} values, which were measured before applying a high electric field, are almost independent of the top HfO_2 thickness (Fig. 3e). Compared to the ideal V_{fb} value estimated from the work function difference between Si and the Ir gate metal [Φ_{MS} (V)], a negative voltage shift takes place. Here we ignore the fixed charges and dipoles in the bottom SiO_2/Si structure according to the previous studies[28–30]. For simplicity, we assume two types of charges at the HfO_2/1ML-TiO_2/SiO_2 interfaces: a positive sheet charge [S_I (cm^{-2})] and a dipole layer with a negative sheet charge on the HfO_2 side and positive on the SiO_2 side [Φ_D (V)]. The dependence of V_{fb} on HfO_2 thickness t_{Hfo_2} (nm)] is expressed as[28,40]

$$V_{FB} = \Phi_{MS} - \frac{qS_I t_{HfO2}}{\varepsilon_{HfO2}} - \Phi_D, \quad (1)$$

where ε_{HfO2} is the dielectric constant of the HfO_2 layer. Equation (1) indicates that V_{fb} should be proportional to the HfO_2 thickness when the unipolar charges dominate the voltage shifts, as shown by the dashed line in Fig. 3e. The observed t_{HfO2} dependence implies that the initial voltage shift is dominated by the interface dipole. The estimated initial dipole strength is about 0.47 V, which is slightly larger than that of the HfO_2/SiO_2 interface[26,28]. The maximum and minimum V_{fb} shifts after applying a high electric field are independent of the HfO_2 thickness, suggesting that the observed field-induced voltage shift is due to the change in dipole strength. It is concluded that the interface dipole in the HfO_2/1-ML TiO_2/SiO_2 IDM system of 0.47 V is modulated by about ± 0.16 V.

The pulse response is an important characteristic when discussing the modulation mechanism as well as when applying it to memory and synaptic devices. In this study, we examined the pulse-induced V_{fb} shift using a repetitive sequence of the *C-V* measurement and pulse application (Fig. 4a, inset). Since the six-stacked IDM structure shows a slightly larger charge trapping effect under a high electric field (Fig. 3c), the four-stacked IDM structure was investigated to examine the IDM pulse response. Figure 4a and b exhibit the strong dependence of the voltage shift on the pulse width [t_{pulse} (sec)] and the pulse voltage [V_{pulse} (V)].

A promising IDM mechanism is the electric-field-induced breakage/repair of the interfacial Ti-O bonds. More simplistically, the bistable switchable state between the broken Ti-O and the repaired Ti-O bonds can be assumed. In other words, the Ti coordination number changes due to the electric field (*e.g.*, between the five-fold and four-fold Ti atom). The thermochemical theory proposed for the breakage of Si-O bonds[41,42] is a sophisticated expression to explain the electric-field-induced bond breakage. The reaction rate, k (s^{-1}), under the electric field, E (V/cm), is given by

$$k = \nu_0 exp\left(-\frac{\Delta H_0^* - p_{eff} E}{k_B T}\right), \quad (2)$$

where ν_0 is the molecular vibrational frequency, which is generally on the order of ~10^{13} (s^{-1}). T and k_B are the temperature (K) and Boltzmann's constant, respectively. Zero-field activation energy [ΔH_0 (eV)] exponentially decreases the reaction rate, while the effective dipole moment [p_{eff} (eÅ)] dominates the electric-field dependence. Hence, these two parameters can be separately deduced from the field dependence of the reaction rate, as described below.

At an actual IDM interface, the large amount of Ti-O bonds (~10^{14} cm^{-2}) contributes to the modulation. In this discussion, we assume the simplest kinetics where the bond breakage/repair process proceeds randomly. This means that the nucleation and domain growth, which are general polarization switching kinetics in ferroelectric films, are neglected[43–45]. The total amount of bonds, θ (cm^{-2}), which suffer from the breakage/repair process from 0 seconds to the specific time, t (sec), follows the rate equation: $d\theta/d\,t = (1-\theta)\cdot k$. Thus, the amount of switched bonds can be given by $\theta(t) = 1 - exp(-k\cdot t)$. After applying a suitable electric field for a sufficient time, δV_{fb} reaches the saturated voltage [δV_{sat} (V)]. The measured time dependence should be expressed as $\delta V_{fb}(t) = \delta V_{sat}\cdot[1 - exp(-k\cdot t)]$. This equation has a good consistency with the measured data, and the reaction rate can be deduced as shown by Fig. 4c.

Significant change is not recognized from the pulse-width dependence shown in Fig. 4c, which suggests that the effect of different time-dependent phenomena such as trap and dipole loss responses[34,35] are not significant in this pulse-width range. From the field dependence shown in Fig. 4c, ΔH_0 and p_{eff} are estimated to be 0.72 eV and 4.6 eÅ, respectively. These parameters are within an acceptable range. For example, the reported bond breakage of $O-Si\equiv O_3$ tetragonal molecules in silica is $\Delta H_0 = 1$–2 eV and $p_{eff} = 7$–13 eÅ, depending on the charge trapping, bond distortion, and the defective structure[41,42]. It has also been reported that Hf-O bond breakage in HfO_2 shows $\Delta H_0 = 4.6$ eV[46]. Obviously, ΔH_0 of the IDM operation is smaller than those of Si-O and Hf-O bond breakages. In addition, the reported breakdown field (E_{bd}) of TiO_2 is 1–2.5 MV/cm, which is smaller than either SiO_2 (15 MV/cm) and HfO_2 (6.7 MV/cm)[42,46,47]. Therefore, we can reasonably consider that the Ti-O bond in the IDM layer is easily broken compared to the Si-O and Hf-O bonds. The displacement of the charged Ti and O atoms associated with the Ti-O bond breakage likely alters the interface dipole of the HfO_2/1-ML TiO_2/SiO_2 structure, as described for HfO_2/1-ML TiO_2/Si structure in Fig. 1a. In the amorphous HfO_2/1-ML TiO_2/SiO_2 structure, various Ti-O bonding configurations may contribute to the IDM operation because such an operation occurs at the amorphous atomically rough interface. However, more elaborate studies are necessary to assign detailed structural changes.

An appropriate hysteresis is observed in the $I_d - V_g$ curve of the FET device with six-stacked HfO_2/SiO_2 IDM structure (Fig. 5a), demonstrating that the IDM phenomena can be read as the channel current. The endurance characteristics observed by alternately applying positive and negative bias pulses show good cyclic switching of 10^5 and a large current difference of about 10^5. However, this memory performance has yet to reach a level to be competitive with advanced HfO_2 FeFET and two-terminal resistance change devices[3–8,48,49]. In particular, the large operation voltage is a serious issue.

We consider that scaling of the equivalent oxide thickness (EOT) is indispensable to suppress the operating voltage because the current multi-stack IDM gate is not optimized in terms of the EOT scaling. Below are prospective ideas for the EOT scaling. (1) Bottom dielectric layer: the 5–10-nm thick SiO_2 bottom layer is employed in the current IDM structures. A thin HfO_2 layer should be effective, provided that a low D_{it} can be maintained. (2) Scaling of inner dielectric layers: the current multi-stack IDM structure employs 1.8-nm thick HfO_2 and SiO_2 layers. Thinning these layers is possible and effective, but the interface abruptness should be simultaneously improved. (3) Material selection of IDM dielectrics: the IDM structure using dipoles induced at high-*k*/high-*k*

interfaces is advantageous compared to the current low-dielectric-constant SiO_2/HfO_2 interface. We expect to realize low-voltage IDM operations using (1)–(3).

Furthermore, we would like to mention an issue with the multi-stack IDM structure, which is shown in Fig. S3c. The retention characteristics are degraded more than the HfO_2/Si IDM structure (Fig. 1d). The depolarization field and the carrier traps are considered to be the major causes[50,51]. For the latter, further studies on the oxide material selection and formation method to eliminate the defects in multi-stack oxide structure are necessary.

The pulse-induced current change was investigated as an application to synaptic devices (Fig. 5c). The current is approximately constant at pulse voltages between −2.5 V and +3.5 V. Outside this range the current change becomes large as the absolute pulse voltage increases. This behavior can be easily understood by the above thermochemical mechanism represented by Eq. (2). An important feature of this mechanism is the threshold voltage, which is an important function in the STDP operation[16,52]. Furthermore, these current changes can be roughly predicted by the above random bond breakage/repair model, which is advantageous in designing synaptic device. STDP operations based on a similar three-terminal FeFET devices have been reported, where the current can be controlled gradually by rectangular or triangular pulses[17,53]. We expect that the STDP operation of IDM FET device can be realized in a similar manner.

In conclusion, the concept of an IDM memory is proposed and demonstrated using HfO_2-based gate stacks of Si MOS devices. In this demonstration, the 1-ML TiO_2 modulator inserted at HfO_2/Si and HfO_2/SiO_2 interfaces plays a major role. The electrical characteristics of multi-stacked HfO_2/1-ML TiO_2/SiO_2 IDM MOS capacitors are investigated in detail because this IDM structure is preferable for Si-FET-based flash memory devices. After fabricating the multi-stacked IDM FET device, its switching operation and pulse-induced current change are presented.

Methods

Oxide deposition. HfO_2, SiO_2, and TiO_2 films were deposited via an ultra-high vacuum evaporation system[30]. Metallic Hf, Si, and Ti were evaporated in oxygen pressure without heating Si substrate. After the formation of HfO_2/TiO_2/Si and $HfO_2/TiO_2/SiO_2$/Si IDM structures, post-deposition annealing was performed at 350–400 °C for 1 min. The x-ray photoelectron spectroscopy confirmed that almost stoichiometric amounts of HfO_2, SiO_2, and TiO_2 were deposited on the substrates by this method. In particular, this evaporation method allows the HfO_2/Si interface with a monolayer thickness to be controlled[28–30,32] and is indispensable to prepare the HfO_2/1-ML TiO_2/Si structure, which was employed in the first demonstration of the IDM concept.

MOS and FET fabrication. The MOS capacitors were prepared on n-type or p-type Si(100) substrates. The bottom SiO_2 layers were grown by thermal oxidation of Si substrates. SiO_2 layers with thicknesses between 5–10 nm were fabricated by hydrofluoric acid etching. For the single IDM structures, top HfO_2 layers of varying thicknesses between 2–6 nm were deposited. For the multi-stack IDM structures, 1.8-nm-thick inner HfO_2, 1.8-nm-thick inner SiO_2, and 3.5-nm-thick top HfO_2 layers were deposited. Ir films were deposited on the oxide layers, and the Ir electrodes (100 × 100 μm) were fabricated by a lithography technique. The MOS FET devices ($L_g = 1$ μm and W = 100 μm) were fabricated by the so-called gate last processes[32]. First, the source/drain regions were fabricated on p-type Si(100) substrates. Second, multi-stack IDM structures with the same thick layers as the above MOS capacitors were fabricated. Finally, the Ir gate electrodes were fabricated by the same method used to prepare the MOS capacitors.

***C-V* measurements and analyses.** The high-frequency *C-V* curves were measured at 1 MHz with a gate voltage sweep from a negative to a positive bias, and then immediately swept in the opposite direction. The lower-frequency *C-V* curves were measured at 5 kHz under weak light irradiation. The flat-band voltage (V_{fb}) was determined by fitting with the ideal *C-V* curve (Fig. 3a). It is difficult to adopt the same method to the *C-V* curves of HfO_2/Si IDM MOS capacitors due to the large stretched characteristics. Figure 1c plots the relative voltage shifts determined by the flat-band capacitor[34,35]. The maximum and minimum electric fields were estimated from the measured maximum capacitances in the accumulation and inversion ranges, respectively.

Pulse response measurements. First, a gate voltage of −4 V was applied as an initialization, shifting V_{fb} to the positive bias direction. Second, 100-times cyclic *C-V* measurements were performed at 1 MHz in the range from −0.4 V to +0.7 V. After this process, V_{fb} was stabilized between 0.35–0.45 V, which is the stable state under these *C-V* measurement conditions, and is defined as the initial V_{fb} (t = 0). Finally, the cyclic sequence of the *C-V* measurement under the same conditions and pulse application was performed (Fig. 4a, inset). The pulse electric field was determined for the initial state by using an ideal MOS *C-V* curve.

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Acknowledgements

This work was supported by JSPS KAKENHI Grant Number 16H02335. Part of the FET fabrication was conducted at the AIST Nano-Processing Facility (AIST-NPF). The author thanks K. Sumita (National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan) for her help with device fabrication. The author also thanks H. Nohira (Tokyo City University, Tokyo, Japan), J. Nara and T. Yamasaki (National Institute for Materials Science, Tsukuba, Japan) for their helpful discussions on the IDM mechanism.

Author Contributions

N.M. carried out the experiment and wrote the paper.

Additional Information

Supplementary information accompanies this paper at https://doi.org/10.1038/s41598-018-26692-y.

Competing Interests: The author declares no competing interests.

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