

Review

Two dimensional semiconducting materials for ultimately scaled transistors

Tianyao Wei,^{1,2,6} Zichao Han,^{1,6} Xinyi Zhong,³ Qingyu Xiao,³ Tao Liu,^{1,4,*} and Du Xiang^{2,4,5,*}

SUMMARY

Two dimensional (2D) semiconductors have been established as promising candidates to break through the short channel effect that existed in Si metal-oxide-semiconductor field-effect-transistor (MOSFET), owing to their unique atomically layered structure and dangling-bond-free surface. The last decade has witnessed the significant progress in the size scaling of 2D transistors by various approaches, in which the physical gate length of the transistors has shrunk from micrometer to sub-one nanometer with superior performance, illustrating their potential as a replacement technology for Si MOSFETs. Here, we review state-of-the-art techniques to achieve ultra-scaled 2D transistors with novel configurations through the scaling of channel, gate, and contact length. We provide comprehensive views of the merits and drawbacks of the ultra-scaled 2D transistors by summarizing the relevant fabrication processes with the corresponding critical parameters achieved. Finally, we identify the key opportunities and challenges for integrating ultra-scaled 2D transistors in the next-generation heterogeneous circuitry.

INTRODUCTION

To meet the stringent requirements raising from the 21st century abundant-data processing, such as big-data analytics, artificial intelligence, and Internet of Things, the continuous miniaturization of Si-based microelectronics has driven the exponential growth of integrated circuits over the past decades (Figure 1). By reducing the size of a single transistor, the total number of transistors per chip has been significantly increased, which greatly enhances the functions of chips at a much lower price. Nevertheless, the miniaturization of Si complementary metal-oxide-semiconductor field-effect-transistors (CMOSFETs) has reached sub-7 nm technology nodes following the Moore's Law, where further down-scaling to achieve higher transistor density, higher speed, and lower power consumption becomes increasingly challenging owing to various parasitic effects arising from the physical limit of bulk materials (Claeys and Simoen, 2017; Iwai, 2004; Kuhn et al., 2010; Wei et al., 2009). Specifically, when the width of the depletion region on the drain side in a FET is comparable to the length of the conducting channel, the dynamics of mobile charge carriers are not merely modulated by the gate electric field, but the drain bias also contributes to the charge injection by lowering the potential barrier (drain-induced barrier lowering, DIBL), leading to the reduction of threshold voltage as well as the increase of off-state current (Al-Mistarihi et al., 2013; Hiblot, 2018). Such situation, termed short channel effects (SCEs), causes drastic degradation in the carrier mobility and sub-threshold characteristics of the Si-based transistors, together with larger leakage floor and higher static power dissipation that hinder their potential in realizing next-generation electronics (Sharma et al., 2014).

In the CMOS industry, the concept of "natural length" provides a characterization of the ultimate transistor scale that strongly depends on the gate and channel thicknesses (Figure 2A) (Chiang, 2014; Dubey et al., 2013; Suddapalli and Nistala, 2019). Typically, in a single-gate three-terminal FET with planar geometry, the switching behavior is governed by a one-dimensional Poisson's equation written as follows (Colinge, 2004):

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\varphi(x)}{\lambda^2} = 0$$

where $\varphi(x)$ describes the potential distribution in the conducting channel from source to drain, $\lambda = \sqrt{\frac{t_{ch}t_{ox}\epsilon_{ch}}{\epsilon_{ox}}}$ is the "natural length." t_{ch} , ϵ_{ch} , t_{ox} , and ϵ_{ox} represent the thickness and dielectric constant of channel material and gate oxide, respectively. Based on the electrostatic description, the "natural length" λ

¹Institute of Optoelectronics, Fudan University, Shanghai 200438, People's Republic of China

²Frontier Institute of Chip and System, Fudan University, Shanghai 200438, People's Republic of China

³Department of Materials Science, Fudan University, Shanghai 200433, People's Republic of China

⁴Zhangjiang Fudan International Innovation Centre, Fudan University, Shanghai 200438, People's Republic of China

⁵Shanghai Qi Zhi Institute, Shanghai 200232, People's Republic of China

⁶These authors contributed equally

*Correspondence: liu_tao@fudan.edu.cn (T.L.), xiang_du@fudan.edu.cn (D.X.)

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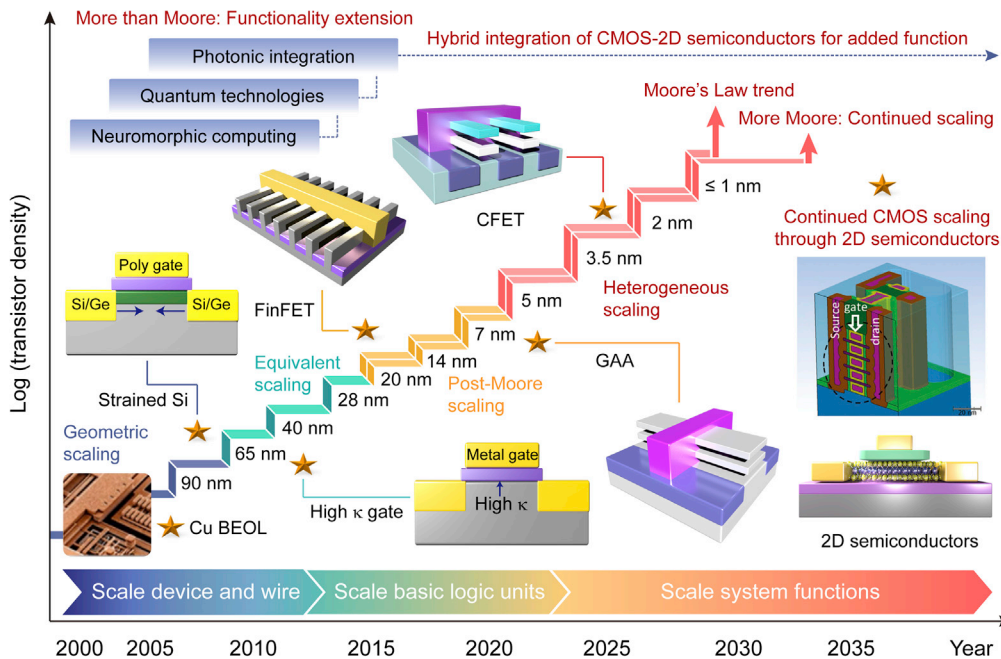


Figure 1. The evolution trend of the technology nodes for Si transistors

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corresponds to the length of the penetration distance of the drain-generated electric field into the channel, giving rise to a direct quantification of the DIBL effect in the channel depletion region. Thus, a smaller λ indicates weakened SCEs on the switching behavior of a transistor, leading to more efficient control of charge injection through the gate electrode (Figure 2B). Tremendous efforts have been devoted to achieving minimized λ by exploring different types of novel device configurations with reduced t_{ox} and t_{ch} , as well as high-quality insulating materials possessing larger ϵ_{ox} (Fischetti et al., 2007; Huang et al., 2017; Kumari et al., 2013; Yadav et al., 2017). However, as the Si-based semiconductor technology enters the sub-10 nm technology node, further decrease of the channel and gate dielectric thicknesses would yield limited success owing to the physical limit of the bulk structures. Ideally, when the ratio between the effective gate length and λ is in the range of 5-10, it is generally enough to avoid the SCEs and produce a reasonable subthreshold behavior (Auth and Plummer, 1997; Colinge, 2004; Ferain et al., 2011; Suzuki et al., 1993; Yan et al., 1992). Unfortunately, this is evidently inaccessible in bulk Si when approaching the extreme scale. For the normal dielectric environment in which t_{ox} and ϵ_{ox} are around 2 nm and 10 respectively, a planar three-terminal Si FET with a channel/gate length of 10 nm would require a channel thickness less than 2 nm under the natural length description. The ultrathin body leads to the significant loss of electrostatic integrity arising from material failure such as defects, surface roughness, and dangling bonds in the channel (Figure 2C) (del Alamo, 2011; Guo et al., 2018; Radamson et al., 2017).

The emergence of 2D materials, particularly the semiconducting transition metal dichalcogenides (TMDs), have attracted intense interests from both scientific and technological perspectives (Chhowalla et al., 2015; Huo et al., 2017; Li et al., 2018; Schaibley et al., 2016). The van der Waals (vdW) layered structure enables the ultimate channel thickness when scaling down to their monolayer limit ($t_{ch} < 1$ nm) while still maintain excellent material integrity with dangling bond-free surface (Figure 2D) (Chhowalla et al., 2016), enabling high carrier mobility even at this extreme scale (Figure 2E) (Podzorov et al., 2004; Tang et al., 2018). The carriers are confined in single or few-atom thick channels in TMD FETs, resulting in the extremely thin channel depletion region and allowing further reduction of the channel/gate length in comparison to the bulk materials, illustrating extraordinary potential in the application of post-Moore electronics (Chou et al., 2021; Das et al., 2021; Guo et al., 2018; Nan et al., 2018). For the case of the 2D FETs in planar configuration, the SCEs-limited natural length λ can be empirically expressed as $\lambda_{2D} = t_{ch} + \frac{\epsilon_{ch}}{\epsilon_{ox}} t_{ox}$ (Dennard et al., 1974). Considering the similar dielectric environment for both Si and TMDs-based transistor technology, the

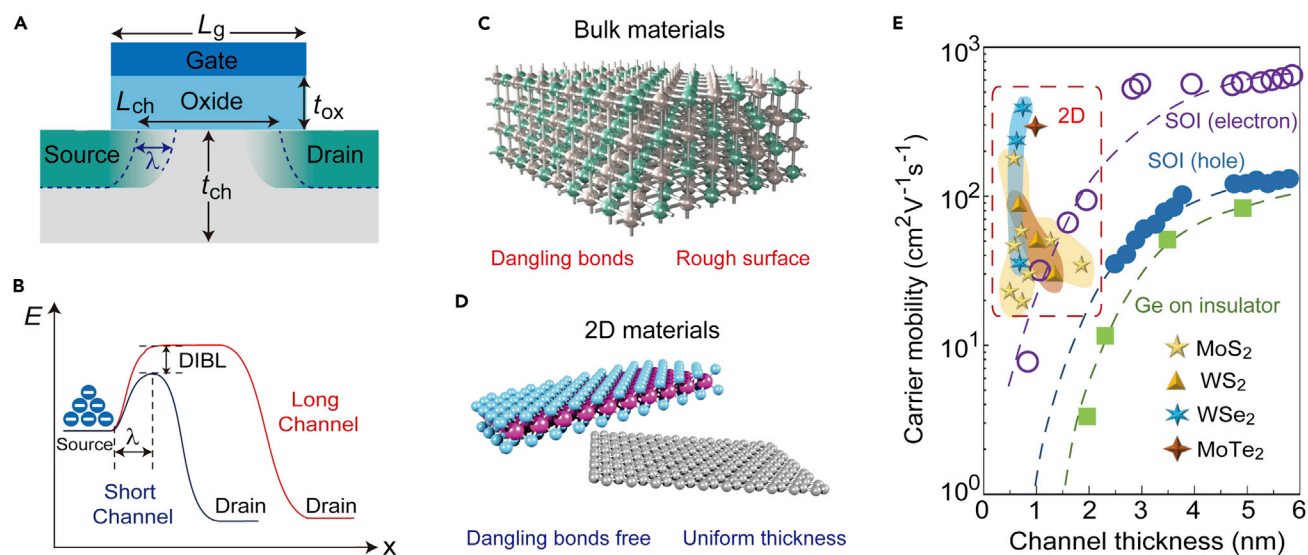


Figure 2. Short channel effects for Si and 2D transistors

(A) Schematic illustration of the Si transistor at the extreme scale.

(B) Energy band diagram of typical transistor in long and short channel configurations. The DIBL and nature length λ are indicated for reference.

(C) The crystalline structure of typical 3D bulk materials with obvious dangling bonds on the rough surface.

(D) The crystalline structure of typical 2D TMD and graphene which are dangling bond free with uniform thickness even scaling down to the atomic layer.

(E) Carrier mobility as a function of channel thickness for both 3D Si (Schmidt et al., 2009; Uchida et al., 2002), Ge (Yu et al., 2015), and typical 2D semiconductors including MoS₂ (Cui et al., 2015; Lembke et al., 2015; Li et al., 2019; Liu et al., 2016a; Shen et al., 2021; Xie et al., 2017; Yu et al., 2016), WS₂ (Alharbi et al., 2017; Ovchinnikov et al., 2014), WSe₂ (Allain and Kis, 2014; Fang et al., 2012; Liu et al., 2013), MoTe₂ (Zhang et al., 2019a). The carrier mobility degrades rapidly in the empirical relationship of $\mu \sim t^{-6}$ for 3D bulk transistors, while the mobility can still maintain above $100 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for 2D transistors.

λ_{2D} would approach 1 nm by employing monolayer TMDs as the channel material, corresponding to an ultra-short gate length less than 10 nm free from SCEs, which is much more favorable to break through the sub-10 nm technological bottleneck than Si (Chhowalla et al., 2016). The electrical transport characteristics of MoS₂ transistors with channel length ranging from 2 μm to 50 nm have been investigated, revealing its outstanding immunity against SCEs compared to that of Si MOSFETs in a similar length scale (Zhang and Appenzeller, 2015). Additionally, the environmental dependence of the SCEs and scaling properties of MoS₂ FETs has also been studied (Liu et al., 2012). Water molecules were found to induce higher p-doping levels in transistors together with a reduction in the effective body thickness, where the latter is owing to the stronger confinement of the electronic wave function within the MoS₂ layers. This work illustrates the opportunity to modulate the electrostatics in ultra-scaled 2D FETs by means of intercalated species. Moreover, the rich band structure of the 2D materials also enables flexible design of diverse novel logic and memory electronics through band engineering (Liu et al., 2020; Manzeli et al., 2017; Zeng et al., 2018). Therefore, the introduction of 2D semiconductors to short-channel devices can ease the challenges in ultra-scaled Si MOSFETs, which contribute to the evolution of post-Moore integrated circuits (ICs) in high speed and high energy efficiency (Das et al., 2021; Manzeli et al., 2017; Zhu et al., 2021).

In this review, we will first discuss the fundamental intrinsic properties of 2D semiconductors such as the band gap, effective mass, carrier and heat transport, illustrating their suitability for short-channel devices. After that, we introduce state-of-the-art strategies for achieving ultra-scaled 2D transistors in the aspects of the channel, gate, and contact length, as shown in Figure 3. For the scaling of the channel length, we mainly focus on the techniques of electron beam lithography and controlled phase transition, and the device configurations based on 2D nanogap, multi-bridge channel, and vertical channel. For the scaling of the gate length, we include transistors with one-dimensional gates, self-aligned engineering, and fin-type structured field-effect-transistor (FinFET) configuration. For the scaling of contact lengths, we focus on edge-contact techniques in the aspects of both top-down and bottom-up strategies, including edge metallization, phase engineering, and heterostructure engineering. Among them, we not only present the innovative techniques and processes but also summarize the achieved parameters for performance evaluation accordingly, which could provide a comprehensive view of ultra-scaled 2D transistors. Finally, we identify key opportunities and challenges for integrating ultra-scaled 2D transistors in the post-Moore era.

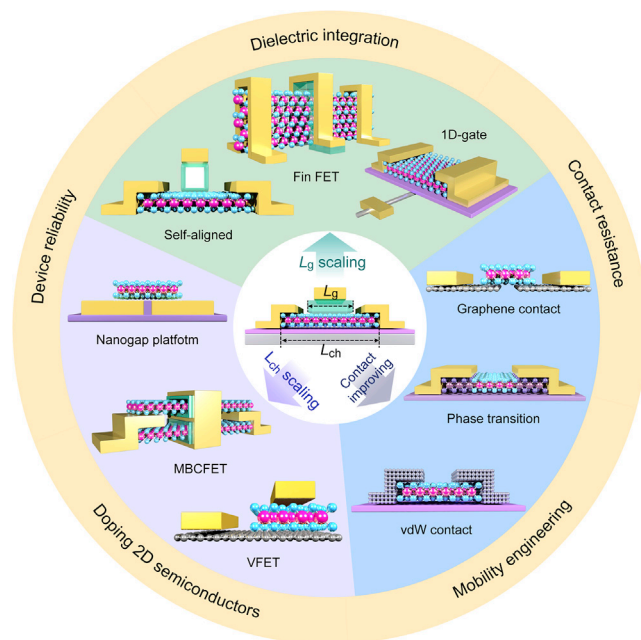


Figure 3. A summary of ultra-scaled 2D transistors achieved through shrinking the channel and gate length, respectively

INTRINSIC PROPERTIES OF 2D SEMICONDUCTORS FOR TRANSISTORS

Although the majority of the scientific community remains optimistic about the prospective of 2D materials in next-generation electronics, it is argued that not all 2D materials are equally suitable for constructing FET channels (Khan et al., 2020). A set of intrinsic properties of 2D semiconductors should be taken into account to evaluate their suitability for high-performance transistors. The most intuitive example is the pristine graphene possessing gapless nature, which has been validated to be fundamentally inconsistent with the requirement for proper operation of semiconducting FETs (Schwierz, 2013). Indeed, a variety of material properties such as bandgap, carrier effective mass, heat transport, and contact resistance, should be considered in a collective and complementary mode to realistically evaluate the suitability of this material family for transistors. In this section, we discuss the applicability of 2D materials in post-Moore FETs, on the basis of their relevant parameters and properties.

Bandgap (E_G) has been identified as a crucial factor influencing the performance of 2D materials-based devices, owing to its decisive effect on the off-state current ($I_{off} \propto \exp\left(\frac{-E_G}{mk_B T}\right)$) and on/off ratio ($\frac{I_{on}}{I_{off}} \propto \exp\left(\frac{E_G}{mk_B T}\right)$) of transistors, where m is a factor of 2 or larger depending on the transistor configuration, k_B is the Boltzmann constant, and T is the temperature (Kim et al., 2011). For example, to ensure the functionality of a logic FET, the bandgap of channel material is required to be at least 400 meV for a sufficiently high on/off ratio and effective switch-off (Kim et al., 2011; Reddy et al., 2011; Schwierz, 2010). As we stated above, the natural graphene sheet behaves as a Dirac semimetal with inherently zero bandgap, which is thus unsuitable to be used as the FET channel materials. Semiconducting TMDs such as MoS_2 and WSe_2 , exhibit intrinsic bandgap ranging from 0.5 to 2.0 eV which is comparable to that of Si (Chaves et al., 2020; Choi et al., 2017; Duan et al., 2015). Moreover, the bandgap of TMDs generally undergoes an indirect-to-direct transition as being thinned down from thicker crystal to monolayer form, offering more flexibility in the demand-driving device design and architecture (Kang et al., 2017b; Lezama et al., 2015; Zhang et al., 2014). Therefore, we could conclude that the semiconducting TMDs possess advantages in satisfying the fundamental criteria for FET channels from the bandgap aspect.

Another significant factor is the charge transport property of the channel materials, where fast response of the charge carriers to the change in external electric field is highly demanded. Device parameters, mainly including the mobility, peak velocity, and saturation velocity, provide direct measurements of the efficiency

of such field response (Cheng et al., 2014; Seo et al., 2016). Among them, high mobility is the most straightforward indicator for a fast-response FET. In the linear regime, the mobility is inversely proportional to the carrier effective mass, suggesting that the lower effective mass is beneficial for achieving higher mobility (Chhowalla et al., 2016). However, as continuously down-scaling the channel length, unfavorable source-to-drain tunneling current starts to emerge in the transistors with extraordinarily high mobility, leading to the performance degradation owing to the weakened electrostatic control on the channel (Cheng et al., 2019; Luo et al., 2021). Moreover, the small effective mass results in a low density of states (DOS), which requires a much larger gate voltage to achieve high on-current, thus causing the degradation of the switching characteristic in the device (Klinkert et al., 2020; Schenk et al., 2020). To resolve this issue, the channel material is expected to possess optimal carrier effective mass to avoid the tunneling current arising from the sizing effect, while maintaining sufficiently high DOS. Previous reports have investigated the tunneling behavior of TMD FETs with 5 nm source-drain distance, where Mo-based TMDs were identified to be more appealing than the W-based counterparts, owing to their optimal effective masses together with sufficiently high mobility (Bernardi et al., 2017; Nichols et al., 2016; Pang et al., 2020).

In addition, the Joule heating in a FET channel originating from the current flow is also a determining factor of the device performance, in which the heat must be effectively released to avoid over-heating-induced degradation. In a standard FET with three-terminal planar structure, efficient heat dissipation requires high thermal conductivity of both the channel and substrate, as well as low thermal boundary resistance at each interface. The thermal conductivity of TMDs is not obviously advanced comparing with Si-based bulk materials as stated in previous reports, thus exploring high-quality dielectric materials with high thermal conductivity and atomically clean interface might be the mainstream for developing TMD-based high-performance FETs (Bae et al., 2019; Liu et al., 2019a; Wang et al., 2014). Won Jong Yoo's group reports that self-heating is impeded along the black phosphorus (BP) and dielectric interface, which leads to a thermal plateau inside the channel and eventual Joule breakdown (Ali et al., 2019). Additionally, the authors extracted the thermal conductance to be $1\text{-}10\text{ mW m}^{-2}\cdot\text{K}^{-1}$ at the BP-dielectric interface by using a size-dependent electro-thermal transport model. Two different dielectric materials including hexagonal boron nitride (h-BN) and SiO_2 are used in the BP devices, in which much higher breakdown power density and electric field endurance together with efficient and homogeneous thermal spreading are observed in the h-BN supported device, owing to its more superior structural and thermal compatibility with BP. This work illustrates that h-BN is more advantageous for efficient cooling in BP devices than that of SiO_2 substrate. To further mitigate the early breakdown and uneven thermal spreading in BP devices, the same group fabricated the devices in the vertical vdW structure. The vertical device possesses 230 times higher field strength and one order enhancement in power sustainability compared with those lateral devices, owing to the integration of thermally favorable constituent materials and the formation of the optimal path for self-heat removal in the vertical configuration (Ahmed et al., 2017). Saptarshi Das's group investigated the current distribution among the individual layers in multilayer 2D systems (Das and Appenzeller, 2013). They found that the "Hot-Spot", which is the centroid of the current distribution, migrates dynamically within the interlayers, resulting in an unusual trend in the effective contact resistance which is mainly determined by the effective interlayer resistance. This work reveals the fundamental information about the charge transport in 2D systems, which may play a crucial role in the implementation of future electronics.

Apart from the above-mentioned intrinsic properties, a semi-extrinsic parameter, the contact resistance, is revealed to be of equal importance for 2D transistors. The ion implantation technique has been widely used to highly dope the contact areas in Si transistors, which is beneficial to realize ultra-low contact resistance below $50\ \Omega\ \mu\text{m}$ (Taylor et al., 2013; Wong et al., 2017). In contrast, direct deposition of bulk metal contacts onto the 2D plane generally introduces gap states that lead to the Fermi level pinning (FLP) effect, usually leading to a large contact resistance in the magnitude of several $\text{k}\Omega\cdot\mu\text{m}$ using TMDs as channel materials (Durán Retamal et al., 2018; Liu et al., 2022). For this reason, various approaches have been developed to eliminate the FLP effect for low Schottky barrier height and contact resistance, such as the transfer of vdW bonded bulk metal, metallic or semi-metallic 2D materials-based electrodes, as well as the phase engineered seamless contacts (Huang et al., 2020a; Schulman et al., 2018). All these strategies address the contact issue to some certain extent, making semiconducting TMDs viable candidates for FETs with proper functionalities. During the submission of this article, we become aware of a review about the structural properties, doping, contact engineering of 2D semiconductors (mainly TMDs), which also provided detailed discussions on the advanced devices beyond CMOS technology (Shen et al., 2022). These contents are equally important for the ultimate device scaling and performance optimization, and we refer to interested readers to this review.

CHANNEL LENGTH SCALING OF TRANSISTORS

The atomically thin feature of 2D semiconductors gives rise to the promise of ultra-scaled transistors beyond the physical limit of Si-based electronics, which inspires intensive research in the design and fabrication of 2D short-channel devices (Chhowalla et al., 2016; Liu et al., 2021c). In this section, we will demonstrate some representative 2D short-channel devices categorized by device configurations and fabrication techniques. The discussion follows a progressive manner in the consideration of the channel length, as well as the innovativeness of the corresponding device fabrication scheme, aiming to provide a comprehensive overview of ultra-scaled 2D transistors achieved by channel length scaling.

Ultrafine electron beam lithography

Electron beam lithography (EBL), a widely incorporated technique in nano-device processing, shows great potential in the direct patterning of short-channel 2D transistors for practical applications (Gao et al., 2018; Jiang et al., 2022; Li et al., 2020b), in which huge progress has been achieved. For instance, Jing Kong's groups (Shen et al., 2021) report monolayer MoS₂ FETs with a channel length of 35 nm utilizing semimetal (Bi) as contacts (Figure 4A), in which a considerably low contact resistance (R_c) of 123 $\Omega \mu\text{m}$ with negligible Schottky barrier height is achieved, owing to the saturation of the metal-induced gap states (Figure 4B). The ultra-low contact resistance promises a record high on-state current density (I_{on}) of 1135 $\mu\text{A} \mu\text{m}^{-1}$ and high carrier saturation velocity (v_{sat}) of $2.5 \times 10^6 \text{ cm s}^{-1}$ at low $V_{ds} = 1.5 \text{ V}$ (Figure 4C), delivering comparable performance to modern silicon transistors with similar dimensions (Figure 4D). It is envisioned that the I_{on} could be further improved to 1800 $\mu\text{A} \mu\text{m}^{-1}$ in a 10-nm-channel monolayer TMD FET at a n_{2D} of $4.5 \times 10^{13} \text{ cm}^{-2}$ in a foreseeable future, which meets the industrial goal of next-generation transistor technologies. This work suggests the feasibility of fabricating 2D short-channel devices by employing the simple lithography processes while ensuring robust device performance via semimetal contacts. Xinran Wang's group fabricated MoS₂ transistors with an even shorter channel length of 20 nm using the same EBL technique (Li et al., 2019). Through employing the monolayer molecular crystal of 3,4,9,10-perylene-tetracarboxylic dianhydride (PTCDA) as a buffer layer, the HfO₂ dielectric with an equivalent oxide thickness (EOT) of 1 nm was successfully integrated with the MoS₂ device (Figure 4E). The breakdown field (E_{bd}) reaches up to 16.5 mV cm^{-1} , and the leakage current can be as low as $\sim 10^{-2} \text{ A} \cdot \text{cm}^{-2}$ at the 1 nm EOT, satisfying the International Technology Roadmap for Semiconductors (ITRS) low-power requirements for CMOS. Thanks to the outstanding characteristics of the PTCDA/HfO₂ gate dielectric, the short-channel MoS₂ transistors exhibit a high carrier mobility of 34 $\text{cm}^2 \text{V}^{-1} \cdot \text{s}^{-1}$, current on/off ratio over 10^7 , and sub-threshold swing (SS) down to 73 $\text{mV} \cdot \text{dec}^{-1}$ (Figure 4F).

It is important to note that the real resolution e.g. feature size and half-pitch of EBL is quantified by the point spread function, which determines the nanoscale energy deposition into the resist (Manfrinato et al., 2014). The overlap of such spread energy profile gives rise to the limitations in the practical pattern density obtained by the single-step EBL approach, making it difficult to further downscale the channel length approaching 10 nm (Manfrinato et al., 2013). On the other hand, decreasing pitch size generally introduces additional challenges in the electrodes lift-off process, which might deteriorate the device performance owing to the rougher edges of the metal contacts (Peng et al., 2014; Tinoco et al., 2017).

By adopting a two-step EBL process, James C. Hone's group (Zhu et al., 2018) successfully fabricated monolayer MoS₂ FETs with a channel length of 14 nm on thin layer HfO₂ dielectric. The source electrodes with a pitch size of 400 nm were firstly patterned and metallized, followed by the deposition of drain electrodes (width >350 nm) between each pair of source contacts via a second EBL cycle (Figure 4G). The as-fabricated transistors exhibit a high current on/off ratio of 3.3×10^6 and a low SS of 86.5 $\text{mV} \cdot \text{dec}^{-1}$ at $V_{ds} = 0.1 \text{ V}$ (Figure 4H). Although the on/off ratio progressively decreases with increasing the bias voltage, it remains over 10^5 when V_{ds} is below 2 V, suggesting the effective immunity to the short-channel effects of the devices (Figure 4I).

While the two-step EBL approach is promising to achieve ultra-scaled 2D transistors, it suffers from the difficulties of precisely positioning the drain electrodes in the middle of the source pairs, leading to the low success rate in device fabrication and the significant variations in the channel length, especially when attempting to further reduce the channel size. Nevertheless, ultrafine EBL is still one of the most powerful tools in processing the ultra-scaled 2D transistors, where intensive engineering in the exposure system might be a potential route toward the realization of sub-10 nm channel length (Manfrinato et al., 2013).

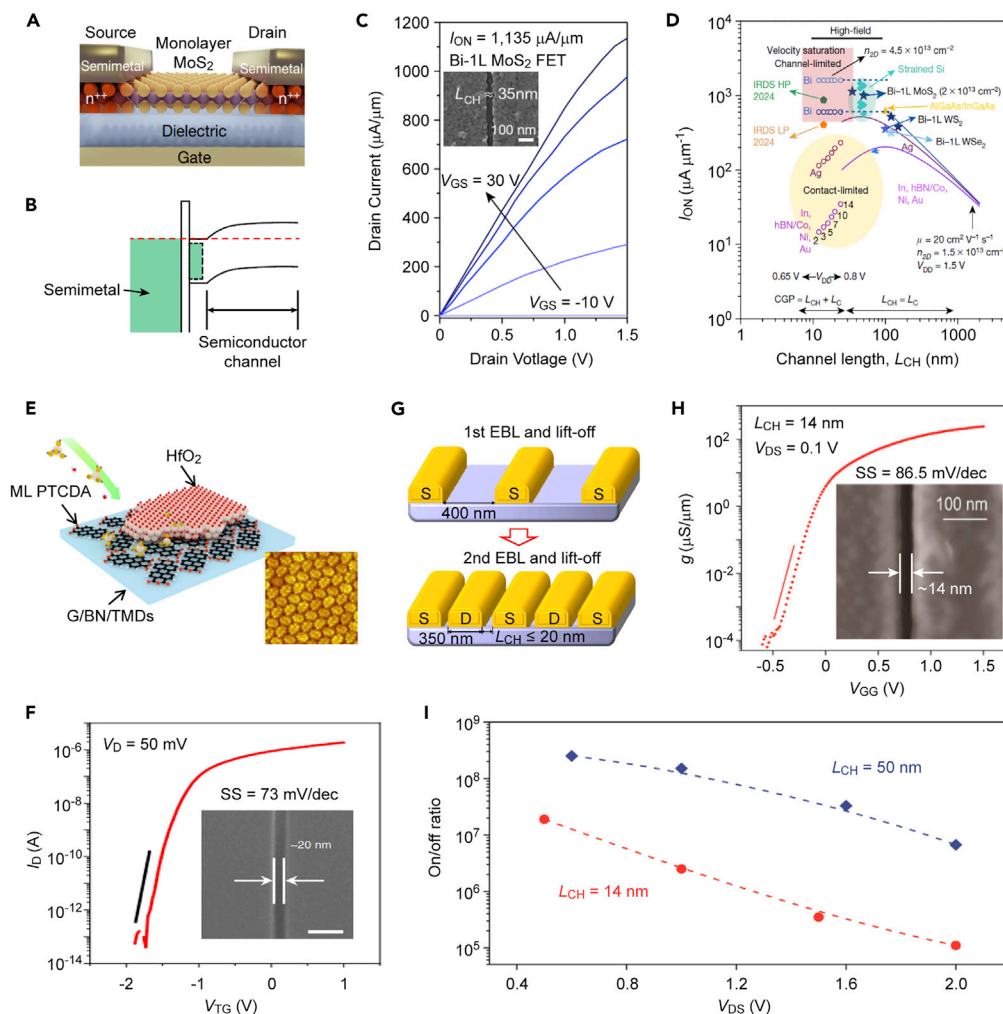


Figure 4. Channel length scaling of 2D transistors based on EBL technology

(A) Schematic of monolayer MoS₂ transistor using semimetal Bicontacts.

(B) Band alignment between semimetal and semiconductor. The metal-induced gap states (MIGS) in semiconductor are saturated when contacting with semimetal, leading to the negligible Schottky barrier height as well as low contact resistance.

(C) Output curves of short channel MoS₂ transistor measuring at different gates from -10 V to 30 V. The maximum I_{ON} can be as high as 1135 $\mu\text{A } \mu\text{m}^{-1}$; Inset shows the SEM image of the as-fabricated device.

(D) Projected I_{ON} as a function channel length for monolayer TMDs transistors using different contact technologies.

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(E) Schematic illustration of the hybrid ML PTCDA/HfO₂ gate stack on 2D materials. Inset: a 10 nm × 10 nm high-resolution STM scan of ML PTCDA on graphene.

(F) Transfer characteristics of the short channel ML MoS₂ transistor using ultrathin PTCDA/HfO₂ gate dielectric. Inset shows the corresponding SEM image of the transistor. Figures E and F are reproduced with permission from (Li et al., 2019) Copyright© 2019, Springer Nature.

(G) Schematic of the two-step EBL fabrication process for achieving the 2D short channel transistors in sub-20 nm.

(H) Transfer characteristics of the ML MoS₂ transistor fabricated by the two-step EBL process; Inset shows the SEM image of the transistor with a channel length of 14 nm.

(I) Current on/off ratio as a function of V_{DS} with a channel length of 14 and 50 nm, respectively. Figures G, H, and I are reproduced with permission from (Zhu et al., 2018) Copyright© 2018, American Chemical Society.

Nanogap

As discussed in the previous section, it is extremely difficult to realize ultra-short channel length without compromising the device yield and performance uniformity in the sub-10 nm regime by solely relying on state-of-the-art EBL-related techniques (Jing et al., 2020). In this context, more innovative methods are to be developed to further reduce the channel dimension with improved precision and controllability. In

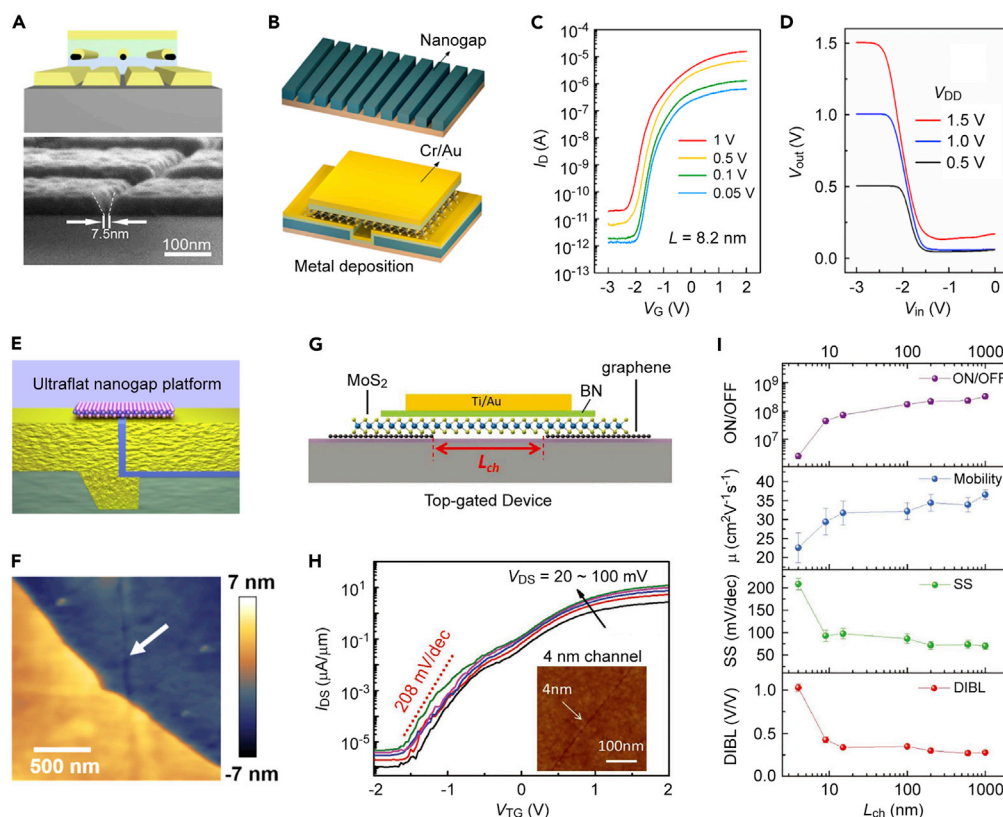


Figure 5. Channel length scaling of 2D transistors with nanogap

(A) Upper: schematic diagram of nanogaps achieved by suspended SWCNT masks; Below: SEM image of the corresponding nanogaps in 7.5 nm. Reproduced with permission from (Xiao et al., 2019) Copyright© 2019, American Chemical Society.

(B) Upper: Schematic diagram of nanogaps on Bi_2O_3 substrate via HNO_3 etching. Below: the as-fabricated short channel MoS_2 transistor in top-gate configuration.

(C) Transfer characteristics of the MoS_2 transistor with channel length of 8.2 nm.

(D) Output characteristics of the inverter based on 2D short-channel transistors. Figures B, C, and D are reproduced with permission from (Xu et al., 2017) Copyright© 2017, American Chemical Society.

(E) Schematic image of the short-channel device fabricated by transferring 2D flakes on top of ultraflat template-stripped metal electrodes with nanoscale gap.

(F) AFM image of MoS_2 flake on Au surface with a nanogap. Figures E and F are reproduced with permission from (Namgung et al., 2021) Copyright© 2021, American Chemical Society.

(G) Schematic illustration of graphene-contacted ultra-short channel MoS_2 transistors in top-gated geometry.

(H) Transfer characteristics of the 4 nm top-gated MoS_2 transistors at different bias voltages from 20 to 100 mV. Inset shows the corresponding AFM image.

(I) Channel length-dependent current on/off ratio, mobilities, SS, and DIBL of back-gated MoS_2 transistors. Figure G, H, I are reproduced with permission from (Xie et al., 2017) Copyright© 2017 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

recent years, 1D structures such as single-walled carbon nanotubes (SWCNTs) and nanowires with ultra-small diameter have been utilized as masks for contact deposition instead of using EBL-patterned resist layers (Bao et al., 2018). In this case, the channel length of transistors is determined by the diameter of these 1D structures, making it possible to access the sub-10 nm regime. For example, Qunqing Li's group reported that horizontally aligned SWCNTs could be suspended above substrates via being clamped by a resist double layer, which serves as masks in the metal deposition process (Xiao et al., 2019). Briefly, the first layer of ZEP-520A resist (mixture of 11% methyl styrene and chloromethyl acrylate copolymer and 89% anisole) was spin-coated onto the substrate, upon which the SWCNTs supported by polymethyl methacrylate (PMMA) was transferred to form a sandwich structure. EBL-defined window was then developed to obtain the suspended SWCNT masks, yielding a series of nanogaps with ~ 7.5 nm in size that defines the channel of transistors after electrode metallization (Figure 5A). This technique enables the fabrication of parallel 2D

short-channel transistors with high successful rate and moderate electrical transport performance, e.g. mobility of $17.4 \text{ cm}^2 \text{ V}^{-1} \cdot \text{s}^{-1}$, SS of $120 \text{ mV} \cdot \text{dec}^{-1}$, and on/off ratio of $\sim 10^7$. Such CNT mask strategy could be further improved by developing guided/self-aligned CNT growth methods to achieve ultra-clean SWCNT arrays with more controllable bundle density and very high degree of alignment (angle SD of $\sim 0.03^\circ$), which are essential to achieve large-scale fabrication of short-channel devices with superior performance and excellent uniformity (Guo et al., 2022; Hong et al., 2010).

In comparison to the CNT mask technique, building the dielectric nanogap platform onto which the 2D materials are transferred could be a more holistic and scalable alternative to achieve short-channel devices (Chen et al., 2021). Jun He's group reported a novel and universal method to fabricate large-scale nanogaps deriving from a corrosion crack along the cleavage plane of $\beta\text{-Bi}_2\text{O}_3$ (Xu et al., 2017). As shown in Figure 5B, the nanogap was formed by consecutive deposition of the HfO_2 dielectric and Au electrodes onto the HNO_3 etched $\beta\text{-Bi}_2\text{O}_3$ layer. Subsequently, monolayer MoS_2 was transferred on top of the electrodes, where an additional layer of HfO_2 was deposited by ALD, serving as the gate dielectric. The resultant MoS_2 transistor possesses a channel length of 8.2 nm defined by the width of the nanogap, exhibiting promising electrical transport performance including low SS of $140\text{-}170 \text{ mV} \cdot \text{dec}^{-1}$, high current density of $\sim 2.5 \mu\text{A} \mu\text{m}^{-1}$, and high current on/off ratio of $10^6\text{-}10^7$, as shown in Figure 5C. The logic inverter based on the short-channel transistors is also demonstrated in this work. The high and low V_{out} corresponding to logic 1 and 0 can be clearly observed in the output curves when gradually increasing the V_{in} , suggesting the potential of scaling 2D logic devices to the sub-10 nm regime (Figure 5D).

Sang-Hyun Oh's group (Namgung et al., 2021) also created the ultra-narrow nanogap through partial etching and re-coating of Al_2O_3 layers at pre-defined thicknesses, together with the deposition of metal electrodes. The whole structure was then mechanically peeled off and flipped to reveal the ultra-flat surfaces consisting of lateral Au- Al_2O_3 -Au structure. 2D flakes could be simply transferred on top of the platform, where the Al_2O_3 nanogap effectively defines the conducting channel with ultra-short length of $\sim 10 \text{ nm}$ (Figure 5E). The AFM image shown in Figure 5F illustrates the clean and smooth surface of the MoS_2 flake and the metal electrodes. It is worth noting that the root-mean-square roughness of the vertically aligned source/drain electrodes can be as low as 0.315 nm by carefully controlling the ALD deposition and chemical etching of the Al_2O_3 dielectric layer, which is essential to enhance the device performance owing to the minimized charge scattering and reduced contact resistance correspondingly (Zheng et al., 2021).

It is noted that the main processing techniques of fabricating the above nanogap-based transistors are wafer-scale compatible, making it possible to achieve the ultra-scaled 2D transistors in arrays for more advanced applications (Jeong et al., 2022). Additionally, the nanogap approach could effectively avoid the surface damage of 2D channels caused by the direct electrode deposition that is commonly observed in the EBL-related procedures even for the CNT mask method, which might degrade the device performance (Radisavljevic et al., 2011). On the other hand, it is worth noting that the minimum size of the nanogap and the corresponding device performance are strongly correlated with the thickness and quality of the ALD-coated dielectric layers. Therefore, it is essential to optimize the growth condition of the dielectric layers, which may achieve the narrower gap, and promote significant advances in nanogap-based high-performance short-channel transistors (Illarionov et al., 2019; Li et al., 2019).

Besides the above-mentioned nano-processing techniques, the intrinsic feature of 2D materials could offer additional opportunities for the realization of ultra-short channels. Guangyu Zhang's group (Xie et al., 2017) reported a graphene-based grain boundary widening technique to fabricate the 2D short-channel FETs. In this work, the 1D grain boundary in monolayer graphene is selectively etched by using hydrogen plasma, resulting in a nanogap with well-defined width. The channel material is then transferred onto the nanogap, where the remaining graphene sheets serve as the source-drain electrodes (Figure 5G). As shown in Figures 5H and 5I, the monolayer graphene-contacted MoS_2 FETs with channel length scaling down to $\sim 4 \text{ nm}$ exhibit promising electrical transport performance including a current on/off ratio of $\sim 2.6 \times 10^6$, off current density of $\sim 5 \text{ pA} \mu\text{m}^{-1}$, SS of $\sim 208 \text{ mV} \cdot \text{dec}^{-1}$, and DIBL of $\sim 1.03 \text{ V V}^{-1}$. This work provides a facile route toward the fabrication of various 2D materials-based devices with nearly Ohmic contacts for ultra-scaled electronics. Recently, Wei Lu et al. reported the fabrication of nanogaps using tilted-angle disposition method. In this work, a two-step deposition approach was utilized to achieve BP-based short-channel devices. In the first step, $4 \mu\text{m}$ channel was defined using UV lithography, followed by the electrode metallization. Secondly, another lithography process was performed, after which the electrode

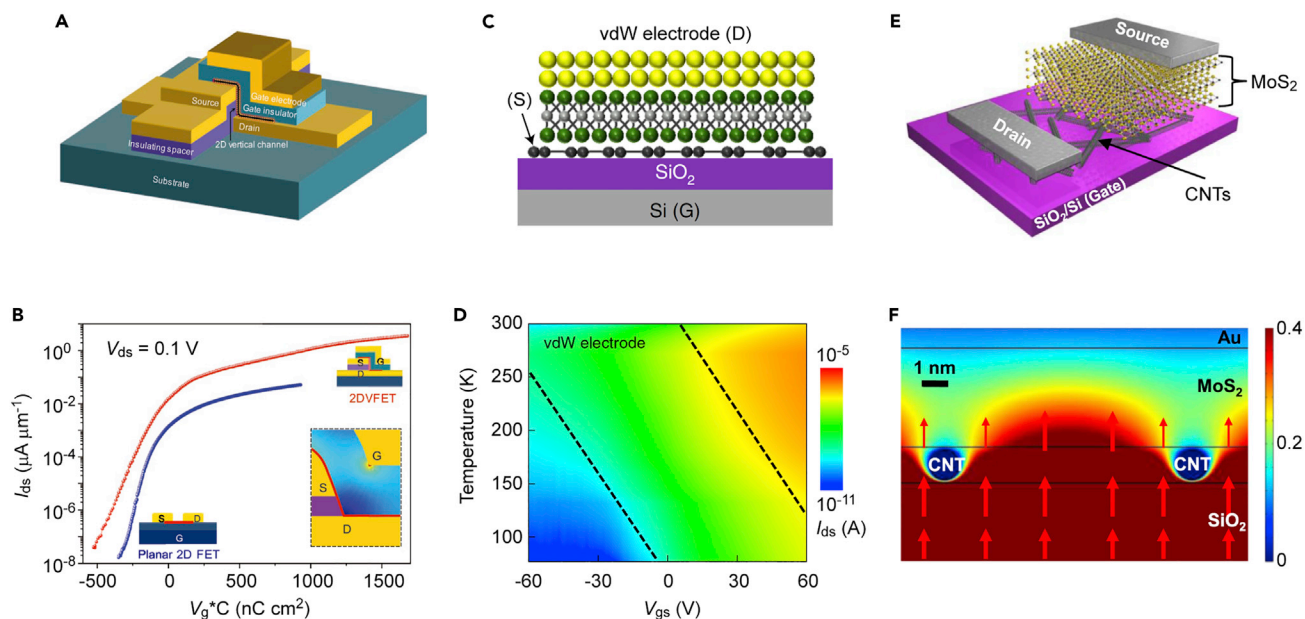


Figure 6. Channel length scaling based on vertical device configuration

(A) Schematic illustration of the 2D vertical FET with mainly six layers which are the bottom electrode, insulating spacer, top electrode, 2D vertical channel, top-side gate insulator, and gate electrode.

(B) Transfer characteristics of the 2D vertical FET and conventional 2D planar FET. Inset: schematic illustration of the local enhancement of electric field in 2D vertical FET. Figures A and B are reproduced with permission from (Jiang et al., 2020) Copyright© 2020 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

(C) Cross-sectional schematic of 2D vertical FET fabricated by using vdW electrodes. The items from bottom to top are graphene, MoS₂, and vdW electrode, respectively.

(D) 2D plot of I_{ds} versus temperature (y axis) and gate voltage (x axis) for the device with vdW electrode. The bias voltage is fixed at 0.5 mV. Figures C and D are reproduced with permission from (Liu et al., 2021b) Copyright© 2021, Springer Nature.

(E) Schematic diagram of the 2D vertical FET based on SWCNT network and MoS₂ heterostructure.

(F) Electrostatic screening effect simulation of the gate electric field in the SWCNT network/MoS₂ heterostructure. The red arrows indicate the electric field from the Si gate through the SWCNT electrode, MoS₂ channel, to the Au metal electrode. Figures E and F are reproduced with permission from (Phan et al., 2019) Copyright© 2019, American Chemical Society.

deposition was conducted along a tilted angle θ instead of the perpendicular direction. The resultant channel lengths ranging from 100 nm to 20 nm can be effectively controlled by adjusting the tilted angle from 65° to 40°. This approach is favourable for improving the sensitivity and response speed of terahertz photodetectors by exploring the photo-thermoelectric effect in an ultra-short 2D channel (Guo et al., 2020).

Vertical channel

In contrast to the general 2D transistors where the planar electrical transport is still preserved, ultra-short vertical conducting channels can be realized by taking advantage of the atomically thin nature of 2D materials. Ideally, the channel length of such vertical transistors is determined by the thickness of 2D flakes, which can be easily down-scaled to the sub-nanometer regime by adopting their monolayer form. Moreover, devices in vertical configuration could offer more flexible integration schemes compared to the strict planar structure (Su et al., 2021; Wang et al., 2021; Zhang et al., 2021).

Recently, Young Hee Lee's group reported 2D vertical FETs by transferring MoS₂ onto the prefabricated source-insulating spacer-drain patterns, in which either the Al₂O₃ film or h-BN was utilized as the spacer and top-gate dielectric (Jiang et al., 2020). Figure 6A schematically illustrates the vertical FET structure, in which the effective channel length is defined by the thickness of the Al₂O₃/h-BN spacer (~10 nm, inset of Figure 6B). The device exhibits excellent electrical transport performance including large on-current density of 70 $\mu\text{A } \mu\text{m}^{-1}$ and high on/off ratio ranging from 10⁷ to 10⁹ by using the chemical vapor deposition (CVD) grown monolayer MoS₂ sample. Figure 6B compares the transport performance of the MoS₂ transistors in both vertical and lateral configurations, where the I_{on} is greatly improved by two orders of magnitude for the vertical device with maintained on/off ratio, suggesting its advantages over the conventional planar

structure (Liu et al., 2018b; Wang et al., 2019). Such vertical configuration is also applicable to other 2D semiconductors with similar performance enhancement, which is verified by the MoTe₂ transistor in ambipolar transport characteristic.

Apart from defining the conductive channel using insulating 2D spacers, sandwiching the semiconducting TMDs between bulk metal and graphene electrodes also enables the realization of a vertical transistor, in which the thickness of the semiconductors directly determines the channel length. By incorporating the method of transferring vdW metal electrodes, Yuan Liu's group (Liu et al., 2021b) reported that the vertical transistor with channel length down to the monolayer scale can be readily achieved (Figure 6C). Arising from the minimized direct tunneling current and FLP effect, the vertical FETs exhibit on/off ratios of 26 and 10³ for channel lengths of 0.65 and 3.60 nm, respectively. The temperature-dependent measurements illustrate that the on/off ratio of the 3.0 nm channel length device is around 758 at room temperature, which is greatly improved to ~10⁵ at 77 K (Figure 6D). This behavior indicates that the thermionic emission mechanism governs carrier transport in the vertical device with the optimized metal contacts using vdW integration, in great contrast to the tunneling leakage current dominated traditional devices under direct metal deposition (Zhang et al., 2021). Jonghwa Eom's group demonstrated a vertical FET in a similar structure, in which multilayer MoS₂ was used as the channel material. The corresponding device exhibits a large current density of 10⁵ A·cm⁻² and a high current on/off ratio of ~10⁶ (Farooq Khan et al., 2017).

It is noted that the semi-metallic nature of graphene could significantly weaken the back-gate electrostatic control on the TMD channel owing to the screening effect, leading to the degradations in both the on-state current density and on/off ratio. Woo Jong Yu and coworkers (Phan et al., 2019) reported that the SWCNT network can be used as the bottom electrode instead of graphene (Figure 6E), which enables effective transport of the gate field through the empty space of the network, thus providing direct modulations on the band alignment at the channel/CNT interface (Figure 6F). As a result, more than 10-fold increase in the on/off ratio can be achieved in the CNT-based vertical FET compared to the devices with graphene contact.

Multi-bridge channel

In the trend of continuous development of the technological node, conventional three-terminal transistors in planar configuration encounter severe problems in further improving the device performance owing to the restricted gate controlling capability, which arises from the quantum confinement effect. Multi-bridge channel field-effect-transistor (MBCFET), formed by vertically stacking the conductive channels in a gate-all-around (Pizzocchero et al., 2016) configuration, has been identified as a very promising candidate to achieve ultimate transistor scaling owing to its outstanding electrostatic controllability and power/area efficiency (Tang et al., 2020).

MBC structures based on 2D semiconductors have been experimentally realized, demonstrating robust device performance. Peng Zhou's group reported for the first time a 2-level-stacked MoS₂ ultrathin MBCFET with a channel thickness of 1.2nm/0.6nm, in which h-BN and graphene were utilized as the dielectric layer and electrodes to construct the GAA geometry (Huang et al., 2020b). The high-resolution TEM image and the corresponding EDS mapping illustrate the clean interface of the heterostructures without any contamination, which is important to ensure the high-efficient carrier transport and good gate controllability of the device. This ultrathin MBCFET exhibits a high drive current of 13.2 μA μm⁻¹ at V_{ds} = 1V, and a minimum SS of 60 mV·dec⁻¹ at room temperature. Notably, the leakage current of the device is as low as 0.92 pA μm⁻¹, which is only 6.5% of that in the Si MBCFET, illustrating its superiority in the aspect of low-power-consumption electronics compared to the Si-based devices (Barraud et al., 2020). The same group further investigated the MoS₂ MBCFET fabricated through vdW assembly (Figures 7A and 7B), where excellent current-controlling ability and high on/off ratio of 4×10⁸ are observed (Huang et al., 2021a). More intriguingly, the normalized drive current in each level channel of the device is 23.11 μA μm⁻¹, exceeding that of the latest seven-level-stacked Si MBCFET, while the leakage current is only 0.4% of this value (Barraud et al., 2020), further suggesting its great potential in the applications of high-performance and low-power-consumption electronics (Figure 7C).

To improve the scalability of 2D MBCFET and facilitate its functionalities in heterogeneous circuitry, large-scale TMD monolayers synthesized by the CVD technique have been utilized in the GAA structure instead of the mechanically exfoliated flakes. Yanqing Wu's group (Xiong et al., 2021) demonstrated a short-channel

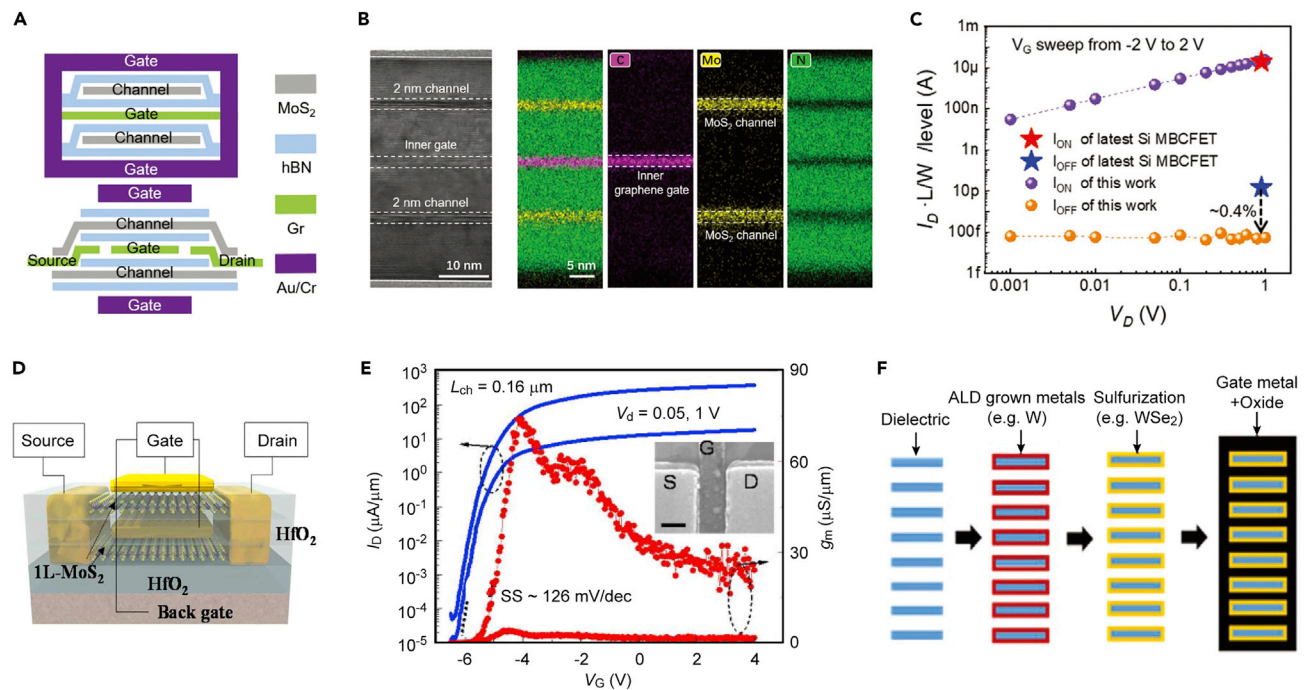


Figure 7. 2D MBCFETs

(A) Schematic structure of MBCFET with two-level-stacked channels.

(B) High-resolution TEM and EDS mapping of the MBC FET.

(C) On-state and off-state current of 2D ultrathin MBCFET dependent on the V_D voltage bias. Figures A, B, and C are reproduced with permission from (Huang et al., 2021a) Copyright© 2021 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

(D) Structure schematic of the 2-stacked MoS₂ nanosheets device. The ALD-grown HfO₂ is used as the dielectric layer in the device.

(E) Transfer characteristics of the short channel MoS₂ MBC FET with L_{ch} of 160 nm. Inset shows the corresponding SEM image displaying the L_g and L_{ch} . Figures D and E are reproduced with permission from (Xiong et al., 2021) Copyright© 2021, IEEE.

(F) One-step 2D-channel formation on suspended bridges. Reproduced with permission from (Liu et al., 2021a) Copyright© 2021 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

MoS₂ MBCFET consisting of two CVD grown monolayers as conductive channels, which are stacked by sequentially layer-by-layer fabrication process (Figure 7D). The ultimate scales of the channel and gate lengths in the resultant devices are approximately 160 and 100 nm, respectively. The device exhibits robust electrical transport performance including low SS of 126 mV·dec⁻¹, high on/off ratio of ~10⁷, and large on-state current density of 420 μA μm⁻¹ at $V_{ds} = 1$ V (Figure 7E). Moreover, it is worth mentioning that this work provides the first demonstration of vertically stacked 2D complementary FETs which exhibits excellent logic inverter function with a moderate gain around 10V/V at $V_{in} = 1.5$ V. It is noted that the MBCFET configuration could promise 50% footprint reduction compared to the planar transistor structure for logic devices. In addition to the complementary logic devices, the advantages of implementing 2D MBCFETs in static random-access memory (SRAM) have also been investigated (Liu et al., 2021a). The simulation results show that the read access time and write time of 2D SRAM in MBCFET configuration can be largely reduced by 41 and 38%, respectively, in comparison to the corresponding Si nanosheet FETs (NSFETs).

These conceptually demonstrated 2D MBCFETs, albeit promising candidates with superior electrostatic controllability for applications in low-power-consumption electronics are still a fair way off from being integrated in large-scale functional circuits, owing to the complicated device structure and the difficulties in process integration. Although Zhou et al. experimentally displayed the 2D MBCFET as a proof-of-concept, the mechanical exfoliation of 2D flakes followed by the layer-by-layer stacking process is time-consuming and cost-ineffective. Additionally, CVD-grown 2D semiconductors on large scale have been utilized by Wu et al. to fabricate the MBCFETs in arrays, the tradeoff between the synthetic temperature of the 2D materials at upper tiers and the critical temperature of defect formation at lower tiers should be taken in consideration. On the other hand, Intel proposed a one-step 2D channel formation method, which exhibits great potential for large-scale and low-cost manufacturing (Chau, 2019). The method begins with the

construction of multiple suspended bridges, followed by the ALD deposition of transition metal and post-chalcogenization process, enabling the production of 2D channels on all of the insulating bridges at once (Figure 7F). Similarly, the thermal budget of synthesizing the 2D materials should be carefully examined. Moreover, transition metal deposition combined with post-chalcogenization generally produces 2D films with small grain size and poor quality, which should be further optimized for high-performance device applications.

GATE LENGTH SCALING OF TRANSISTORS

With reference to the fundamental structure of a 2D transistor, scaling the effective gate length is identified as another feasible approach to achieve ultra-scaled devices in addition to engineering the channel length (Liu et al., 2012; Liu et al., 2018a). In the following, we discuss recent advances in gate length scaling techniques, which are organized as three parallel sections based on the ultimate device structures. The relevant key parameters achieved by the resultant devices are summarized accordingly.

Transistors with one-dimensional gate

As Si-based bulk structures rapidly approaching their physical limits for the effective modulation of the conductive channel, the global-gated device configurations encounter difficulties in the aspect of continuous down-scale of 2D transistors (Chhowalla et al., 2016). Recently, highly conductive 1D structures such as metallic CNTs have attracted tremendous attention owing to their typical geometrical properties, which could be implemented as local gate electrodes with nanoscale effective length to realize ultra-scaled 2D transistors (Liu et al., 2016b).

For instance, Ali Javey's group (Nourbakhsh et al., 2016) reported the fabrication of SWCNT gated MoS₂ transistors using ZrO₂ as dielectric, which successfully realizes an extremely short physical gate length of 1 nm (Figure 8A). Figure 8B shows the electrical transport properties of the device under different bias voltages with ultra-low leakage floor, indicating the ability of the ~1 nm SWCNT gate to completely deplete the MoS₂ channel and thus turn off the device. The authors observed excellent room temperature switching characteristics including near-ideal SS of 65 mV·dec⁻¹ and high on/off ratio of ~10⁶ (Figure 8B). The SS of the device can be further improved by simultaneously applying the CNT local gate and Si global gate, which leads to the complementary reduction in the series/contact resistance. The detailed simulation based on Sentaurus TCAD was also performed to further understand the electrostatics of the nanotube-gated 2D transistor (Figure 8C). The contour plots in the Off and On states clearly illustrate the low and high electric field in the MoS₂ near the SWCNT, indicating the depleted and strong inversion channel. The effective channel length (L_{EFF}) is defined to reveal the region of channel controlled by the SWCNT gate, which is nearly 3.9 and 1.0 nm for the Off and On states, respectively.

It is worth mentioning that the realization of the short-gate transistors relies on the natural geometry of CNTs, which could circumvent any high-precision patterning process and therefore significantly lower the requirements on the lithography techniques (Chen et al., 2006). More importantly, the gate length defined by the diameter of CNTs is in general smaller than 5 nm, which readily crosses the theoretically inaccessible regime for traditional Si transistors, paving the way to realize electronic devices approaching the extreme scales (Quhe et al., 2021).

In addition to the CNTs, nanowires are also identified as potential building blocks for ultra-scaled local gates in 2D transistors (Colinge et al., 2010). For example, Kaustav Banerjee's group (Cao et al., 2016) reported that the ultrathin metallic Co₂Si nanowire can be integrated into the fabrication process of MoS₂ FETs, which simultaneously serves as the source-drain deposition mask and the gate electrode (Figure 8D). In this case, the physical gate length of the transistor is defined by the diameter of the nanowire, which gives rise to an effective channel length in a range of 10-30 nm depending on the morphology of the contacting point between the MoS₂ and Co₂Si nanowire. Significant current on/off ratio over 10⁶ is achieved in the transistor with a considerably low off-state current of ~10 pA μm⁻¹. It is worth noting that the channel length is highly possible to be scaled down to 6 nm using nanowire-shaped gate with a radius of 8 nm (Figure 8E), further validating the promising scalability of thin nanowire-based 2D transistors.

Besides the 1D/2D hybridized device structures discussed above, the atomically thin nature of 2D materials offers another opportunity for the reduction of gate length through reconfiguring the device geometry into an edge-to-face alignment. Tian-ling Ren's group (Ren et al., 2020) proposed a side-wall monolayer MoS₂

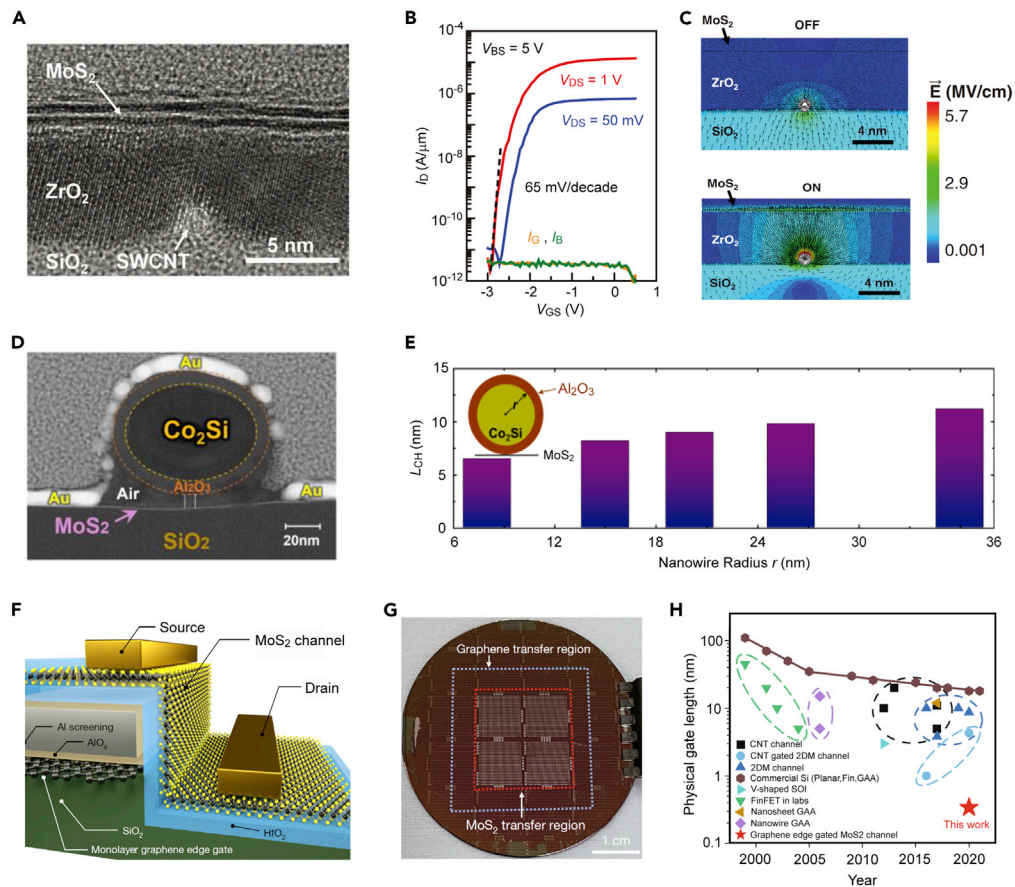


Figure 8. Gate length scaling through integrating one-dimensional CNT/nanowire

(A) Cross-sectional TEM image of the bilayer MoS₂ transistor with 1-nm gate length, where SWCNT and ZrO₂ are used as the gate electrode and dielectric layer, respectively.

(B) Transfer characteristics and the corresponding leakage current of the SWCNT gated MoS₂ transistor at V_{DS} = 50 mV and 1 V.

(C) Electric field contour plots for a simulated bilayer MoS₂ device in the Off and On states. Figures A, B, and C are reproduced with permission from (Desai et al., 2016) Copyright© 2016, American Association for the Advancement of Science.

(D) Cross-sectional TEM image of monolayer MoS₂ FET gated by 1D metallic Co₂Si nanowire.

(E) The relationship between channel length L_{ch} and Co₂Si nanowire radius r for MoS₂ transistors in ultra-scaled gate length. Inset shows a simplified circular-shaped Co₂Si nanowire. Figures D and E are reproduced with permission from (Cao et al., 2016) Copyright© 2016, IEEE.

(F) Schematic of monolayer MoS₂ in side-wall gate configuration by using monolayer graphene edge gate with a thickness of 0.34 nm.

(G) Optical image of the 0.34 nm L_g side-wall transistor arrays on a 2-inch wafer.

(H) The timescale evolution of gate length in ultra-scaled 2D transistors. Figures F, G, and H are reproduced with permission from (Ren et al., 2020) Copyright© 2020, Springer Nature.

transistor employing the edge of monolayer graphene as the gate electrode (Figure 8F). The 0.34 nm physical gate length of the device is defined by the single-atom thickness of monolayer graphene, which represents the ultimately accessible gate scale in a 2D transistor under state-of-the-art nanoscale technologies (Figure 8H). Moreover, this work provides a wafer-scale fabrication strategy to achieve side-wall transistor arrays with a minimum in-batch variation of device parameters e.g. on/off ratio and SS (Figure 8G), which facilitates the development of ultra-scaled transistors toward multi-functional electronic circuits and reveals their enormous potential to further extent the Moore's Law (Jia et al., 2022).

Fin-type structured field-effect-transistor

The gate coupling efficiency plays a vital role in determining the electrical switching properties in a transistor, particularly in the extreme scale. However, when the scale approaches sub-10 nm, the gate-channel

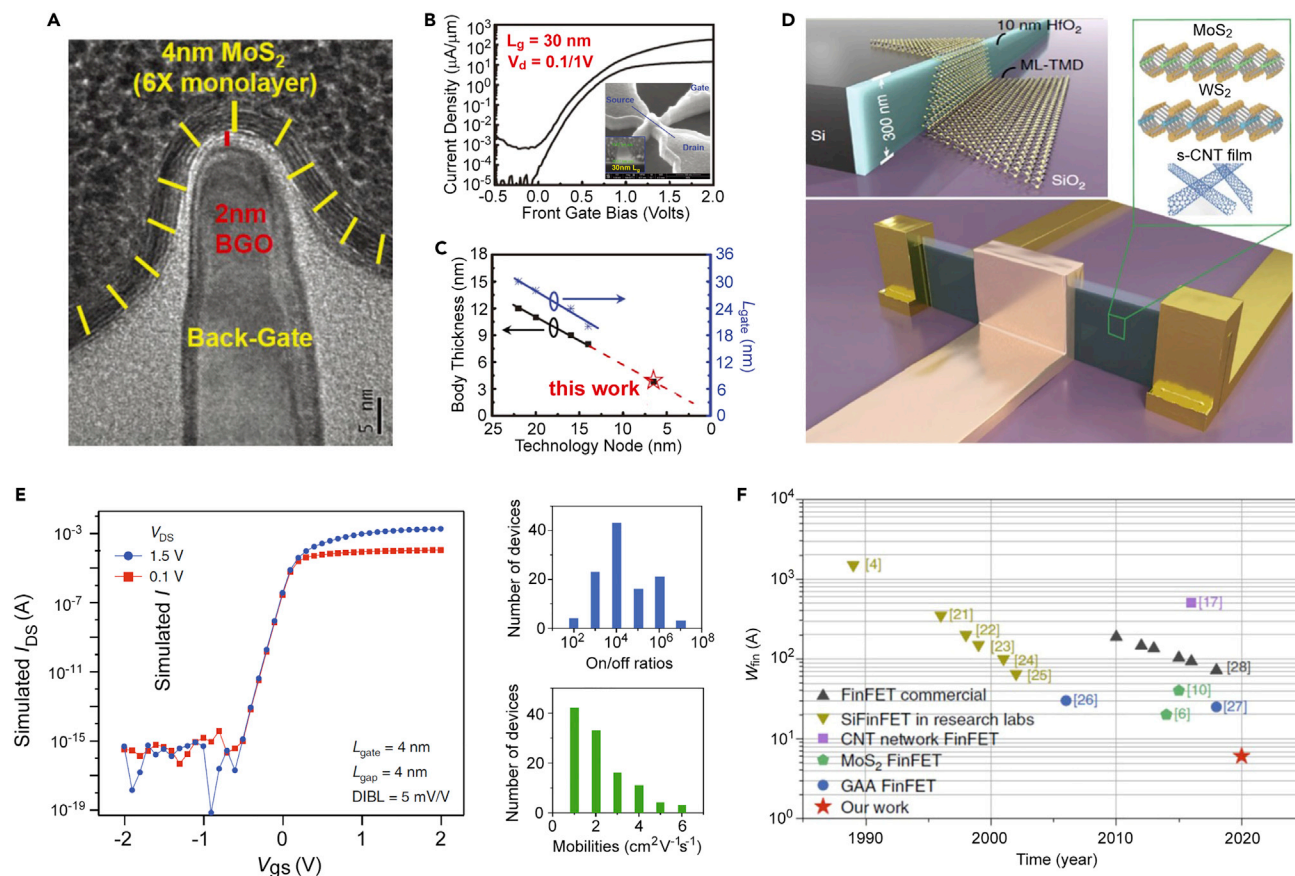


Figure 9. 2D FinFETs

(A) Cross sectional TEM image of MoS₂ FinFET using Si back gate.

(B) Transfer characteristics of the MoS₂ FinFET with 4 nm thin body sweeping by the front gate voltage. Inset shows the SEM image of the device for measurement.

(C) The development trends of the FinFET channel thickness and gate length. Figures A, B, and C are reproduced with permission from (Chen et al., 2015) Copyright© 2015, IEEE.

(D) Left: The simulated field effect curves of 4 nm gate length FinFET. Right: Statistics of on/off ratio and mobility of MoS₂ ML-FinFET.

(E) Schematic illustration of the 2D FinFET with W_{fin} of 0.6 nm. The monolayer MoS₂ crystal is grown over a 300 nm height Si step with the side wall coated by HfO₂ dielectric.

(F) A timescale evolution of W_{fin} for the transistors in FinFET configuration. Figures D, E, and F are reproduced with permission from (Chen et al., 2020) Copyright© 2020, Springer Nature.

contacting area in the conventional planar device is severely restricted, which causes degradations in the gate controlling efficiency with a large leakage floor, leading to a dramatic increase in heat dissipation. To enhance the gating efficiency while maintaining a small footprint of transistors, efforts have been devoted to developing new device architectures extending in the out-of-plane direction, following which a novel FinFET has been introduced (Jurczak et al., 2009).

Initially, Chenming Hu's group (Chen et al., 2015) fabricated a 6-layer MoS₂ FinFET (fin width $W_{fin} = 4$ nm) based on a back gate Si fin structure with 2 nm-thick gate oxide, followed by the deposition of a 30 nm long front gate (Figure 9A). The hydrogen plasma treatment was further employed to achieve a molybdenum-rich surface to lower the sheet resistance of the MoS₂ channel. As shown in Figure 9B, the transfer characteristics of the MoS₂ FinFET demonstrate a current on/off ratio over 10^5 and I_{on} of $\sim 200 \mu\text{A } \mu\text{m}^{-1}$ at 1 V operation bias, illustrating the great potential of the fin-structure-based TMD transistors in ultra-scaled technological node (Figure 9C). Similarly, Huaxiang Yin's group (Pan et al., 2019) reported a Si fin structure gated monolayer MoS₂ transistor on the scale of 10 nm. The device exhibits excellent switching behavior with average drain current on/off ratio exceeding $\sim 10^6$, indicating high-efficient modulation of the MoS₂ channel through the Si fin back gate.

More recently, by adopting a bottom-up fabrication route, Zheng Han's group (Chen et al., 2020) demonstrated a vertically aligned monolayer MoS₂ FinFET (ML-FinFET) with W_{fin} of ~ 0.6 nm, which is realized by adapting a template-growth method (Figure 9D). Firstly, a 300 nm step edge is etched from a planar Si on the insulator wafer, followed by the coating of 10 nm HfO₂ achieved via ALD and anisotropic dry etching. After that, monolayer MoS₂ crystal is conformably grown on the step edge with the deposition of source-drain electrodes. The planar portion of the as-grown MoS₂ is then etched via the plane-removing process. Finally, wet etching is performed to remove the silicon step followed by the metallization of the gate electrode, achieving the MoS₂ FinFET with sub-1 nm W_{fin} . The current on/off ratio of the monolayer FinFET approaches $\sim 10^7$, suggesting the robustness of the device (Figure 9E). This work pushes the W_{fin} of the FETs to an atomic physical limit, an order of magnitude thinner than that of state-of-the-art FinFETs, breaking the limitation of lithography precision on the W_{fin} , which is beneficial for lower power consumption and higher integration of next-generation nanoelectronics (Figure 9F).

Apparently, the fin-shaped structure effectively enlarges the area of gate-channel interface without compromising the miniaturization of the device footprint, which significantly strengthens the gate controllability, thereby alleviating the short channel effect occurring in the planar device with comparable scales. Moreover, the manufacturing process of 2D FinFETs is compatible with the mainstream silicon technology, paving a way to further extend the gate scaling in the post-Moore era (Trombini et al., 2019; Vashishtha and Clark, 2021).

Self-aligned engineering of transistors

Self-alignment technology has been proposed as an effective way to precisely position the gate electrode at extreme scales, while eliminating various unfavorable factors introduced from the lithography-related procedures, including residue absorption, interfacial traps, and parasitic capacitance/resistance.

As shown in the high-resolution TEM image in Figure 10A, Eric Pop et al. reported for the first time a monolayer MoS₂-based self-aligned top-gate FETs (SATFETs), in which the Al₂O₃ gate dielectric scaling down to 10 nm is formed by self-passivated surface oxidation of the thermally deposited Al nano-block (English et al., 2016). The technique achieves a core-shell structure, which serves both as an anchor for the gate electrode and a hardmask for the deposition of source-drain contacts. The device exhibits high saturation current I_{Dsat} exceeding $400 \mu\text{A} \mu\text{m}^{-1}$, and low SS down to $80 \text{ mV} \cdot \text{dec}^{-1}$ with a gate length of 30 nm and EOT of 2.5 nm, suggesting the potential of 2D SATFETs in achieving high-performance ultra-scaled electronics. It is noted that the ballistic transport in 2D transistors might emerge at a scale below 100 nm, which is firstly investigated in this work. The ballistic transmission efficiency (T_r) of the MoS₂ SATFETs is around 0.15 at $T = 300\text{-}400$ K in the saturation regime (Figure 10B), which gradually increases to 0.25 with an effective electron velocity (v_{EFF}) of $9 \times 10^5 \text{ cm s}^{-1}$ at $T = 80$ K, arising from the suppression of the phonon scattering at low temperatures (Figure 10C). Nevertheless, the T_r and v_{EFF} in the saturation regime are still far smaller than state-of-the-art silicon transistors in the similar scales. To further improve the T_r and v_{EFF} in the ultra-scaled 2D transistors, it is essential to reduce the effective channel length (L_{EFF}) and enhance the carrier mobility. The L_{EFF} is determined by the profile of the top of barrier (ToB), which becomes sharper and thus results in lower L_{EFF} by contact doping and improved EOT. On the other hand, the mobility in 2D transistors is strongly related to the carrier scattering, which can be boosted by reducing the densities of disorders, impurity charges, and phonons in the channel, as well as improving the dielectric interface.

On the basis of the above-mentioned fabrication strategy, Xinran Wang et al. (Li et al., 2021) reported a significant improvement in the performance of SATFETs with a gate length of 60 nm by using semimetal Bicontacts (Figure 10D). Arising from the immunity against the FLP effect, the device exhibits zero Schottky barrier height and ultra-low R_c of $280 \Omega \cdot \mu\text{m}$ which is nearly one order of magnitude smaller than that of the MoS₂ transistors using traditional metal contacts such as Ag, Cr, and Au (Figure 10E). The optimized metal contacts contribute to the outstanding electrical transport performance of the SATFETs with a high I_{ON} of $680 \mu\text{A} \mu\text{m}^{-1}$, high current on/off ratio over 10^6 , and a good SS of $120 \text{ mV} \cdot \text{dec}^{-1}$, which are much more superior than those of the CVD MoS₂ transistors in top-gate configuration (Figure 10F). The SATFET arrays also exhibit excellent SCEs immunity and negligible DIBL effect, which are of great importance in the application of high-density integrated circuits. The combination of high-performance top-gate 2D FETs with large-area CVD MoS₂ will significantly promote the development of 2D integrated circuits and heterogeneous systems.

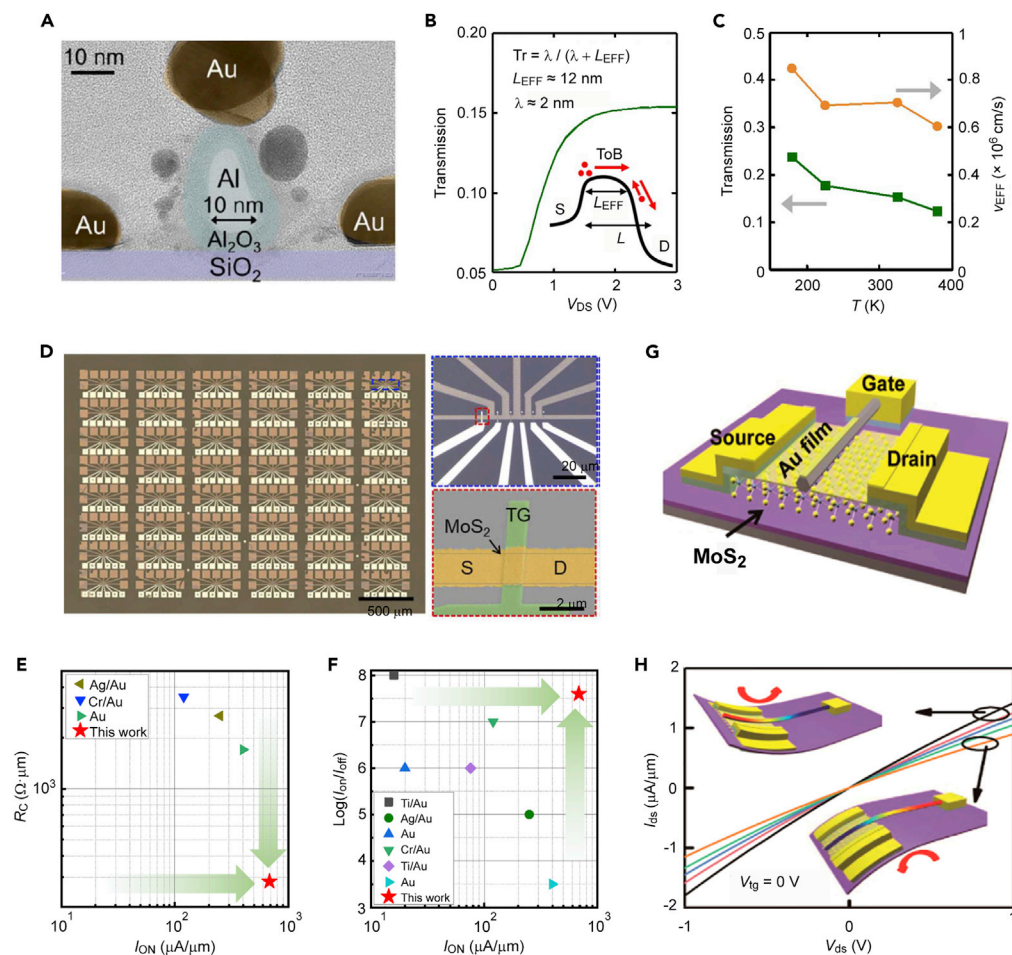


Figure 10. 2D transistors achieved via self-aligned engineering technique

(A) Cross-sectional TEM image of the 2D MoS₂ SATFET with L_g of 10 nm in false color.
 (B) Transmission (*Tr*) vs V_{DS} for the 2D SATFET under gate length of 10 nm at a temperature of 225 K. Inset shows conduction band diagram for the carrier transport cross the barrier.
 (C) *Tr* and effective velocity (*v*_{EFF}) as a function of temperature. Figures A, B, and C are reproduced with permission from (English et al., 2016) Copyright© 2016, IEEE.
 (D) Optical images of the Bicontacted MoS₂ SATFETs in arrays over 6 mm². The corresponding false-colored SEM image of a single top-gated SATFET is also demonstrated at the bottom right.
 (E) Benchmark of *R*_C versus *I*_{ON} of the top-gated monolayer CVD MoS₂ FETs.
 (F) Benchmark of on/off ratio versus *I*_{ON}. Figures D, E, and F are reproduced with permission from (Li et al., 2021) Copyright© 2021, IEEE. (G) Schematic of the self-aligned GaN nanowire top-gated MoS₂ FETs.
 (H) Output characteristics of the self-aligned MoS₂ transistor under different strains without applying gate voltage. Inset shows the schematics of the effects of strain on the transistor. Gradient ramp indicates the piezo-potential in GaN NW; red and blue indicate positive and negative piezo-potential, respectively. Figures G, H are reproduced with permission from (Liu et al., 2016a) Copyright© 2016, American Chemical Society.

In addition to the oxide-based SATFETs, semiconducting nanowires could offer an additional degree of freedom in designing new functional devices through band gap alignment to the TMD channel materials (Lin et al., 2001). Zhonglin Wang et al. (Liu et al., 2016a) reported high-performance self-aligned MoS₂ FETs using p-type semiconducting GaN nanowires as local gates (Figure 10G). The fabrication process ensures the preservation of the intrinsic properties of MoS₂ while suppressing the interfacial scattering rate, leading to excellent electrical transport characteristics such as high on/off ratio of ~10⁷ and small SS of 64 mV/dec. The photodetection properties of the device are also investigated, in which high photoresponsivity of 443.3 A·W⁻¹ and fast response time of 5 ms are observed. The performance can be further improved with much higher photoresponsivity of 734.5 A·W⁻¹ by applying strain on the device owing to the unique piezoelectric property of the GaN nanowire (Figure 10H).

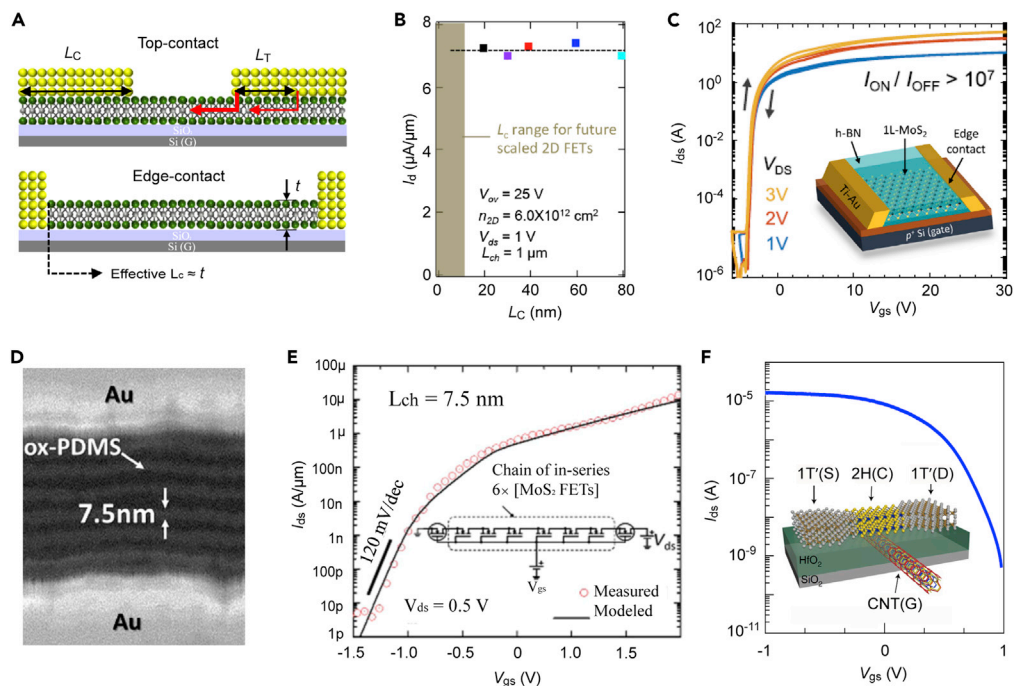


Figure 11. Contact scaling based on edge contact technique

(A) Schematic of 2D FET with traditional top contacts and edge contacts.

(B) Relationship between I_d and L_c for *in-situ* edge contacts after aligning V_{th} , showing potential for sustaining performance while scaling contact length. Reproduced with permission from (Cheng et al., 2019) Copyright© 2019, American Chemical Society.

(C) The transfer curve of the monolayer MoS₂ transistor with edge contacts. Inset shows the corresponding schematic of the device for measurement. Reproduced with permission from (Jain et al., 2019) Copyright© 2019, American Chemical Society.

(D) SEM image of the hetero-phase MoS₂ transistor with $L_{ch} = 7.5$ nm.

(E) MIT Virtual Source Compact modeling (MVS) of the transfer curve of the hetero-phase MoS₂ short channel transistor. Inset shows circuit configuration consisting of a chain of six MoS₂ FETs used in the MVS model. Figures D and E are reproduced with permission from (Nourbakhsh et al., 2016) Copyright© 2016, American Chemical Society.

(F) Transfer curve of CNT-gated p-type MoTe₂ FET in 1T'-2H hetero-phase configuration. Inset shows the corresponding schematic of the device for measurement. Reproduced with permission from (Zhang et al., 2019a) Copyright© 2019, Springer Nature.

CONTACT SCALING OF TRANSISTORS

Besides the scaling of channel and gate lengths, contact scaling is another important aspect of device miniaturization. However, as the contact length (L_C) is scaled closing to the carrier transfer length (L_T) in a conduction channel, the area available for carrier injection is reduced, which dramatically increases the contact resistance owing to the current crowding (Allain et al., 2015; Cheng et al., 2019). In particular, the current crowding is more pronounced with the $L_C \leq L_T$ in the range of tens or hundreds nanometers, leading to the limitations on the contact scaling process (Cheng et al., 2019). Notably, edge contact geometries have been identified as a viable route toward the ultimate scale of electrical contacts, as the edge is independent of the physical contact length, especially for 2D channels with edges at the atomic scale (Figure 11A) (Lee et al., 2022; Wang et al., 2013). Additionally, the carrier transport at the metal-2D materials interface is dominated by the covalent bonding in edge-contact, which is distinct from the vdW gap existed in the top-contacted devices. This is essential to eliminate the metal-induced gap states that are responsible for the uncontrollable Schottky barrier and Fermi-level pinning effect in 2D transistors, which could substantially improve the field-effect mobility (Kim et al., 2017; Liu et al., 2022). Recently, Won Jong Yoo's group comprehensively reviewed the 1D edge contacts for 2D material-based devices, in which state-of-the-art techniques for achieving the edge contacts, together with the charge transport and device applications of edge contacts are elaborately discussed (Choi et al., 2022). Here, we focus on the contact scaling in 2D transistors by using the edge-contact techniques.

Aaron D. Franklin's group reports the edge contact scaling in both mono- and multilayer MoS₂ by using various metal-channel interfaces. The clean edge contacts of metal-MoS₂ can provide immunity to the contact-scaling limitation, in which the electrical transport performance is independent of the contact length down to the 20 nm regime (Figure 11B) (Cheng et al., 2019). The *in-situ* Ar⁺ sputtering has been identified as a crucial step for producing an optimum metal-MoS₂ contact, enabling the efficient charge transfer for realizing low R_c with a high density of current injection at the atomic site (Shen et al., 2021). This leads to an order of magnitude enhancement of electrical transport performance compared to the *ex situ* metal edge contacts. Similarly, Lukas Novotny's group reports viable edge contact formation to h-BN encapsulated monolayer MoS₂ in a polymer-free manner, by combining the techniques of reactive ion etching, *in-situ* Ar⁺ sputtering at a slightly tilted angle, and annealing (Jain et al., 2019). The transistor exhibits comparable electrical transport performance to the top-contact counterparts, in which a relatively high mobility up to ~30 cm² V⁻¹ s⁻¹, high on-current density >50 μA μm⁻¹, and low SS of ~116 mV·dec⁻¹ are achieved (Figure 11C). The top-down approach via plasma etching and metallization is very promising to achieve the edge contact, whereas it yields limited success in 2D transistors owing to its stringent demands on the facilities such as an *in-situ* ion sputtering and metal deposition system. Alternatively, Lee Ji Ung's group employed the 1D edge-contacted graphene as electrodes instead of metals in the h-BN-encapsulated WSe₂ transistor via dry transfer technique, in which a tunable Schottky barrier with controllable ideality factor is realized (LaGasse et al., 2019).

On the other hand, 2D materials generally possess polymorphic lattice structures including the semiconducting 2H phase and the metallic 1T/1T' phase, where the local phase transition can be realized through phase engineering techniques including catalytic synthesis, chemical treatment, and laser irradiation (Chen et al., 2020; Voiry et al., 2015). Taking advantage of this unique characteristic, 2D transistors with covalently bonded edge-contacts have been achieved through the construction of in-plane 2H-1T/1T' hetero-phase junctions (Kappera et al., 2014). For example, Amirhasan Nourbakhsh and coworkers demonstrate a chain of alternatively connected 2H-1T' MoS₂ structures, where the deterministic phase transition is achieved by using the mask of self-assembled block copolymers followed by the n-butyllithium solution treatment (Nourbakhsh et al., 2016). The exposed MoS₂ is transformed to the metallic 1T' phase which automatically forms the seamless contacts to the semiconducting 2H phase, giving rise to a series of short-channel transistors with 7.5 nm half-pitch (Figure 11D). As shown in Figure 11E, the transistor chain exhibits an excellent on/off ratio over ~10⁷ with a low off-state current of 10 pA μm⁻¹ and SS of ~120 mV·dec⁻¹. Moreover, the access resistance at the seamless 2H-1T' interface is determined to be 75 Ω μm, indicating nearly ideal Ohmic contacts in the transistor chain, which demonstrates great potential to achieve efficient charge injection and ultra-low power dissipation. It is noted that the chemical treatment in the liquid phase could introduce hydrogen absorption on the MoS₂ surface, which is favorable for the structural stabilization of the 1T' phase as well as the high-quality 2H-1T' interfaces.

In addition to the top-down strategy discussed above, the lateral heterophase junctions can be formed through bottom-up techniques by tuning the synthetic temperatures and pre-patterning precursors. Jiao liying's group demonstrates a large-scale phase-contact strategy to obtain 1T'-2H MoTe₂ homo-junction by tellurizing MoO₃ and MoO_{2.0-2.5} (Zhang et al., 2019a). Additionally, the heterophase MoTe₂ transistors in 4 nm gate length are achieved through integrating the CNT gate electrode and HfO₂ dielectric layer. The ultra-scaled transistor exhibits robust performance including a high current on/off ratio of ~10⁵ and a low SS down to ~73 mV·dec⁻¹ (Figure 11F). The Schottky barrier height of such 1D edge contact is also dramatically reduced to be ~20 meV, together with a robust mobility of ~50 cm² V⁻¹ · s⁻¹. The heterophase edge contact strategy can also be extended to other 2D materials, such as the NbSe₂/W_xNb_{1-x}Se₂, MoS₂/Mo₂C, and PtSe₂/PtTe₂ heterostructures synthesized by the *in-situ* selenization in large area arrays (Choi et al., 2019; Kim et al., 2022; Vu et al., 2021). Overall, the bottom-up growth of the lateral heterophase structure demonstrates great potential to achieve edge-contacted 2D transistors on the wafer scale.

CONCLUSION AND OUTLOOK

In conclusion, TMDs have been of central importance in the next-generation electronics with full functionality, owing to the primary merit of their atomically thin nature that allows ultra-scaled transistor architectures to approach the sub 10 nm regime. So far, researchers have made exciting progress in performance enhancement and size scaling of the 2D TMDs-based ultra-scaled transistors. The evolution of the channel and gate lengths with respect to the fabrication techniques and device geometries are summarized, together with the corresponding satisfactory performance parameters (Table 1). In the perspective of

Table 1. Performance summary of the 2D short-channel transistors

| | L_{ch}/L_g (nm) | t_c (nm) | μ ($\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$) | R_C ($\text{k}\Omega \cdot \mu\text{m}$) | V_{DS} (V) | I_{on} $\mu\text{A}/\mu\text{m}$ | I_{off} $\text{pA}/\mu\text{m}$ | V_{th} V | DIBL (V/V) | SS (mV/dec) | $I_{on/off}$ |
|--|----------------------|---------------|--|---|-----------------|---------------------------------------|--------------------------------------|---------------|---------------|----------------|--------------|
| Bi Contact (Shen et al., 2021) | 35 | ML | 55 | 0.123 | 1 | ~900 | ~5 | ~-50 | / | / | 10^8 |
| PTCDA/HfO ₂ Gate (Li et al., 2019) | 20 | ML | 34 | / | 0 | ~50 | ~6 | ~-1.8 | / | 60 | 10^7 |
| Two-step EBL (Zhu et al., 2018) | 14 | ML | 21.4 | 2.3 | 1.6 | 240 | ~1 | ~-0.5 | / | 64 | 10^7 |
| SWCNT Masks (Xiao et al., 2019) | 7.5 | ML | 17.4 | 10.4 | 1 | 45 | ~8 | ~-0.7 | 0.14 | 120 | 10^7 |
| β -Bi ₂ O ₃ Nanogaps (Xu et al., 2017) | 8.2 | ML | 1.1 | / | 1 | 2.5 | 3 | ~-1.2 | / | 140 | 10^6 |
| Graphene Contact (Xie et al., 2017) | 4 | ML | 30 | 3.8 | 0.1 | ~9 | 0.3 | ~-1.0 | 0.425 | 93 | 10^7 |
| MBCFET (Xiong et al., 2021) | 100 | ML | / | 0.77 | 1 | 420 | ~40 | ~-1.5 | 0.25 | 126 | 10^7 |
| VFET with Al ₂ O ₃ /h-BN spacer (Jiang et al., 2020) | 12.6 | ML | / | 1.2–1.5 | 0.5 | 70 | ~0.1 | ~-0.26 | / | / | 10^9 |
| Graphene/MoS ₂ VFET (Farooq Khan et al., 2017) | 38 | 38nm | / | / | -0.5 | ~500 | ~500 | ~-25 | / | / | 10^6 |
| SWCNT/MoS ₂ VFET (Phan et al., 2019) | 0.65 | ML | 21 | / | -2 | ~30 | ~10 ⁴ | / | / | / | 10^3 |
| vdW Contact (Liu et al., 2021b) | 0.65 | 30nm | 3,81 | / | ~0 | ~40 | ~10 ⁴ | ~-40 | / | / | 10^3 |
| Phase transition (Nourbakhsh et al., 2016) | 7.5 | 3ML | 25 | 0.075 | 1.0 | 230 | ~10 | ~-0.7 | 0.1 | 120 | 10^7 |
| SWCNT/ZrO ₂ gate (Desai et al., 2016) | ~1 | 2ML | / | / | 1 | ~7 | ~10 | ~-2 | 0.2 | 65 | 10^6 |
| CNT gate (Zhang et al., 2019a) | ~4 | / | / | / | / | / | / | / | / | 73 | 10^5 |
| Co ₂ Si/Al ₂ O ₃ gate (Cao et al., 2016) | 6 | ML | / | / | 1 | ~20 | 10 | ~-0.6 | / | 180 | 10^6 |
| Graphene/Al ₂ O ₃ side-wall gate (Ren et al., 2020) | 0.34 | ML | / | / | -2 | ~0.2 | ~1 | ~-2 | 1 | 210 | 10^5 |
| 6ML MoS ₂ Si-FinFET (Chen et al., 2015) | 4 | 6ML | / | / | 1 | ~200 | ~10 ³ | ~-0.6 | / | 143 | 10^5 |
| 1ML MoS ₂ Si-FinFET (Pan et al., 2019) | 10 | ML | / | / | 0.9 | ~1.2 | ~1 | -7 | 1 | 360 | 10^6 |
| Vertically Aligned FinFET (Chen et al., 2020) | ~0.6 | ML | 10 | / | 1.0 | ~5 | ~0.5 | ~-0.7 | 0.005 | 300 | 10^7 |
| Al/Al ₂ O ₃ -SATFET (English et al., 2016) | 10 | ML | 34 | 1.7 | 1 | ~10 | / | / | 0.07 | 80 | / |
| Bi Contact Al ₂ O ₃ -SATFET (Li et al., 2021) | 60 | ML | 35 | 0.28 | 0.1 | ~250 | ~30 | ~-4.0 | / | 114 | 10^7 |
| GaN -SATFET (Liu et al., 2016a) | 200 | ML | 20.7 | / | 1 | ~10 | ~1 | ~-1 | / | 64 | 10^7 |

the device size, currently the physical gate length of sub-1 nm can even be realized by using graphene edge electrodes, indicating the ultimate scale of 2D transistors, which is far more advantageous than that of the conventional Si transistors (Wu et al., 2022). Moreover, the device performance has also been largely optimized owing to the extraordinary intrinsic properties of the 2D semiconductors. For example, 2D semiconductor-based MBCFETs achieve far lower leakage currents than that of the Si MBCFETs originating from their suitable band gap and carrier effective mass, illustrating their great potential in low-power electronics. Additionally, the high carrier mobility at extreme physical gate length arising from the dangling-bond-free surface in 2D materials could enable high carrier velocity and saturation current, which is essential for high-speed digital devices. Atomically thin 2D semiconductors also enable lower interlayer signal delays and more efficient heat dissipation, increasing integration density by more than 150% compared to conventional monolithic 3D integration (Jiang et al., 2019). Basically, it can be concluded that these 2D ultra-scaled transistors provide the possibility for their 3D integration compatible with the Si very large-scale integration (VLSI) technology (Akinwande et al., 2019).

The ultra-scaled 2D transistors, albeit very promising for the applications of heterogeneous integrated circuitry with extended Moore's Law, still encounter challenges in the aspects of uniformity, stability, and reliability for the ultimate transition from concept genesis to industrial maturity. First, the uniform synthesis of high-quality single-crystalline 2D films at the wafer scale is essential for their integration in very-large-scale applications, where the uniformity in film thickness and transport performance are important factors to be considered. 2D thin films grown by conventional CVD methods are generally polycrystalline with high nucleation temperature in the range of 600-900°C, hindering their compatibility with the back-end-of-line temperature in CMOS technology (Choi et al., 2017; Huang et al., 2014; Kang et al., 2015). The

exploration of low-temperature synthesis strategies (<400-500°C) for TMDs becomes increasingly crucial. Under this trend, low-temperature growth of single crystalline MoS₂ and WS₂ have been investigated and partially succeeded at 450°C and 300-450°C, respectively, illustrating the potential of 2D materials in future integrated circuits (Akinwande et al., 2019; Delabie et al., 2015; Jurca et al., 2017).

On the other hand, the topological or topographical defects, such as the grain boundaries, atomic vacancies, and strain fields, introduced during the 2D material preparation processes could ultimately affect the uniformity of the devices (Novoselov et al., 2004; Stoller et al., 2008). Under such circumstances, a physical transfer-process-based vdW integration approach has been demonstrated to alleviate these challenges (Jung et al., 2019; Liu et al., 2019b). The weak vdW force and relatively low processing temperatures ensure slight damage to the 2D crystals during the transfer process. It is noted that a highly controlled vacuum environment could be favorable for achieving ultra-clean interfaces with high uniformity in the large-scale transfer process (Kang et al., 2017a). Besides the uniformity, the stability of environment-sensitive 2D semiconductors (such as BP) must also be taken into consideration (Liu et al., 2021c). An effective method to alleviate material degradation in air is to encapsulate the conductive channels using *in-situ* grown protective layer or diffusion barrier, such as Al₂O₃ and HfO₂, with compact lattice structures and robust air stability (Wood et al., 2014). On the other hand, surface modification is also identified as a viable route to improve material stability through the formation of covalent bonds at the surfaces, which has been confirmed in adatoms doped BP and other 2D materials (Feng et al., 2016).

In addition, the reliability of 2D materials at the device level is also an important aspect of their further industrial application, which is largely determined by the properties of channel-dielectric and channel-electrode interfaces, as well as the qualities of the insulator dielectric and metal electrodes. In particular, the introduction of defects and residues at the channel-dielectric interface can generate a series of reliability issues, such as 1/f noise, random telegraph noise, hysteresis, bias temperature instability, time-dependent dielectric breakdown, and hot carrier degradation (Das et al., 2021). The integration of defect-free crystalline insulator with a 2D channel to form a vdW interface could be an option to improve the reliability (Illarionov et al., 2020), where the dielectric materials including h-BN, Bi₂SeO₅, and CaF₂ are proposed as the most promising candidates. However, new problems such as thermal budget and gating efficiency might emerge by using these novel dielectrics (Li et al., 2020b). Alternatively, introducing a buffer layer could also be an effective way to improve material adhesion for obtaining a high-quality channel-dielectric interface, which has been demonstrated in the preparation of uniform and ultrathin HfO₂ dielectrics on 2D materials using molecular crystals of PTCDA as buffer layers (Li et al., 2019). Besides the dielectric layer, another concern is the channel-electrode interface which significantly influences the device performance. The deposition of energetic metal atoms could induce damage in the ultrathin 2D materials underneath, causing Fermi level pinning effect and inefficient charge injection that are manifested as large contact resistances (Liu et al., 2018b). To solve this issue, the fabrication of vdW contacts has been reported, which provide atomically clean and electronically sharp interfaces with minimized interfacial states and tunable Schottky barrier height (Liu et al., 2021b). This approach is applicable to various device configurations including 2D/3D hybrid stacks; however, its feasibility at the wafer scale still requires further explorations (Jung et al., 2019; Li et al., 2020a; Liu et al., 2018b; Liu et al., 2019b; Zhang et al., 2019b). Additionally, edge-contact or semimetal contact are also promising approaches for realizing low contact resistance and contact scaling in 2D transistors (Yang et al., 2019; Zhang et al., 2019a).

Although challenges remain, 2D materials demonstrate great potential in the realization of lab-to-fab transition. As such, multi-pronged efforts, including wafer-scale synthesis of high-quality and uniform 2D thin films, improving device scalability and reliability, and implementation with silicon technology, need to be devoted to their ultimate applications with a fully standardized 2D industrial chain. We envision that, with the continuous progress of 2D research in both scientific and technological aspects, 2D semiconductor technology would become a global industry business with far-reaching influence.

Limitations of the study

The investigation of 2D transistors and integrated circuits has been lasted for nearly ten years, for the purpose of extending Moore's Law. There have been numerous works in the aspects of 2D materials growth, device fabrication, doping techniques, contact engineering, and circuit integration. It is impossible to cover and cite all the related publications. Our review focuses on the recent advances in achieving

ultra-scaled 2D transistors in the aspects of techniques and mechanisms. We introduce state-of-the-art strategies for realizing ultra-scaled 2D transistors in terms of channel length and gate length scaling, providing comprehensive evaluations of the corresponding device performance together with the possible optimization routes through the technological aspect. Our article illustrates a general direction on the realization of ultimate 2D transistors with extreme scales, which should be of interest in both the scientific and industrial communities.

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AUTHOR CONTRIBUTIONS

Conceptualization: T.L. and D.X.; Investigation: T.W., Z.H, T.L, and D.X.; Writing–Original Draft: T.W., Z.H, D.X., and T.L; Writing–Review & Editing: T.W., Z.H, Q.X, X.Z., D.X., and T.L; Supervision: T.L. and D.X.; Funding Acquisition: T.L. and D.X.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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