

Article

Influence of Different Device Structures on the Degradation for Trench-Gate SiC MOSFETs: Taking Avalanche Stress as an Example

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Abstract: The variations in the degradation of electrical characteristics resulting from different device structures for trench-gate SiC metal-oxide-semiconductor field effect transistors (MOSFETs) are investigated in this work. Two types of the most advanced commercial trench products, which are the asymmetric trench SiC MOSFET and the double-trench SiC MOSFET, are chosen as the targeted devices. The discrepant degradation trends caused by the repetitive avalanche stress are monitored. For the double-trench device, the conduction characteristic improves while the gate-drain capacitance (C_{gd}) increases seriously. It is because positive charges are injected into the bottom gate oxide during the avalanche process, which are driven by the high oxide electronic field (E_{ox}) and the high impact ionization rate (I.I.) there. Meanwhile, for the asymmetric trench SiC MOSFET, the I-V curve under the high gate bias condition and the C_{gd} remain relatively stable, while the trench bottom is well protected by the deep P+ well. However, its threshold voltage (V_{th}) decreases more obviously when compared with that of the double-trench device and the inclined channel suffers from more serious stress than the vertical channel. Positive charges are more easily injected into the inclined channel. The phenomena and the corresponding mechanisms are analyzed and proved by experiments and technology computer-aided design (TCAD) simulations.



Citation: Wei, Z.; Fu, H.; Yan, X.; Li, S.; Zhang, L.; Wei, J.; Liu, S.; Sun, W.; Wu, W.; Bai, S. Influence of Different Device Structures on the Degradation for Trench-Gate SiC MOSFETs: Taking Avalanche Stress as an Example. *Materials* **2022**, *15*, 457. <https://doi.org/10.3390/ma15020457>

Academic Editor: Fabrizio Roccaforte

Received: 21 November 2021

Accepted: 4 January 2022

Published: 8 January 2022

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Keywords: SiC MOSFET; trench gate; different device structure; degradation; avalanche

1. Introduction

With etching, oxidation, and other critical processing technologies becoming more and more mature, SiC metal-oxide-semiconductor field effect transistors (MOSFETs) are gradually applied to power electronic fields to replace traditional silicon power devices [1–4]. Numerous SiC MOSFET products have been pushed into the market [5–7]. Due to the advantages of low-specific ON resistance (R_{onsp}), high power density, fast switching speed, and low switching loss, trench-gate SiC MOSFETs are more promising than planar-gate ones [8–10]. However, for the sidewall and the bottom of a trench gate, which suffer from higher electric fields during practical applications, trench-gate SiC MOSFETs are faced with more serious reliability issues when compared with planar-gate devices [11,12].

Infineon and Rohm have released their trench-gate SiC MOSFET products in recent years, which are state-of-art commercial trench-gate devices [13,14]. The reliability of them under different stresses, such as the surge current stress, the avalanche stress, and the short-circuit stress, has been well studied [15–26]. Most of the existing articles only report the failure or the degradation mechanism of one single trench-gate device [15–22]. Very

few of them investigated the failure of both devices at the same time [23–26]. However, no one reported that the disparate device structures would result in different degradations in the device performances, even if they are both trench-gate SiC MOSFETs.

In this work, the variations in the degradation trends resulting from the structure difference between two types of trench-gate devices, which are the double-trench SiC MOSFET produced by Rohm and the asymmetric trench SiC MOSFET produced by Infineon, are investigated in detail. The avalanche stress, which applies load current (I_{load}) and extremely high breakdown voltage (BV) to a device simultaneously and leads to obvious degradation or even damage, is chosen as the targeted stress. It is found that after enduring repetitive avalanche stress, the static and dynamic characteristics of the two trench-gate devices exhibit different degradation trends. With the help of Silvaco TCAD simulations, the dominant mechanism is found and proved by analyzing the physical characteristics of both the devices under avalanche state.

2. Device Structures and Experiment Conditions

The cross-sectional schematic diagrams of the double-trench SiC MOSFET (SCT3160KL) and the asymmetric trench SiC MOSFET (IMW120R140M1H) studied in this work are shown in Figure 1a,b. Their rated BV is 1200 V, as listed in Table 1. The rated ON-state resistance (R_{on}) and the DC drain current (I_D) of the double-trench SiC MOSFET were 160 m Ω and 18 A, while the R_{on} and the I_D of the asymmetric trench SiC MOSFET were 140 m Ω and 19 A. They share similar conduction and blocking characteristics.

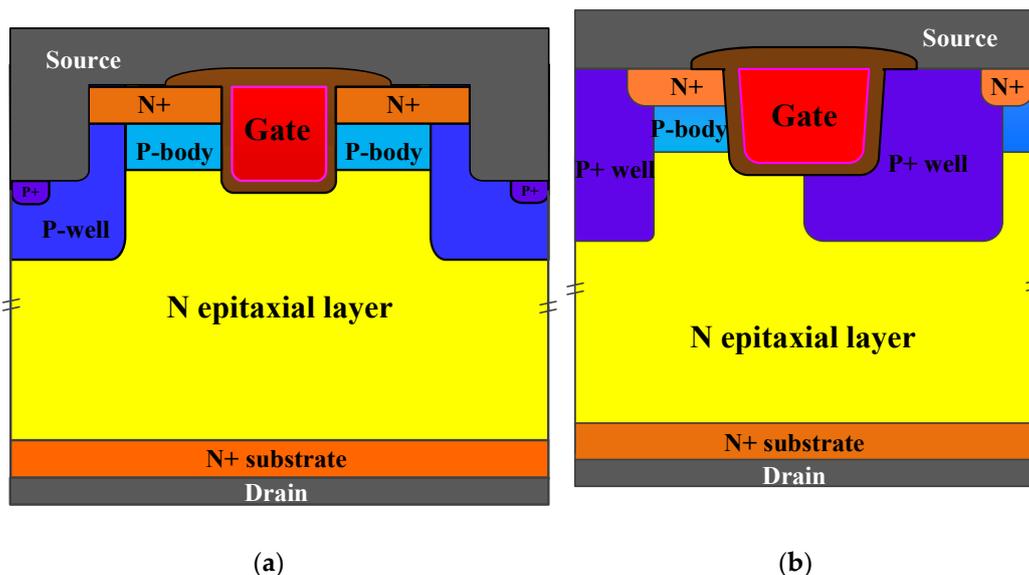


Figure 1. Schematic cross-sections of different trench-gate SiC MOSFETs. (a) The double-trench SiC MOSFET and (b) the asymmetric trench SiC MOSFET.

Table 1. Device electrical parameters.

Electrical Parameters	Double-Trench MOSFET (SCT3160KL)	Asymmetric Trench MOSFET (IMW120R140M1H)
R_{on} (m Ω)	160	140
I_D (A)	18	19
$BV@I_{dss} = 1 \mu A$ (V)	1814	1479

The double-trench SiC MOSFET has not only a gate trench to form the two vertical channels but also a source trench. The length and depth of each trench were both 1 μm . The P-well in the source trench can reduce the bottom electric field of the trench gate.

For an asymmetric trench SiC MOSFET, there is only one channel in a single cell. The right corner of the gate is surrounded by the highly doped deep P+ well, which extends to the bottom of the trench gate, protecting the left trench corner where current flows. As shown in Figure 1b, different from the double-trench device, the left trench sidewall of the asymmetric device was parallel to the (11–20) crystal plane. Since the N epitaxial layer is homoepitaxially grown on a 4° off-axis 4H–SiC (0001) substrate, the channel of the asymmetric trench SiC MOSFET is inclined [27]. At the same time, the (11–20) crystal plane provides twice the channel mobility of other crystal planes, which improves the current density of the asymmetric trench SiC MOSFET [27,28].

The cell pitch of the double-trench SiC MOSFET was 3.6 μm, while that of the asymmetric one was 3.2 μm. The doping concentrations of the P-body and N-drift region of the double-trench device were set to be $1 \times 10^{17} \text{ cm}^{-3}$ and $8 \times 10^{15} \text{ cm}^{-3}$, while those of the asymmetric one were $1 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{16} \text{ cm}^{-3}$, respectively. All the cell dimensions and the doping concentrations were modified based on the real device structures and the measured characteristics. The simulations performed in this paper were based on the device structures in Figure 1.

Figure 2 expresses the schematic circuit diagram of the avalanche stress system and the oscilloscope waveforms generated by the system on the asymmetric trench SiC MOSFET. A drive circuit controlled the ON and OFF of the device under testing (DUT). The gate-source voltage (V_{gs}) was set from 0 to 18 V. The DUT was connected in series with an inductor ($L = 1 \text{ mH}$). The power supply voltage (V_{DD}) was 100 V. As shown in Figure 2b, when the gate of the DUT turns ON, the drain-source current (I_{ds}) gradually rises. The rising slope of the current was proportional to the V_{DD} and inversely proportional to the inductance value:

$$\frac{di}{dt} = \frac{V_{DD}}{L} \quad (1)$$

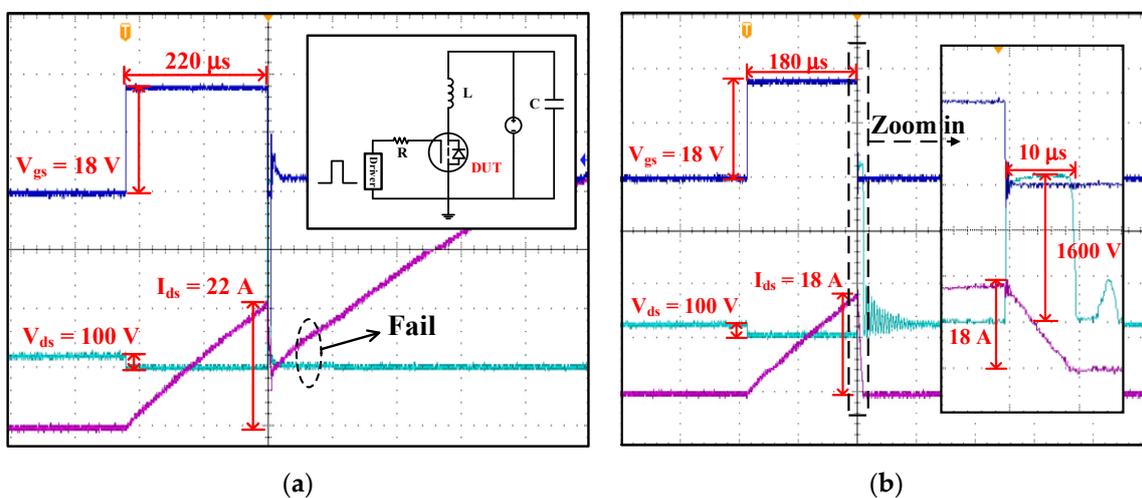


Figure 2. The avalanche waveforms of the asymmetric trench SiC MOSFET. (a) The failure waveforms and the schematic circuit diagram of the avalanche stress system. (b) The waveforms adopted to stress the device.

When the gate of the DUT turns OFF, the energy stored in the inductor is dissipated on the DUT. At this time, the SiC MOSFET is under the avalanche state. The V_{ds} equals to the BV and the current flows through the inductor following the formula:

$$\frac{di}{dt} = -\frac{BV - V_{DD}}{L} \quad (2)$$

When the current in the circuit falls to 0 A, the energy stored in the inductor is completely consumed and the avalanche state of the device ends.

When applying the avalanche stress on the device and gradually increasing the gate pulse width until it fails, the asymmetric trench SiC MOSFET can endure a peak I_{load} (I_{peak}) of 22 A, as shown in Figure 2a. All the three ports of the failed device were short-circuited, indicating that the device dies from thermal runaway [25]. The avalanche waveforms with an I_{peak} of 18 A, which is 80% of 22 A, as shown in Figure 2b, were adopted here to repetitively stress the asymmetric trench SiC MOSFET. The gate pulse width was 180 μ s and the I_{ds} increased to 18 A at a rate of 0.1 A/ μ s. After that, the gate of the device turns OFF and the device is under the avalanche state while the V_{ds} is kept at 1600 V.

The avalanche-induced failure waveforms of the double-trench SiC MOSFET are shown in Figure 3a. After enduring a 16 A-avalanche stress, the gate leakage current (I_{gss}) is higher than 1 μ A, indicating that the gate failure is the dominant mechanism [18,19]. Obviously, the asymmetric trench SiC MOSFET can endure much more serious single-pulse avalanche stress than the double-trench one, implying that the asymmetric structure has a better protection effect [25]. Similarly, the avalanche stress with 13 A I_{peak} , which is 80% the maximum avalanche current the device can endure, was adopted to stress the double-trench SiC MOSFET. The stress waveforms are presented in Figure 3b. The gate pulse width was 130 μ s. When under the avalanche state, the V_{ds} of the double-trench device is 1700 V.

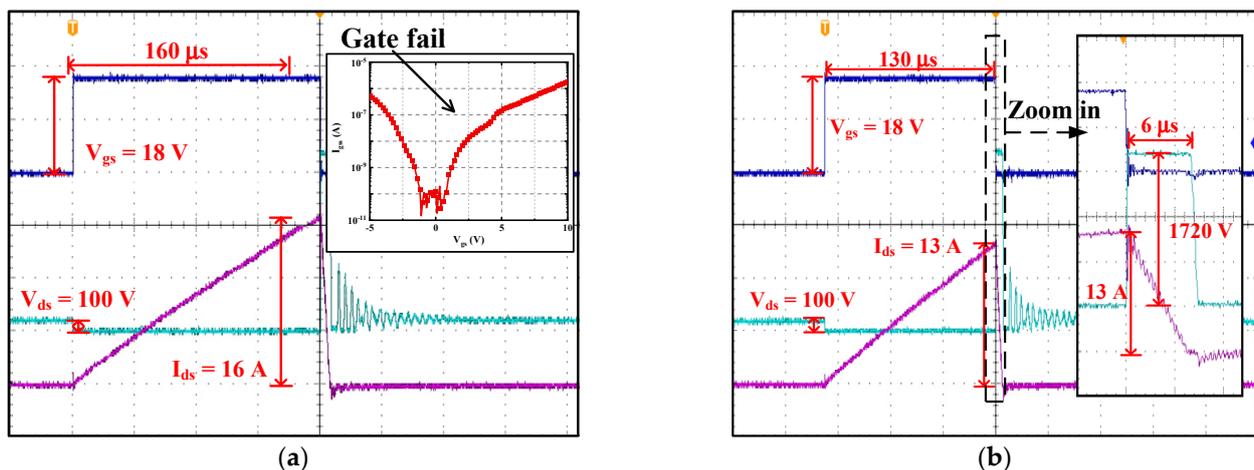


Figure 3. The avalanche waveforms of the double-trench SiC MOSFET. (a) The failure waveforms. (b) The waveforms adopted to stress the device.

In addition, during the repetitive avalanche stress experiments for both the devices, the duty cycle of all pulses was 0.1%. Wind heat dissipation was also added to suppress the rise in the junction temperature. The repetitive avalanche stress with extremely high voltage and current will lead to the degradation of the devices, which is going to be analyzed in Section 3.

3. Results and Discussions

3.1. Degradation of Electrical Characteristics

3.1.1. Asymmetric Trench SiC MOSFET

After enduring repetitive avalanche stress, the electrical characteristics under different stress cycles were measured and compared. Figure 4 shows the degradation in the threshold voltage (V_{th}) of the asymmetric trench SiC MOSFET. With the increase of the total stress cycles, the V_{th} curves shifted to the negative direction. The V_{th} under the condition of $V_{ds} = 1$ V and $I_{ds} = 2.5$ mA is extracted in Figure 4c. After enduring 10k cycles, the V_{th} of the asymmetric device dropped from 4.4 to 3.9 V. In the logarithmic scale, the V_{th} at $I_{ds} = 1$ nA was reduced by 1.15 V, as shown in Figure 4b, which is more obvious than that in the linear scale. This indicates that after enduring the repetitive avalanche stress, the channel of the asymmetric trench SiC MOSFET degrades.

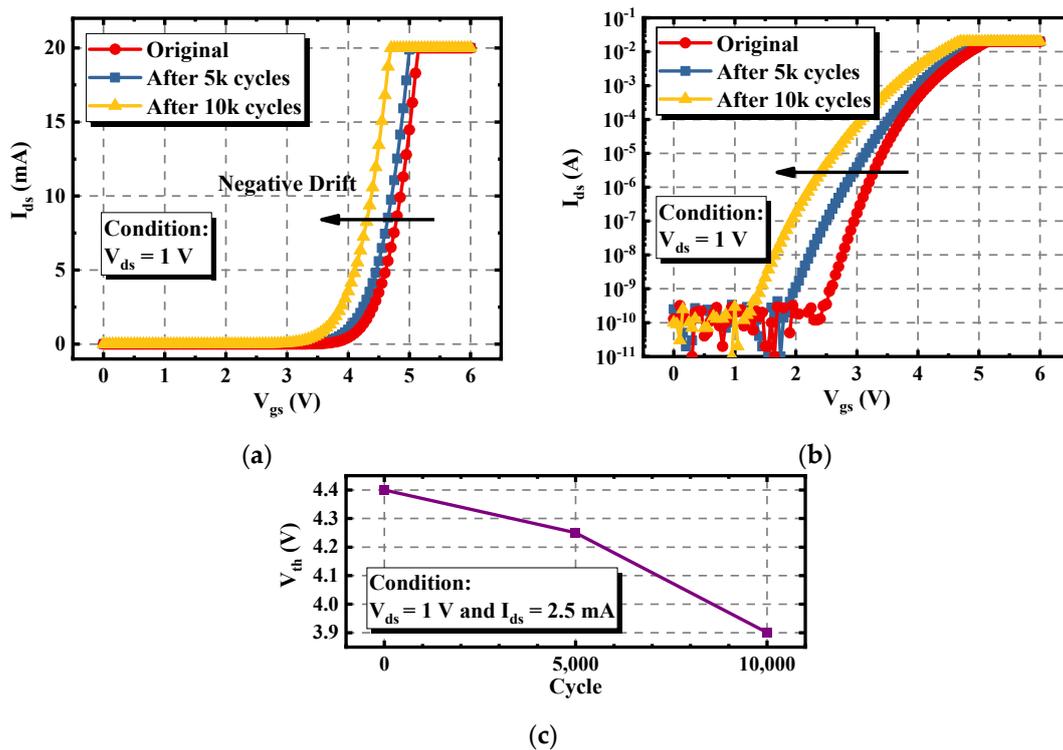


Figure 4. Variations of the I_d - V_g characteristic of the asymmetric trench SiC MOSFET under different avalanche stress cycles. (a) I_d - V_g curves in the linear scale. (b) I_d - V_g curves in the logarithmic scale. (c) Extracted degraded V_{th} .

The variations of the I_d - V_d characteristics of the asymmetric trench device under the conditions of $V_{gs} = 6\text{ V}$ and $V_{gs} = 18\text{ V}$ are plotted in Figure 5a,b. The I_{ds} under the condition of $V_{gs} = 6\text{ V}$ increased due to the decrease of the V_{th} . Meanwhile, the I_d - V_d curve remained stable when the device was biased under the condition of $V_{gs} = 18\text{ V}$. This is because the channel of the device was fully open and the channel resistance was relatively low when compared with the resistances of the junction field effect transistor (JFET) region and N-drift region. This also indicates that the JFET region and drift region of the asymmetric trench SiC MOSFET are rarely affected by the repetitive avalanche stress.

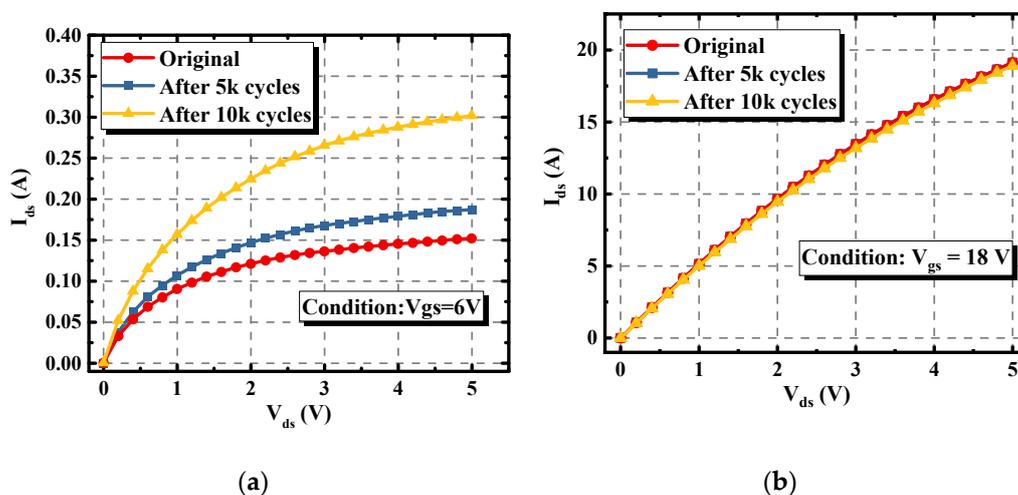


Figure 5. Variations of the I_d - V_d characteristic of the asymmetric trench SiC MOSFET under different avalanche stress cycles. (a) I_d - V_d curves under the $V_{gs} = 6\text{ V}$ bias condition. (b) I_d - V_d curves under the $V_{gs} = 18\text{ V}$ bias condition.

The variations of the capacitance characteristic of the asymmetric trench device were also measured. As shown in Figure 6, with the increase of the stress cycles, the gate-drain capacitance (C_{gd}) of the device increased slightly. Within 10k cycles, the maximum C_{gd} rose from 128 pF to 154 pF, equaling to an increment of 20.3%. This is because there were positive charges injected into the left corner and the bottom interface of the gate trench, which will be explained later in Section 3.2.

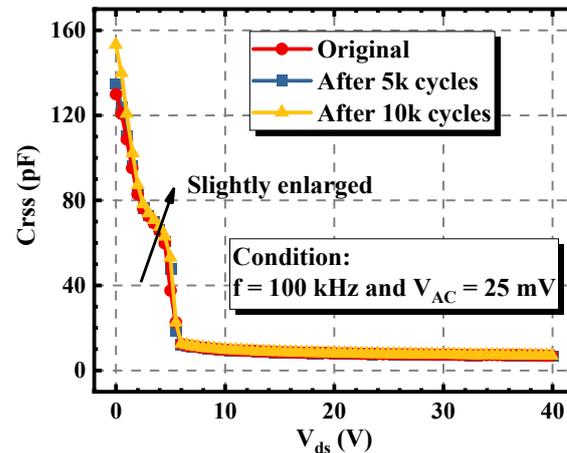


Figure 6. Variations of the C_{gd} of the asymmetric trench SiC MOSFET under different avalanche stress cycles.

3.1.2. Double-Trench SiC MOSFET

The repetitive avalanche experiment was also performed on the double-trench SiC MOSFET. As can be seen in Figure 7, the V_{th} of the device only expressed a slight negative shift during the experiment, implying that the channel of the device was rarely degraded, which is quite different from the phenomenon monitored in Figure 4. Meanwhile, as shown in Figure 8, with the increase of the stress cycles, the I_d - V_d curve under the condition of $V_{gs} = 18$ V rose significantly. This means that the R_{on} at $V_{gs} = 18$ V and $I_{ds} = 18$ A was decreased by 14%.

The repetitive avalanche experiment was also performed on the double-trench SiC MOSFET. As can be seen in Figure 7, the V_{th} of the device only expressed a slight negative shift during the experiment, implying that the channel of the device was rarely degraded, which is quite different from the phenomenon monitored in Figure 4. Meanwhile, as shown in Figure 8, with the increase of the stress cycles, the I_d - V_d curve under the condition of $V_{gs} = 18$ V rose significantly.

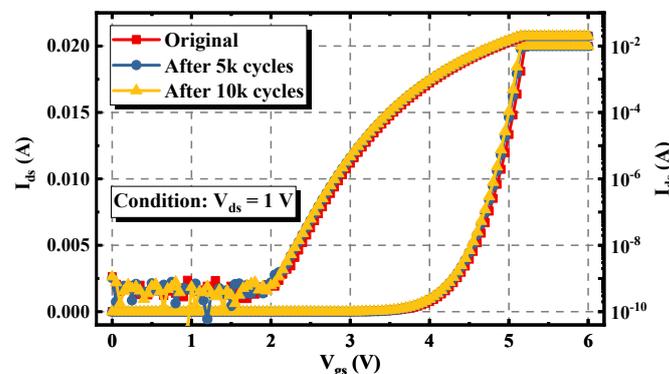


Figure 7. Extracted I_d - V_g characteristic of the double-trench SiC MOSFET under different avalanche stress cycles.

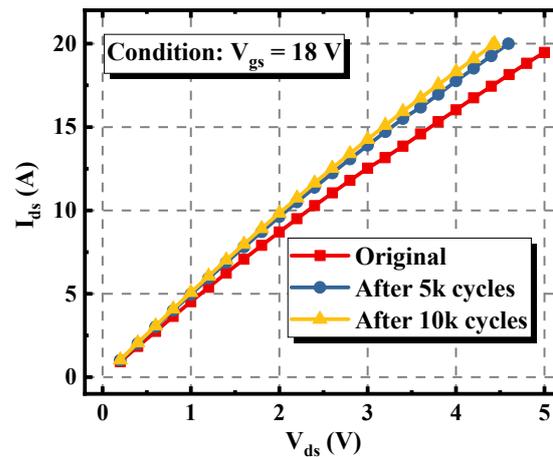


Figure 8. Variations of the I_d - V_d characteristic at $V_{gs} = 18$ V of the double-trench SiC MOSFET under different avalanche stress cycles.

As plotted in Figure 9, after enduring 10k avalanche stress cycles, the maximum C_{gd} of the double-trench device increased from 274 pF to 397 pF, equaling to an increment of 44.9%. This obvious degradation resulted from the positive charges injected into the bottom oxide [20]. This indicates that compared with the asymmetric trench SiC MOSFET, much more positive charges were injected into the trench bottom oxide of the double-trench device during the avalanche process, making the C_{gd} change greatly. At the same time, the positive charges attracted electrons and decreased the resistance of the JFET region. Therefore, the V_{th} of the double-trench SiC MOSFET was unchanged while the R_{on} was reduced.

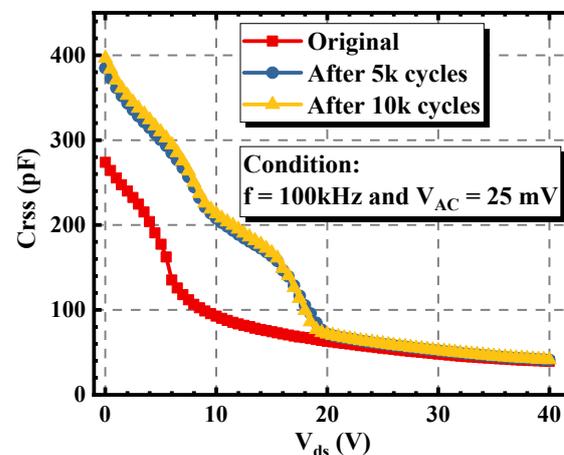


Figure 9. Variations of the C_{gd} of the double-trench SiC MOSFET under different avalanche stress cycles.

3.2. Simulations and Analysis

Simulations were then performed to help analyze the various degradation trends between the two types of devices with different structures. Figure 10a reflects the electric field distribution of the double-trench SiC MOSFET under the avalanche state. The highest electric field was located at the bottom of the source trench, where the avalanche breakdown occurred. Meanwhile, the electric field at the gate trench cannot be ignored. The oxide electric field (E_{ox}) and the impact ionization rate (I.I.) along the gate oxide interface are extracted in Figure 10b. The peak value of the E_{ox} appeared at the bottom, pointing from the semiconductor to the oxide, while the peak I.I. appeared at the corners. This illustrates that the E_{ox} and I.I. at the bottom and corners of the trench together lead to the injection of positive charges into the gate oxide, resulting in an increase in C_{gd} and decrease in the

resistance of the JFET region. There was no I.I. in the channel region of the double-trench device, meaning that the channel was not affected by the stress, which is consistent with the measured data in Figure 7.

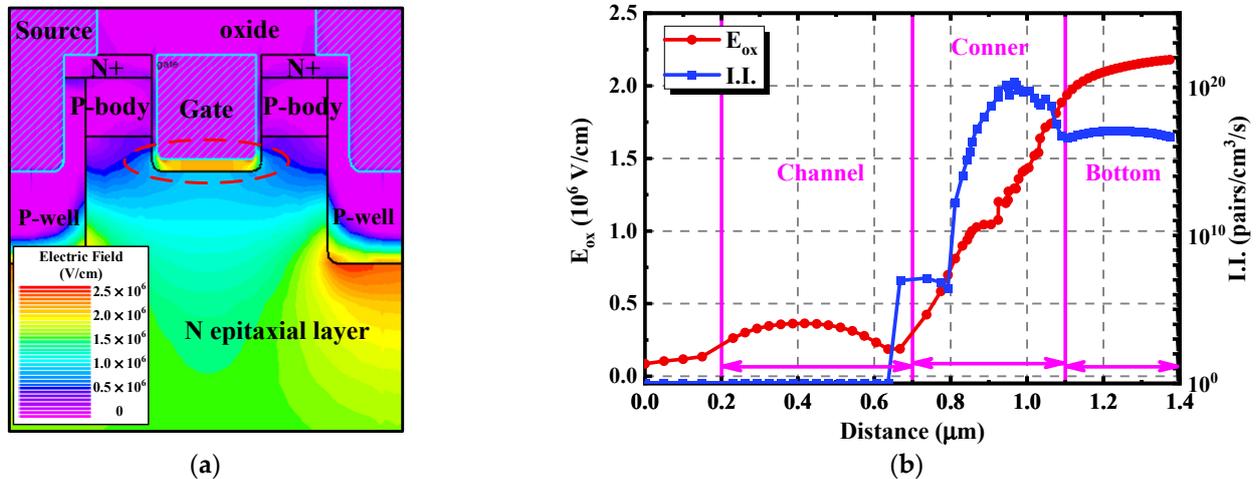


Figure 10. Physical characteristics of the double-trench SiC MOSFET under the avalanche state. (a) Distribution of the electric field. (b) Extracted E_{ox} and I.I. along the gate oxide interface.

Furthermore, an asymmetric trench SiC MOSFET structure with a vertical channel was built to help analyze the different degradations resulting from the double-trench and the asymmetric structures, ignoring the influence brought by the inclined channel. The physical characteristics of it under the avalanche state are shown in Figure 11. As can be seen in Figure 11a, the peak value of the electric field was located at the bottom of the deep P+ well. Different from the double-trench SiC MOSFET, due to the narrower JFET region, the serious E_{ox} did not appear at the bottom of the trench in the asymmetric device. Comparing Figure 11b with Figure 10b, it can be concluded that both the E_{ox} and the I.I. along the trench bottom and the corner of the asymmetric device are much lower than those in the double-trench device. The peak E_{ox} fell from 2.18×10^6 V/cm to 8.51×10^5 V/cm, decreasing by 61.0%. Meanwhile, the peak I.I. reduced from 1.46×10^{20} pairs/cm³/s to 1.70×10^{17} pairs/cm³/s, equating to a nearly three-orders of magnitude reduction. This demonstrates that the deep P+ well in the asymmetric trench SiC MOSFET can protect the bottom gate oxide well. This is why the double-trench SiC MOSFET shows much more serious degradation in the C_{gd} and the I_d - V_d curve under the high gate bias condition. Moreover, it is worth noting that there existed a 3.80×10^7 pairs/cm³/s I.I. peak in the channel, even though it was still minor.

The real asymmetric trench SiC MOSFET produced by Infineon adopted the (11–20) crystal plane to form the channel, making the channel inclined. Figure 12 simulates the physical characteristics of the device. The most obvious difference between Figures 12b and 11b is that a much higher I.I., reaching a peak value of 7.14×10^{14} pairs/cm³/s, appears at the inclined channel region. This is because the inclined crystal plane made the channel become exposed to the avalanche stress, promoting the positive charges to be injected into the channel oxide. Therefore, the V_{th} of the asymmetric trench SiC MOSFET continued to decrease, just as presented in Figure 4. The simulation results are mostly agreeable with the measured data, proving the correctness of the mechanisms discovered and the investigation made in this work.

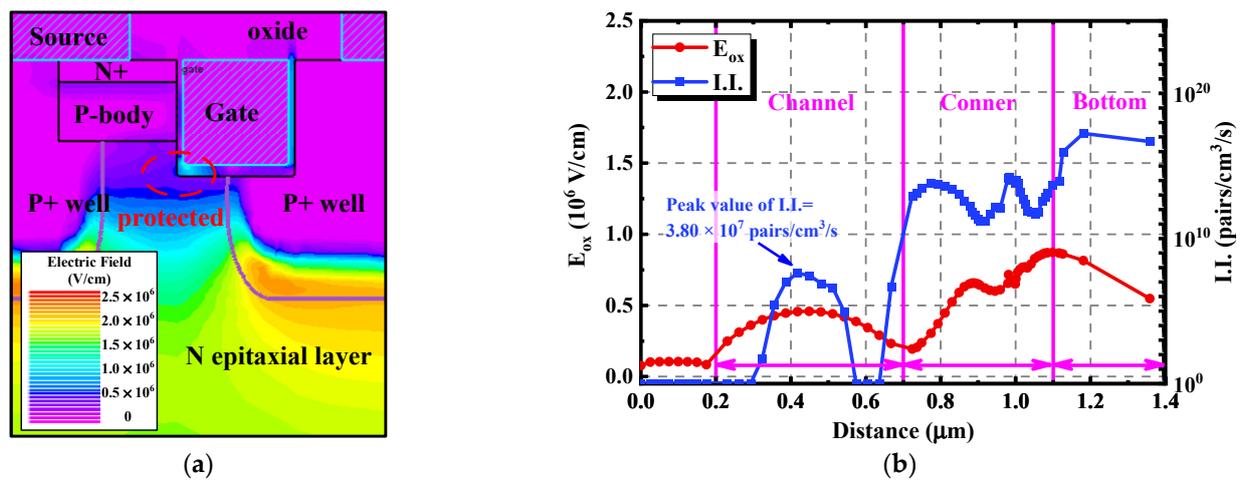


Figure 11. Physical characteristics of the asymmetric trench SiC MOSFET with a vertical channel under the avalanche state. (a) Distribution of the electric field. (b) Extracted E_{ox} and I.I. along the gate oxide interface.

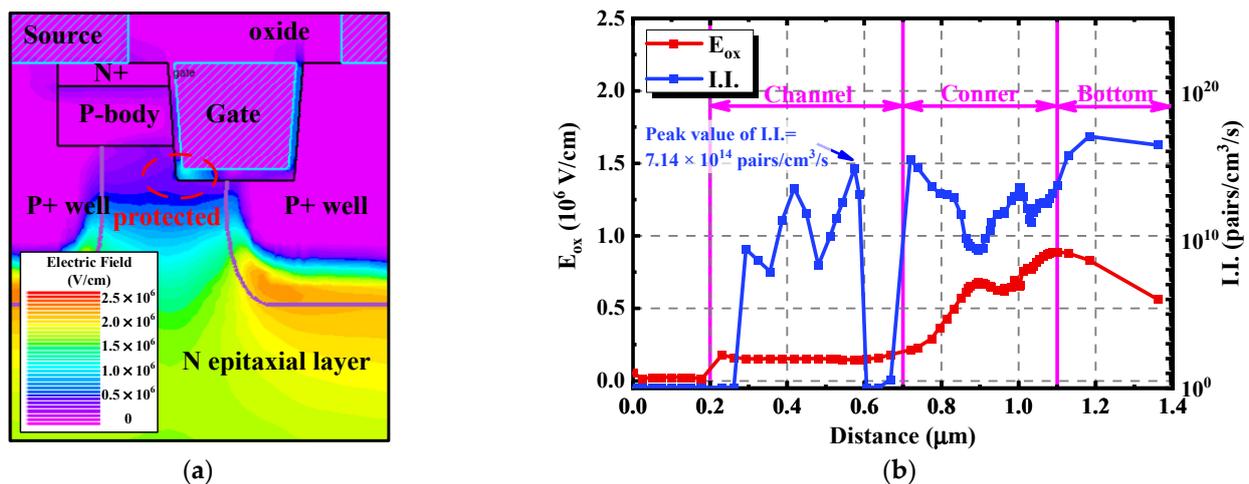


Figure 12. Physical characteristics of the asymmetric trench SiC MOSFET with an inclined channel under the avalanche state. (a) Distribution of the electric field. (b) Extracted E_{ox} and I.I. along the gate oxide interface.

4. Conclusions

Based on the measured discrepant degradation trends between the double-trench SiC MOSFET and the asymmetric trench SiC MOSFET before and after enduring the repetitive avalanche stress, the mechanisms brought by the different device structures were revealed. On the one hand, since ultrahigh peak values of E_{ox} and I.I. appeared at the bottom oxide of the double-trench SiC MOSFET under the avalanche state, the positive charges injected there contributed to the obvious decrease of the R_{on} and to the increase of the C_{gd} . These phenomena were not observed in the asymmetric trench device because the deep P+ well protected the bottom gate oxide well. On the other hand, the inclined channel of the asymmetric device attracted a much higher I.I. in the channel region, leading more positive charges to be injected into the oxide there. Hence, the degradation of the V_{th} of the asymmetric trench SiC MOSFET was more obvious. The differences in the degradation brought about by the different device structures were summarized and verified. Different from the double-trench SiC MOSFET, the gate oxide at the corner of the trench of the asymmetric trench SiC MOSFET device was well protected. However, when adopting inclined channel, the channel of the asymmetric device is more vulnerable to damage.

Therefore, the reliability of both the bottom and the sidewall of the trench needs to be considered in the trench design. It is believed that for these two types of trench-gate SiC MOSFETs, there also exists different degradation phenomena induced by other repetitive stresses, such as the short-circuit stress, the power cycling stress, and the surge current stress, which will be studied in detail in the future.

Author Contributions: Conceptualization, J.W., Z.W. and H.F.; methodology, J.W., S.L. (Sheng Li), L.Z. and S.L. (Siyang Liu); software, Z.W., H.F. and X.Y.; investigation, J.W., Z.W., H.F. and X.Y.; data curation, Z.W., H.F., S.L. (Sheng Li), and L.Z.; writing—original draft preparation, Z.W.; writing—review and editing, J.W., S.L. (Siyang Liu), W.S., W.W. and S.B.; funding acquisition, J.W., S.L. (Siyang Liu), W.S., W.W. and S.B. All authors have read and agreed to the published version of the manuscript.

Funding: This research study was funded in part by the National Key R&D Program of China under grant 2020YFF0218501; in part by the National Natural Science Foundation of China under grant 62004037; in part by the Fund for Transformation of Scientific and Technological Achievements of Jiangsu Province under grant BA2020027; in part by the Foundation of State Key Laboratory of Wide-bandgap Semiconductor Power Electronics Devices under grant 2021KF003; and in part by the Distinguished Young Scholars Program of Southeast University.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data sharing is not applicable for this article.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Takeyama, A.; Makino, T.; Okubo, S.; Tanaka, Y.; Yoshie, T.; Hijikata, Y.; Ohshima, T. Radiation Response of Negative Gate Biased SiC MOSFETs. *Materials* **2019**, *12*, 2741. [[CrossRef](#)] [[PubMed](#)]
2. She, X.; Huang, A.Q.; Lucia, Ó.; Ozpineci, B. Review of Silicon Carbide Power Devices and Their Applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8193–8205. [[CrossRef](#)]
3. Mantooth, H.A.; Glover, M.D.; Shepherd, P. Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2014**, *2*, 374–385. [[CrossRef](#)]
4. Hamada, K.; Nagao, M.; Ajioka, M.; Kawai, F. SiC—Emerging Power Device Technology for Next-Generation Electrically Powered Environmentally Friendly Vehicles. *IEEE Trans. Electron Devices* **2015**, *62*, 278–285. [[CrossRef](#)]
5. Palmour, J.W. Silicon Carbide Power Device Development for Industrial Markets. In Proceeding of the IEEE International Electron Devices Meeting (IEDM) 2014, San Francisco, CA, USA, 15–17 December 2014; pp. 1.1.1–1.1.8, ISBN 978-1-4799-8001-7.
6. Sabri, S.; Brunt, E.V.; Barkley, A.; Hull, B.; O’Loughlin, M.; Burk, A.; Allen, S.; Palmour, J. New Generation 6.5 kV SiC Power MOSFET. In Proceeding of the IEEE the Workshop on Wide Bandgap Power Devices and Applications (WiPDA) 2017, Albuquerque, NM, USA, 30 October–1 November 2017; pp. 246–250, ISBN 978-1-5386-3117-1.
7. Giovanni, F.D.; Buonomo, S. Latest Developments in Silicon Carbide MOSFETs: Advantages and Benefits vs. Application. In Proceeding of the AEIT Annual Conference 2013, Mondello, Italy, 3–5 October 2013; pp. 1–6, ISBN 978-8-8872-3732-0.
8. Anwar, S.; Wang, Z.J.; Chinthavali, M. Characterization and Comparison of Trench and Planar Silicon Carbide (SiC) MOSFET at Different Temperatures. In Proceeding of the IEEE Transportation Electrification Conference and Expo (ITEC) 2018, Long Beach, CA, USA, 13–15 June 2018; pp. 1039–1045, ISBN 978-1-5386-3048-8.
9. Na, J.; Cheon, J.; Kim, K. 4H-SiC Double Trench MOSFET with Split Heterojunction Gate for Improving Switching Characteristics. *Materials* **2021**, *14*, 3554. [[CrossRef](#)] [[PubMed](#)]
10. Tian, K.; Hallén, A.; Qi, J.; Nawaz, M.; Ma, S.; Wang, M.; Guo, S.; Elgammal, K.; Li, A.; Liu, W. Comprehensive Characterization of the 4H-SiC Planar and Trench Gate MOSFETs From Cryogenic to High Temperature. *IEEE Trans. Electron Devices* **2019**, *66*, 4279–4286. [[CrossRef](#)]
11. Huang, W.; Deng, X.; Li, X.; Wen, Y.; Li, X.; Li, Z.; Zhang, B. Investigation of Surge Current Reliability of 1200V Planar and Trench SiC MOSFET. In Proceedings of the IEEE 15th International Conference on Solid-State & Integrated Circuit Technology (ICSICT) 2020, Kunming, China, 3–6 November 2020; pp. 1–3, ISBN 978-1-7281-6235-5.
12. Aichinger, T.; Schmidt, M. Gate-oxide reliability and failure-rate reduction of industrial SiC MOSFETs. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS) 2020, Dallas, TX, USA, 28 April–30 May 2020; pp. 1–6, ISBN 978-1-7281-3199-3.
13. Nakamura, T.; Nakano, Y.; Aketa, M.; Nakamura, R.; Mitani, S.; Sakairi, H.; Yokotsujiet, Y. High Performance SiC Trench Devices with Ultra-low Ron. In Proceeding of the IEEE International Electron Devices Meeting (IEDM) 2011, Washington, DC, USA, 5–7 December 2011; pp. 26.5.1–26.5.3, ISBN 978-1-4577-0505-2.

14. Peters, D.; Siemieniec, R.; Aichinger, T.; Basler, T.; Esteve, R.; Bergner, W.; Kueck, D. Performance and Ruggedness of 1200V SiC-Trench-MOSFET. In *Proceeding of the International Symposium on Power Semiconductor Devices and IC's (ISPSD) 2017*, Sapporo, Japan, 28 May–1 June 2017; pp. 239–242, ISBN 978-4-88686-096-5.
15. Boige, F.; Richardeau, F. Gate leakage-current analysis and modelling of planar and trench power sic mosfet devices in extreme short-circuit operation. *Microelectron. Rel.* **2017**, *76–77*, 532–538. [[CrossRef](#)]
16. Wei, J.; Liu, S.; Tong, J.; Zhang, X.; Sun, W.; Huang, A.Q. Understanding Short-Circuit Failure Mechanism of Double-Trench SiC Power MOSFETs. *IEEE Trans. Electron Devices* **2020**, *67*, 5593–5599. [[CrossRef](#)]
17. Yao, K.; Yano, H.; Tadano, H.; Iwamuro, N. Investigations of SiC MOSFET Short-Circuit Failure Mechanisms Using Electrical, Thermal, and Mechanical Stress Analyses. *IEEE Trans. Electron Devices* **2020**, *67*, 4328–4334. [[CrossRef](#)]
18. Wei, J.; Liu, S.; Zhao, H.; Fu, H.; Sun, W. Verification of Single-Pulse Avalanche Failure Mechanism for Double-Trench SiC Power MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 2190–2200. [[CrossRef](#)]
19. Li, X.; Tong, X.; Hu, R.; Wen, Y.; Zhu, H.; Deng, X.; Sun, Y.; Chen, W. Failure Mechanism of Avalanche Condition for 1200V Double Trench SiC MOSFET. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 2147–2154. [[CrossRef](#)]
20. Wei, J.; Liu, S.; Yang, L.; Tang, L.; Lou, R.; Li, T.; Fang, J.; Li, S.; Zhang, C.; Sun, S. Investigations on the Degradations of Double-Trench SiC Power MOSFETs Under Repetitive Avalanche Stress. *IEEE Trans. Electron Devices* **2019**, *66*, 546–552. [[CrossRef](#)]
21. Wang, Z.; Li, Y.; Sun, X.; Liu, Y.; Zhu, Z.; Ren, N.; Guo, Q. Reliability Investigation on SiC Trench MOSFET under Repetitive Surge Current Stress of Body Diode. In *Proceeding of the IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia) 2020*, Suita, Japan, 23–25 September 2020; pp. 1–4, ISBN 978-1-7281-5955-3.
22. Fu, H.; Wei, J.; Yan, X.; Zhao, H.; Liu, S. Degradation Investigations on Asymmetric Trench SiC Power MOSFETs Under Repetitive Unclamped Inductive Switching Stress. In *Proceeding of the International Symposium on Power Semiconductor Devices and IC's (ISPSD) 2021*, Nagoya, Japan, 30 May–3 June 2021; pp. 239–242, ISBN 978-4-88686-422-2.
23. Deng, X.; Li, X.; Li, X.; Zhu, H.; Xu, X.; Wen, Y.; Sun, Y.; Chen, W.; Li, Z.; Zhang, B. Short-Circuit Capability Prediction and Failure Mode of Asymmetric and Double Trench SiC MOSFETs. *IEEE Trans. Power Electron.* **2020**, *36*, 8300–8307. [[CrossRef](#)]
24. Zhu, Z.; Xu, H.; Liu, L.; Ren, N.; Sheng, K. Investigation on Surge Current Capability of 4H-SiC Trench-Gate MOSFETs in Third Quadrant Under Various VGS Biases. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *9*, 6361–6369. [[CrossRef](#)]
25. Deng, X.; Zhang, B.; Zhu, H.; Li, X.; Zhou, K. Investigation and Failure Mode of Asymmetric and Double Trench SiC MOSFETs Under Avalanche Conditions. *IEEE Trans. Power Electron.* **2020**, *35*, 8524–8531. [[CrossRef](#)]
26. Yao, K.; Yano, H.; Iwamuro, N. Investigations of UIS Failure Mechanism in 1.2 kV Trench SiC MOSFETs Using Electro-Thermal-Mechanical Stress Analysis. In *Proceeding of the International Symposium on Power Semiconductor Devices and IC's (ISPSD) 2021*, Nagoya, Japan, 30 May–3 June 2021; pp. 115–118, ISBN 978-4-88686-422-2.
27. Siemieniec, R.; Peters, D.; Esteve, R.; Bergner, W.; Kück, D.; Aichinger, T.; Basler, T.; Zippelius, B. A SiC Trench MOSFET concept offering improved channel mobility and high reliability. In *Proceeding of the European Conference on Power Electronics and Applications (EPE'17 ECCE Europe) 2017*, Warsaw, Poland, 11–14 September 2017; pp. 1–13, ISBN 978-90-75815-27-6.
28. Kimoto, T.; Yoshioka, H.; Nakamura, T. Physics of SiC MOS Interface and Development of Trench MOSFETs. In *Proceeding of the IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA) 2013*, Columbus, OH, USA, 27–29 October 2013; pp. 135–138, ISBN 978-1-4799-1194-3.