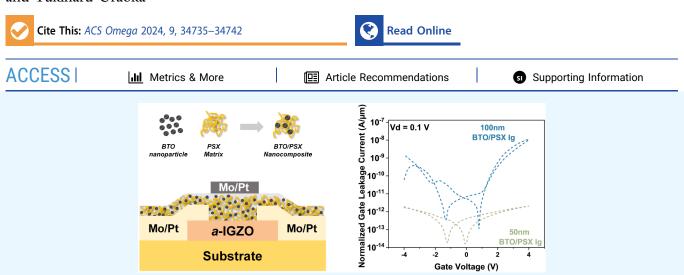


http://pubs.acs.org/journal/acsodf

Article

Effect of Average Grain Size on the Uniformity and Ferroelectricity of BTO/PSX Thin Films Processed by Low-Temperature Solution Method

Chuanjun Wu, Juan Paolo S. Bermundo,* Aimi Syairah Safaruddin, Atsuko Yamamoto, and Yukiharu Uraoka



ABSTRACT: In this study, we utilized 50 nm BaTiO₃ (BTO) nanoparticles and polysiloxane (PSX) with a higher concentration of methyl and silica groups to fabricate insulating layers at a low curing temperature of 100 °C using a solution-based method. This approach aims to enhance film uniformity while retaining the ferroelectric properties. Consequently, we maintained a minimal leakage current in thin-film transistors (TFTs) while achieving transfer characteristics characterized by a distinct hysteresis. Moreover, we verified the presence of ferroelectricity in 50 nm BTO nanoparticles. Compared with prior research, we confirm that decreasing nanoparticle size effectively reduces film roughness but also leads to a reduction in polarization intensity due to smaller diameter BTO nanoparticles. Additionally, a higher proportion of methyl and silica groups effectively lowers the curing temperature of PSX. At the same time, the hydrogen ions released in the polycondensation reaction can also effectively suppress the oxygen vacancies at the interface between dielectric and channel layers, improving the TFT electrical characteristics.

INTRODUCTION

The exponential growth in integrated computing units per chip according to Moore's Law has far outpaced improvements in memory and storage performance. This imbalance between processing speed and memory bandwidth has become a major bottleneck limiting further gains in overall system performance. To solve this memory wall problem, FeFET with integrated nonvolatile ferroelectric memories is a promising solution. Ferroelectric materials can enable nonvolatile, highspeed, high-density memory embedded with logic on the same device.² Integrating computing and storage in this way can lead to synergistic improvements, allowing the memory bandwidth to scale alongside raw computing power.

If ferroelectric memory technology continues to mature, manufacturers could embed extremely fast, yet persistent, memory directly into processors and accelerators. This colocalization of processing and storage would greatly alleviate the memory wall issue and help sustain the performance gains from scaling of transistors and computing units per chip.^{3,4} The end goal is to achieve a balanced system architecture in which memory bandwidth and latency can keep pace with rapidly improving computational throughput.

In recent years, research on nonvolatile memory devices has garnered significant attention. Nonvolatile memories can retain stored states even after power is turned off, offering advantages such as low power consumption, high speed, and high density. 5-7 Ferroelectric materials, with their unique ferroelectric properties and high dielectric constants, show great promise for applications in nonvolatile memory devices.8

Among various ferroelectric materials, BaTiO3 (BTO) has emerged as a promising candidate for ferroelectric memory applications. BTO is a prototypical perovskite ferroelectric

Received: April 24, 2024 Revised: July 5, 2024 Accepted: July 15, 2024 Published: July 29, 2024





ceramic material that has been extensively studied since its initial synthesis. Over the past few decades, researchers have deeply investigated BTO's crystal structure, phase transition behavior, nanoscale grain fabrication, and thin film deposition. Prior research has shown that BTO ferroelectric films prepared by the solution method have dielectric constants (k) ranging from 5.21 to 7.70⁹ and pronounced ferroelectricity, making it a potential material for nonvolatile memory applications. The high k-value and ferroelectric properties of BTO enable the fabrication of thin-film transistor (TFT) devices with nonvolatile storage capabilities. Specifically, the pronounced ferroelectric polarization of BTO thin films can be leveraged to store data states in a nonvolatile manner. By integrating ferroelectric BTO as the gate dielectric in TFTs, the high dielectric constant of BTO can effectively enhance the capacitance of the dielectric layer to obtain a higher output current between the source/drain. Therefore, exploiting the unique characteristics of the perovskite ferroelectric BTO allows the development of nonvolatile ferroelectric memory TFTs for computing in memory FET devices.

However, in the case of BTO film preparation, ceramic materials typically necessitate high heat treatment temperatures, exceeding 650 °C, to achieve uniform components and complete crystallization. Nevertheless, BTO undergoes a ferroelectric-to-paraelectric phase transition near its Curie temperature (around 120 °C). Although this phase transition process is reversible, it can still lead to the rearrangement of ferroelectric domains, generation of defects, and reduction in macroscopic polarization strength. Particularly in TFT devices, if the BTO ferroelectric thin film undergoes annealing at temperatures higher than the Curie temperature after its fabrication, these issues can make device performance difficult to control and the reliable fabrication of TFT devices challenging. Therefore, reducing the heat treatment temperature below the phase transition temperature while ensuring high film uniformity and low leakage current becomes a challenging task for this research.

Recent studies have shown that enhancing memory properties can be accomplished by combining a polymer matrix with small organic/inorganic molecules or metal nanoparticles. 11 In this study, inorganic-organic polysiloxane (PSX) was selected owing to its potential for electronic applications and attributes, including transparency and exceptional thermal and chemical resistance. PSX typically possesses a low k-value of 3.0. However, the addition of a polymer matrix into BTO improves the nanocomposite's thermal and mechanical stability and flexibility. Moreover, the spin coating technique can be utilized to facilitate processes with a controlled viscosity, contingent on the chemical formula. PSX has the potential to undergo complete polymerization at low temperatures, making it suitable for flexible substrates depending upon the functionalization of the constituent groups. As a result, the PSX polymer matrix was chosen to reduce both the leakage current from BTO and the curing temperature of the film.

In our prior studies, we have tried to prepare dielectric layer films of TFTs using 20 and 100 nm BTO combined with PSX. As a result, ferroelectricity was found only in the 100 nm diameter BTO/PSX film. However, because the surface of the film is too rough, it is not favorable for the subsequent preparation of TFT devices. ¹²

The present investigation involved the fabrication of dielectric layers for TFTs by combining PSX and BTO

nanoparticles with 50 nm diameter in varying compositional ratios. In an effort to reduce leakage current, BTO with smaller nanoparticles may aid in reducing surface roughness and enhancing the interfacial quality between the gate/dielectric and channel layers. Furthermore, the purpose of the PSX component, which features customized functional group ratios, is to optimize the oxygen vacancy ($V_{\rm O}$) concentration at the interface between the dielectric and channel. The implementation of this PSX engineering methodology has the potential to augment the devices' overall output characteristics.

METHOD

The deposition of BTO/PSX film is used for uniformity measurement, deposition of BTO nanoparticles, and fabrication process of samples. The procedure for film preparation is as follows.

The experimental reagents were placed in a room-temperature environment for 1 h. Then, several BTO nanoparticle solution samples and PSX samples were premixed in microcentrifuge tubes in the appropriate proportions. Subsequently, vigorous shaking at 37 kHz in Ultrasonic Cleaner was done for 20 min to thoroughly combine the samples. Finally, the samples were deposited onto the substrate surface using a spin coater. The substrate was placed on the spin coater chuck, and the sample solution was dispensed onto the center of the substrate. The spin coater was set to ramp up to 1000 rpm and maintain that speed for 3 s to spread the solution evenly across the substrate. The speed was then increased to 8000 rpm and held for 20 s to thin the film to the desired thickness. Finally, the speed was decreased to 6000 rpm for 2 s for a smooth, gradual slowdown. After spin coating, the samples were cured at 100 °C for 1 h to fully cure and remove any remaining solvent.

MOS capacitors comprised of metal (Al)-oxide (BTO/ PSX)-semiconductor (Si) were fabricated to verify hysteresis in C-V testing. Before proceeding, a SiO₂/Si substrate measuring 1 cm × 1 cm was cleaned through a sulfuric acid/hydrogen peroxide mix (SPM) and buffered hydrofluoric acid (BHF) etching. Electron-beam deposition (EB) was utilized to deposit a 100 nm thick Al electrode onto the substrate's underside. Annealing was conducted for 1 h at 300 °C in an N₂ environment. Following the application of a photoresist to shield the electrode, subsequent BHF etching was conducted to etch the SiO₂ residue on the substrate surface resulting from the annealing process. BTO/PSX film was subsequently spincoated onto the surface of the substrate and cured at 100 °C for 1 h. To finalize the MOS capacitor, electrodes are deposited on top of the film using EB, as shown in Figure 1a. The MOS capacitor's C-V characteristics were subsequently evaluated utilizing an E49800A Precision LCR meter (Agilent).

In order to conduct polarization-electric field (P-E) measurements, a metal-insulator-metal (MIM) device was

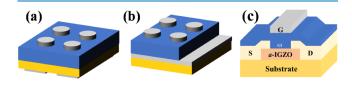


Figure 1. Device structure: (a) metal—oxide—semiconductor (MOS) device, (b) metal—insulator—metal (MIM) device, and (c) top-gate thin film transistor (TFT) device.

constructed. The fabrication procedures mirrored those used in the fabrication of the MOS device, including sample cleaning. As the bottom electrode, an Al film 100 nm in thickness was deposited on the surface of the sample by EB deposition. A BTO/PSX insulating film was spin-coated onto the surface of the sample and allowed to cure at a temperature of 100 °C for an hour. Ultimately, a 100 nm thickness of Al with a 300 μm diameter was deposited via EB in order to function as the upper electrode, as shown in Figure 1b. In order to validate the ferroelectricity and polarization characteristics of the BTO/PSX films, a Sawyer–Tower circuit was constructed and P–E measurements were conducted utilizing a Tektronix DPO 2002B Digital Phosphor Oscilloscope and KEYSIGHT 33500B Waveform Generator to produce a sinusoidal signal.

TFT devices with a top-gate structure were prepared to confirm the ferroelectric hysteresis performance by characterizing the hysteresis window size. SPM-cleaned 1 cm × 1 cm SiO₂/Si is utilized as the substrate. IGZO with a thickness of 70 nm was deposited via radio frequency (RF) magnetron sputtering. The sputtering was performed at a power of 100W for a total time of 12 min and 27 s, which included a 5 min presputtering step followed by 7 min and 27 s of actual sputtering. The sputtering chamber was maintained at a vacuum level of 0.0045 Torr, and the sputtering atmosphere consisted of argon (Ar) gas flowing at 19.1 sccm and oxygen (O2) gas flowing at 0.9 sccm. These sputtering conditions resulted in an IGZO channel thickness of 70 nm. Photolithography and wet etching were employed to pattern the oxide channel layer. Using RF magnetron sputtering, Ti/Pt (80/20 nm) was deposited, and the electrode layer was also patterned via lithography and a lift-off process. Then channel layer and electrode layer require annealing treatment at 300 °C for 1 h in a gas environment of $N_2:O_2 = 4:1$. Following this, a BTO/PSX film is applied onto the surface and cured for 1 h at 100 °C. The top gate electrode is once more composed of Ti/ Pt (80/20 nm) deposited via RF sputtering (see Figure 1c for the TFT structure) Utilizing a semiconductor parameter analyzer (Agilent Technologies B1500A Semiconductor Device Analyzer), the top gate TFT was characterized.

■ RESULT AND DISCUSSION

Using atomic force microscopy (AFM), the surface roughness of 100 and 50 nm BTO/PSX films were examined. By comparing the root-mean-square roughness (Rq) of the two samples, it can be clearly found that the roughness of the BTO/PSX films is significantly reduced after the reduction of the nanoparticle size, as shown in Figure 2a,b. The 50 nm nanoparticle size of the BTO/PSX films also exhibited better film uniformity. Also comparing the actual TFT, as shown in Figure 2c,d, a better film uniformity is observed for the TFT with 50 nm BTO/PSX and is expected to effectively control the leakage current level of the device through the improvement of the interface quality at the gate electrode and channel layers.

The thickness of the film was also confirmed by scanning electron microscopy (SEM) cross section, while energy-dispersive X-ray spectroscopy (EDX) confirmed the distribution of BTO nanoparticles throughout the film bulk, as shown in Figure S1a,b. In EDX characterization, the EDX elemental mapping of Ti or Ba clearly shows that the distribution is continuous and there are no obvious aggregation areas, which

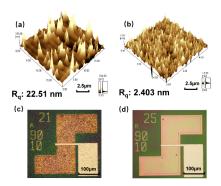


Figure 2. (a) 100 nm particle size BTO/PSX films' surface irregularity. (b) 50 nm particle size BTO/PSX films surface irregularity. (c) Dielectric layer on the surface of a TFT device comprised of 100 nm-particle BTO/PSX film. (d) 50 nm particle size BTO/PSX films. Figure 2a is reproduced from ref [12]. Copyright [2023] American Chemical Society.

can indicate a homogeneous distribution of BTO nanoparticles in the PSX polymer matrix.

The phase transition of two BTO nanoparticles with distinct sizes in response to a change in temperature was verified using variable temperature X-ray diffraction (VTXRD), as illustrated in Figure 3. ¹² Upon comparison of the peak changes at 2θ =

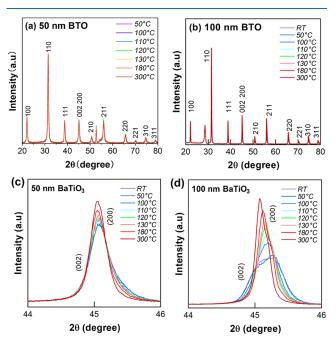


Figure 3. Differences in phase transition temperatures for (a) wide range of 50 nm BTO, (b) wide range of 100 nm BTO, (c) 44–46 degree of 50 nm BTO, and (d) 44–46 degree of 100 nm BTO. Figure b, d is reproduced from ref [12]. Copyright [2023] American Chemical Society.

 45° position for both samples as they rose from room temperature to 300 °C, it becomes evident that all experimental samples underwent a phase transition due to the increase in temperature.

At low temperatures, BTO exhibits a tetragonal crystal structure characterized by a noncentrosymmetric net displacement of ${\rm Ti}^{4+}$ along the c-axis. BTO exists in a ferroelectric phase characterized by spontaneous polarization. The peaks of intensity on (002) and (200) planes are visible in the XRD

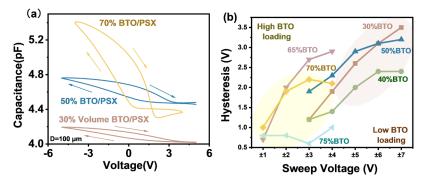


Figure 4. (a) Hysteresis loops were observed across various concentrations of BTO loading. (b) Impact of BTO loading concentration and scanning voltage on the dimensions of the hysteresis window.

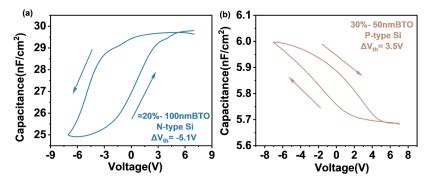


Figure 5. C-V measurement of two BTO/PSX films loaded with comparable amounts of BTO: (a) 100 nm particle size BTO and (b) 50 nm particle size BTO.

pattern 2θ of the 45° position. When the temperature exceeds the Curie temperature, the relative displacement of Ti⁴⁺ disappears and the crystal structure changes to a centrosymmetric cubic structure. At this time, BTO has a paraelectric phase and does not exhibit spontaneous polarization. Because Ti⁴⁺ returns to the center position, only the (002) plane intensity peaks at 2θ of the 45° position in the XRD pattern can be observed.

As the VTXRD results show, the intensity peak at 2θ of the 45° position in the 100 nm BTO sample gradually becomes sharp as the temperature is increased from room temperature to 300 °C. This means that BTO nanoparticles complete the transition from the ferroelectric phase (tetragonal) to the paraelectric phase (cubic) during the temperature increase. Although this transition process was also found in the 50 nm BTO sample, the modulation of the peak at the $2\theta=45^{\circ}$ position is comparatively less sensitive to temperature changes. We anticipate that the 50 nm particle size BTO will demonstrate a reduced polarization intensity.

A clockwise hysteresis phenomenon was initially observed in films loaded with a 70% BTO (volume ratio of the sample) loading ratio, as illustrated in Figure 4a, by measuring the C–V output curves of the MOS devices. Following this, analogous hysteresis loops were observed in samples containing varying BTO loading ratios. In addition to providing a summary of the data for each sample, it is determined that, macroscopically, a higher BTO loading ratio will cause films to break down easily and to enlarge the hysteresis window at the same scanning voltage. Additionally, an increase in scanning voltage will result in an increased hysteresis window at the same BTO loading ratio, as shown in Figure 4b.

When comparing the C-V output curves of different nanoparticle size samples with similar BTO loading ratios, it

is found that the 50 nm size BTO/PSX film exhibits a low maximum capacitance of 6 nF/cm², which is much smaller than 29.7 nF/cm² for 100 nm size BTO/PSX film. in addition, the 50 nm BTO/PSX films exhibited smaller hysteresis loops, with ΔV_{th} of 3.5 V that is lower than the ΔV_{th} of -5.1 V observed in the 100 nm BTO/PSX films, as shown in Figure 5Figure 5. The dielectric constant and dielectric loss in core—shell-structured ferroelectric materials increase as the film thickness increases. An ideal grain distribution is observed at a film thickness of approximately 450 nm, 13 which enhances the capacitance value. However, in this study, the 50 nm BTO/PSX film shows smaller capacitance as well as a narrower hysteresis window compared to the 100 nm BTO/PSX film, as shown in Figure 5a,b.

Meanwhile, in order to confirm that the hysteresis behavior observed in the C–V measurement is indeed due to ferroelectricity, we also constructed a Sawyer–Tower circuit to perform the P–E measurement, as shown in Figure 6. The polarization intensity of the film increases as the electric field strength increases, while the width of the hysteresis window remains relatively constant, as shown in Figure 7. Compared to the polarization intensity of 100 nm BTO nanoparticles around 1.2 μ C/cm² measured in the prior research, ¹² 50 nm BTO nanoparticles exhibited a smaller polarization intensity of 0.03 μ C/cm² with a narrower hysteresis window.

Afterwards, both 100 and 50 nm samples were used as dielectric layers in TFT devices with a top-gate structure. Counterclockwise hysteresis curves were observed in the transfer characteristics while showing clear hysteresis window sizes, as shown in Figure 8. The leakage currents were in the ranges of 10^{-10} A/ μ m in the 100 nm sample and 10^{-12} A/ μ m in the 50 nm size sample. Thus, the leakage currents of the TFT devices were decreased by 2 orders of magnitude with the

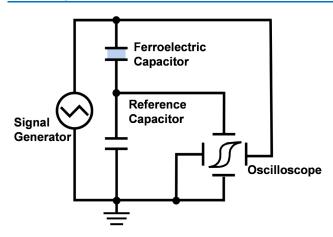


Figure 6. Schematic of the Sawyer–Tower circuit used to perform P–E measurements.

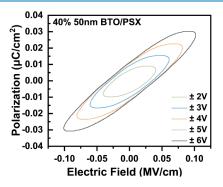


Figure 7. P-E measurement of 50 nm BTO/PSX film.

improvement of the dielectric layer film quality in 50 nm BTO/PSX.

It is noteworthy that while the polarization intensity of the 50 nm particle size BTO is comparatively weaker than that of the 100 nm particle size BTO and the thickness of the 50 nm BTO/PSX nanocomposite film surpasses 500 nm, the 50 nm BTO demonstrates superior electrical properties (such as faster switching and higher operating current) and a TFT hysteresis window comparable to that of 100 nm BTO. It is valuable to investigate the factors contributing to this mechanism.

The size reduction of BTO nanoparticles introduces challenges in achieving optimal storage performance due to size effects and increased domain wall defect density. These factors lead to weakened polarization intensity, making the device's storage stability susceptible to even minor failures in

ferroelectric domains during polarization reversal. As a result, the hysteresis characteristics of the device can be significantly affected.

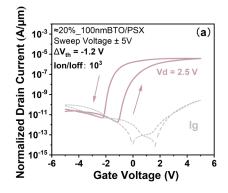
To address these issues and enhance storage stability, our future work will concentrate on two main aspects. First, we optimized the film preparation process to improve uniformity and reduce defects. Second, we plan to develop pretreatment methods for BTO nanoparticles to ensure their more uniform distribution within the PSX matrix, thereby reducing the domain wall defect density.

According to the outcomes of VTXRD, P–E, and MOS C–V measurements, the polarization intensity of the 50 nm particle size BTO is weaker than that of the 100 nm particle size BTO. There is a notable positive correlation between the polarization intensity and grain size of ferroelectric materials. This relationship becomes especially substantial when the grain size approaches the nanometer level. The comparatively diminished polarization intensity observed in 50 nm particle size BTO is believed to be primarily attributable to the grain boundary effect, wherein the number of grain boundaries within the crystal increases substantially with decreasing grain size.

Due to its intricate atomic structure, the grain boundary region contains more defect states. An increase in the quantity of grain boundaries disrupts the arrangement of electric dipoles within the grain, thereby impeding the formation of a structured polarization structure. On the other hand, an untidy electric field is more prone to induce stochastic movement among local electric dipoles at the grain surface, resulting in a reduction in the overall polarization response strength.

Simultaneously, the polarization intensity is influenced by the inhibition of the phase transition in a core—shell structure caused by smaller grain sizes. The large difference in particle radius between Ba²⁺ and Ti⁴⁺ in BTO crystals leads to the movement and aberration of cations, resulting in different low-symmetric structures (ortho-rhombic and monoclinic phases) and coexistence with high-symmetric phases (cubic and tetragonal phases), forming the core—shell phenomenon.

However, the core—shell structure requires a sufficiently large grain space to establish long-range ordered polarization and structure, which inhibits the phase transition of the core—shell structure when the nanocrystal grain space is limited. A portion of the crystals are unable to maintain the tetragonal structure turning into a centrosymmetric cubic structure, so the ferroelectricity is lost, leading to a weakening



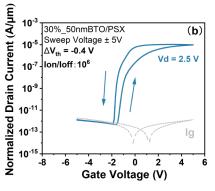


Figure 8. Comparison of TFT transfer characteristics between (a) 50 and (b) 100 nm BTO particles at 2.5 V.

of the overall polarization strength in smaller particle size BTO.

Nevertheless, the substantial hysteresis window observed in the TFT devices during the production of 50 nm particle size BTO can be attributed primarily to the higher BTO loading concentration, as demonstrated by STEM cross-sectional images of samples in both devices, as shown in Figure 9a ,b.

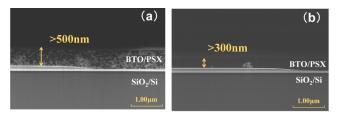


Figure 9. STEM cross section of (a) 50 nm particle-size BTO/PSX films and (b) 100 nm particle-size BTO/PSX films.

From the STEM cross-sectional image of the 50 nm BTO/PSX film in Figure 9a, two issues can be observed regarding the distribution of 50 nm BTO nanoparticles in PSX: (1) The distribution of nanoparticles is not uniform enough. (2) Local agglomeration of nanoparticles still exists in some regions. To address the issue of nonuniform distribution of BTO nanoparticles in PSX, surface modification of BTO nanoparticles using silane coupling agents can be considered. This approach may help to improve the dispersibility of BTO in PSX, ultimately achieving a more uniform distribution of BTO nanoparticles within the PSX matrix. Regarding the agglomeration of BTO nanoparticles, increasing the frequency and duration of the ultrasonic treatment can be considered. This measure can help overcome the van der Waals forces between particles and break up the agglomerates.

In future studies, we plan to explore the feasibility of these improvement strategies to obtain BTO/PSX composite films with a more uniform distribution and lower degree of agglomeration, enhancing their dielectric properties and energy storage density. Further experimental work and characterization will help to validate the effectiveness of these approaches.

As a perovskite structure material, BTO remains in a tetragonal structure at room temperature with a net displacement of Ti^{4+} on the *c*-axis, and changes to a cubic structure as the temperature increases to about 120 °C, where Ti^{4+} returns to the center of the structure and the net displacement disappears. In the tetragonal structure, it leads to the existence

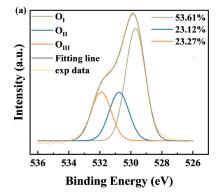
of crystal planes (200) and (002), whereas in the cubic structure the two planes coincide.

Performing fast Fourier transform (FFT) on the STEM image to obtain the crystal spacing information on the 50 nm BTO sample, as shown in Figure S2a we can find two sets of mutually perpendicular diffraction spots. Inverse FFT (IFFT) was performed on these diffraction spots to obtain the interplanar spacing of the respective crystalline surfaces, as shown in Figure S2b,c. By comparing the spacing between crystal planes (002) and (200) in the IFFT by XRD card of tetragonal BaTiO₃(COD 96-150-7757),¹⁹ it was confirmed that the tetragonal structure exists in the 50 nm BTO sample.

Furthermore, despite the increased film thickness, which reduced the capacitance of the 50 nm BTO/PSX films, the higher BTO loading ratio remains advantageous in enhancing the electrical performance of the TFT devices. A novel PSX ratio was implemented in the preparation of BTO/PSX films for this investigation, the molecular formula of PSX is shown in Figure S3. Compared to the PSX of MePhQ504010 which was used in the prior experiment, 12 the increased proportions of methyl and silica functional groups in MeQ7030 are helpful for the PSX polycondensation reaction to be more efficient at a lower temperature, thereby facilitating the curing of BTO/PSX films. Simultaneously, the liberated H⁺ and OH⁻ are advantageous during the polycondensation reaction, as shown in Figure S4, because these passivate the oxygen vacancies in the channel layer, thereby decreasing oxygen vacancy defects.20

Consequently, employing an X-ray photoelectron spectroscopy (XPS) depth profile experiment, we assessed the oxygen elemental characterization of the experimental samples. We compared the photoelectron peaks of elemental oxygen (O 1s) at IGZO bulk, as shown in Figure 11 (see Figure S5 for the sample structure and location of the XPS measurements; Figure S6a,b for the XPS measurements at the BTO/PSX layer; and Figure S6c,d for XPS measurements at the interface between BTO/PSX and IGZO layers). As a result, we can observe four subpeaks under the main peak of element O, namely O_I(metal-O), O_{II} (nonstoichiometric metal oxide), $O_{III}(O-H)$, and $O_{IV}(Si-O)$. The proportion of the XPS spectra of the o 1s attributed to O_{II} in the IGZO bulk is 28.13% for the IGZO-only film (without BTO/PSX), as shown in Figure 10. While it is 29.91% of $O_{\rm II}$ and a mere 23.12% at the IGZO bulk when employing MePhQ504010 and MeQ7030 BTO/PSX films, respectively.

In addition, we also compared the intensity of the $O_{III}(O-H)$ subpeaks at the interface as shown in Figure



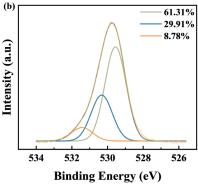


Figure 10. O 1s XPS spectra at different layers: (a) 50 nm BTO/PSX and (b) 100 nm BTO/PSX in the IGZO bulk.

S6c,d and the IGZO layer as shown in Figure 11 between MeQ7030 and MePhQ504010. In the MePhQ504010 sample,

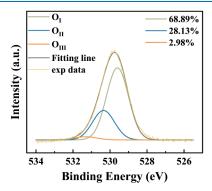


Figure 11. O 1s XPS spectra in only the IGZO layer in the IGZO bulk.

the intensity of the $O_{III}(O-H)$ subpeak at the interface is 43.23%, while the intensity at the IGZO layer decreases to 8.78%. In the MeQ7030 sample, the intensity of the $O_{III}(O-H)$ subpeak at the interface is 28.09%, and the intensity at the IGZO layer is 23.27%. In comparison, the subpeak intensity at the IGZO-only film (without BTO/PSX) is 2.97%. It can be found that the O_{III} (O-H) content of the MeQ7030 sample at the IGZO layer is much higher than that of the other two samples (MePhQ504010 and IGZO only). This occurrence indicates that MeQ7030 PSX can conduct a more extensive polycondensation reaction and release more hydrogen ions (H⁺) and hydroxides (OH⁻) upon being subjected to a 100 °C curing treatment.

Despite the inherent subjectivity and error associated with XPS detection, the presented data provides compelling evidence that PSX exhibits enhanced capability in reducing undercoordinated oxygen ions and oxygen vacancies in the TFT channel layer during low-temperature baking (100 °C) when the proportion of methyl and silica components is increased. By decreasing the oxygen vacancy defects, the electrical properties are also enhanced.

CONCLUSIONS

In this study, we fabricated ferroelectric films by using BTO nanoparticles with 50 nm diameter in combination with organic—inorganic material PSX, which has the following advantages over the traditional sol—gel preparation method: (1) The preparation process is simpler and there is no chemical reaction between the mixing of BTO and PSX. (2) The heat treatment temperature is lower since the polycondensation of PSX at 100 °C facilitates the formation of a dense film without losing the ferroelectric phase of BTO nanoparticles.

Both VTXRD and MOS C-V measurements revealed that the 50 nm BTO exhibited weaker polarization intensity than the 100 nm BTO. We attribute that the decrease in grain size leads to a grain boundary effect and inhibits the phase transition of core—shell structure which results in the reduction of the polarization intensity of BTO

In contrast to the 100 nm BTO particles used in previous studies, the 50 nm BTO nanoparticles exhibit superior dispersion inside the film, leading to enhanced uniformity and leakage current reduction in the BTO/PSX film. The TFT devices exhibited superior nonvolatile memory capability and

transfer characteristics when using the 50 nm BTO/PSX compared to 100 nm BTO/PSX. hence opening up new avenues for the advancement of FeFET computing in memory devices.

ASSOCIATED CONTENT

Solution Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsomega.4c03922.

SEM cross-sectional scanning of BTO/PSX film, SEM-EDXS measurement of BTO/PSX film, STEM of 50 nm BTO/PSX films: FFT spectrograms, interplanar spacing of (002) and (200) planes, the molecular formula for PSX, polycondensation reaction of PSX during heating curing process, film stack structure and positions of XPS measurements, and uniformity, leakage current, and break down voltage of different BTO/PSX films (PDF)

AUTHOR INFORMATION

Corresponding Author

Juan Paolo S. Bermundo — Division of Materials Science, Nara Science Institute of Technology, Ikoma, Nara 630-0192, Japan; orcid.org/0000-0002-9575-6112; Email: b-soria@ms.naist.jp

Authors

Chuanjun Wu — Division of Materials Science, Nara Science Institute of Technology, Ikoma, Nara 630-0192, Japan Aimi Syairah Safaruddin — Division of Materials Science,

Nara Science Institute of Technology, Ikoma, Nara 630-0192, Japan

Atsuko Yamamoto — Display Solutions Patterning Materials, Merck Electronics Ltd., Shizuoka 437-1412, Japan Yukiharu Uraoka — Division of Materials Science, Nara Science Institute of Technology, Ikoma, Nara 630-0192, Japan

Complete contact information is available at: https://pubs.acs.org/10.1021/acsomega.4c03922

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

The authors thank Merck Electronics Ltd. for supplying both the 50 nm BTO dispersion and the PSX solution utilized in this investigation. This study is partially supported by JSPS Kakenhi No. 22K14291.

REFERENCES

- (1) Or-Bach, Z.. A 1000× Improvement of the Processor-Memory Gap. In NANO-CHIPS 2030: on-Chip AI for an Efficient Data-Driven World, Murmann, B.; Hoefflinger, B., Eds.; Springer International Publishing: pp. 247267. 2020, .
- (2) Ishiwara, H. Ferroelectric Random Access Memories. *J. Nanosci. Nanotechnol.* **2012**, *12*, 7619–7627.
- (3) Long, Y.; Kim, D.; Lee, E.; Saha, P.; Mudassar, B. A.; She, X.; Khan, A. I.; Mukhopadhyay, S. A Ferroelectric FET-Based Processing-in-Memory Architecture for DNN Acceleration. *J. Magaz.* **2019**, 5 (2), 113–122.
- (4) Mutlu, O.; Subramanian, L. Research Problems and Opportunities in Memory Systems. *Supercomput. Frontiers Innovat.* **2014**, *1* (3), 19–55.

- (5) Cai, K.; Yang, M.; Ju, H.; Wang, S.; Ji, Y.; Li, B.; Edmonds, K. W.; Sheng, Y.; Zhang, B.; Zhang, N.; Liu, S.; Zheng, H.; Wang, K. Electric Field Control of Deterministic Current-Induced Magnetization Switching in a Hybrid Ferromagnetic/Ferroelectric Structure. *Nat. Mater.* **2017**, *16* (7), 712–716.
- (6) Xiong, Z.; Hu, C.; Luo, X.; Zhou, W.; Jiang, Z.; Yang, Y.; Yu, T.; Lei, W.; Yuan, C. Field-Free Improvement of Oxygen Evolution Reaction in Magnetic Two-Dimensional Heterostructures. *Nano Lett.* **2021**, *21* (24), 10486–10493.
- (7) Yang, M.; Deng, Y.; Wu, Z.; Cai, K.; Edmonds, K. W.; Li, Y.; Sheng, Y.; Wang, S.; Cui, Y.; Luo, J.; Ji, Y.; Zheng, H.-Z.; Wang, K. Spin Logic Devices via Electric Field Controlled Magnetization Reversal by Spin-Orbit Torque. *J. Magaz.* 2019, 40, 1554–1557.
- (8) Xu, Y. Ferroelectric Materials and Their Applications; Elsevier, 2013.
- (9) Kesorn, P.; Bermundo, J. P.; Nonaka, T.; Fujii, M. N.; Ishikawa, Y.; Uraoka, Y. High Performance Amorphous In—Ga—Zn—O Thin-Film Transistors with Low Temperature High-k Solution Processed Hybrid Gate Insulator. ECS J. Solid State Sci. Technol. 2020, 9 (2), 025002.
- (10) Choi, K. J.; Biegalski, M.; Li, Y. L.; Sharan, A.; Schubert, J.; Uecker, R.; Reiche, P.; Chen, Y. B.; Pan, X. Q.; Gopalan, V.; Chen, L.-Q.; Schlom, D. G.; Eom, C. B. Enhancement of Ferroelectricity in Strained BaTiO 3 Thin Films. *Science* **2004**, *306* (5698), 1005–1009.
- (11) Salaoru, I.; Paul, S. Non-Volatile Memory Device- Using a Blend of Polymer and Ferroelectric Nanoparticles. *Journal of Optoelectronics and Advanced Materials* **2008**, 10, 3461–3464.
- (12) Safaruddin, A. S.; Bermundo, J. P. S.; Wu, C.; Uenuma, M.; Yamamoto, A.; Kimura, M.; Uraoka, Y. High-k Solution-Processed Barium Titanate/Polysiloxane Nanocomposite for Low-Temperature Ferroelectric Thin-Film Transistors. ACS Omega 2023, 8 (33), 29939–29948.
- (13) Bi, J.; Shan, L.; Wu, Z.; Fu, X.; Hou, W. Dielectric Properties for Strontium Barium Titanate Thin Films with Different Thickness. *Ferroelectrics* **2018**, 529 (1), 113–119.
- (14) Spanier, J. E.; Kolpak, A. M.; Urban, J. J.; Grinberg, I.; Ouyang, L.; Yun, W. S.; Rappe, A. M.; Park, H. Ferroelectric Phase Transition in Individual Single-Crystalline BaTiO3 Nanowires. *Nano Lett.* **2006**, 6 (4), 735–739.
- (15) Gopalan, V.; Dierolf, V.; Scrymgeour, D. A. Defect–Domain Wall Interactions in Trigonal Ferroelectrics. *Annu. Rev. Mater. Res.* **2007**, *37* (1), 449–489.
- (16) Barrett, N.; Rault, J.; Krug, I.; Vilquin, B.; Niu, G.; Gautier, B.; Albertini, D.; Lecoeur, P.; Renault, O. Influence of the Ferroelectric Polarization on the Electronic Structure of BaTiO3 Thin Films. *Surf. Interface Anal.* **2010**, *42* (12–13), 1690–1694.
- (17) Morozovska, A. N.; Eliseev, E. A.; Glinchuk, M. D. Ferroelectricity Enhancement in Confined Nanorods: Direct Variational Method. *Phys. Rev. B* **2006**, 73 (21), 214106.
- (18) Morozovska, A. N.; Glinchuk, M. D.; Eliseev, E. A. Phase Transitions Induced by Confinement of Ferroic Nanoparticles. *Phys. Rev. B* **2007**, *76* (1), 014102.
- (19) Al-Shakarchi, E. K.; Mahmood, N. B. Three Techniques Used to Produce Fine Powder. *JMP* **2011**, *02* (11), 1420–1428.
- (20) Safaruddin, A. S.; Bermundo, J. P. S.; Yoshida, N.; Nonaka, T.; Fujii, M. N.; Ishikawa, Y.; Uraoka, Y. Highly Reliable Low-Temperature (180 °C) Solution-Processed Passivation for Amorphous In–Zn–O Thin-Film Transistors. *Appl. Phys. Express* **2019**, *12* (6), 064002.