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High-electron-mobility (370 cm^2/Vs) polycrystalline Ge on an insulator formed by As-doped solid-phase crystallization

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High-electron-mobility polycrystalline Ge (poly-Ge) thin films are difficult to form because of their poor crystallinity, defect-induced acceptors and low solid solubility of n-type dopants. Here, we found that As doping into amorphous Ge significantly influenced the subsequent solid-phase crystallization. Although excessive As doping degraded the crystallinity of the poly-Ge, the appropriate amount of As (~10^{20} cm^{-3}) promoted lateral growth and increased the Ge grain size to approximately 20 μm at a growth temperature of 375 °C. Moreover, neutral As atoms in poly-Ge reduced the trap-state density and energy barrier height of the grain boundaries. These properties reduced grain boundary scattering and allowed for an electron mobility of 370 cm^2/Vs at an electron concentration of 5×10^{18} cm^{-3} after post annealing at 500 °C. The electron mobility further exceeds that of any other n-type poly-Ge layers and even that of single-crystal Si wafers with $n \geq 10^{18}$ cm^{-3}. The low-temperature synthesis of high-mobility Ge on insulators will provide a pathway for the monolithic integration of high-performance Ge-CMOS onto Si-LSIs and flat-panel displays.

Ge is a unique and attractive material as it has a higher carrier mobility than Si for both electrons and holes and is compatible with conventional Si processing[1–6]. Therefore, Ge complementary metal-oxide-semiconductor (CMOS) is promising for scaling beyond the Si-CMOS limit. In the last decade, numerical efforts on the gate stack[4–8] and Ge-on-insulator (GOI) technologies[9–16] have made Ge MOS field-effect transistors (MOSFETs) superior to Si-MOSFETs for both p and n channels. Considering that the most promising use of Ge-CMOS is to integrate it into Si large-scale integrated circuits (LSIs) or flat-panel displays, the GOI should be formed at low temperature in a simple process. However, single-crystal GOI technology such as, mechanical transfer[1,10], oxidation-induced condensation[5,11] and rapid-melting growth[12–15] requires a single-crystal wafer or high temperature process (>900 °C).

Polycrystalline Ge (poly-Ge) thin films have been formed on insulators at low temperatures using solid-phase crystallization (SPC)[16–20], laser annealing[21–24], chemical vapor deposition[25,26], lamp annealing[27,28], seed layer technique[29] and metal-induced crystallization (MIC)[30–34]. The poly-Ge layers are naturally highly p-type because of their defect-induced acceptors[35]. Although the low solid solubility of n-type dopants in Ge made it difficult to produce n-type poly-Ge in a low thermal budget[36,37], some techniques including short-time annealing enabled n-type poly-Ge[18,24,38]. However, poly-Ge with high carrier mobility (>200 cm^2/Vs) was difficult for both p- and n-type because of grain boundary scattering or metal contamination. Therefore, the poly-Ge MOSFETs performed worse than single-crystal GOI-MOSFETs.

We achieved a Hall hole mobility of over 340 cm^2/Vs using SPC[39], which has many advantages over other methods, including no metal contamination, no melting-induced surface-ripples and a simple process. Using the SPC-Ge layer on a glass substrate, we demonstrated the best transistor operation among poly-Ge-MOSFETs without minimizing the channel region[40]. The formation of GeO_2 underlayer further improved the Hall hole mobility of poly-Ge to 620 cm^2/Vs[41], which greatly exceeds that of bulk-Si (430 cm^2/Vs). We also achieved n-type poly-Ge by the SPC of Sb-doped amorphous Ge (a-Ge)[42]. However, the electron mobility was limited to 210 cm^2/Vs by the neutral Sb scattering because of the low solid solubility of Sb in Ge. In this study, we examined As as a

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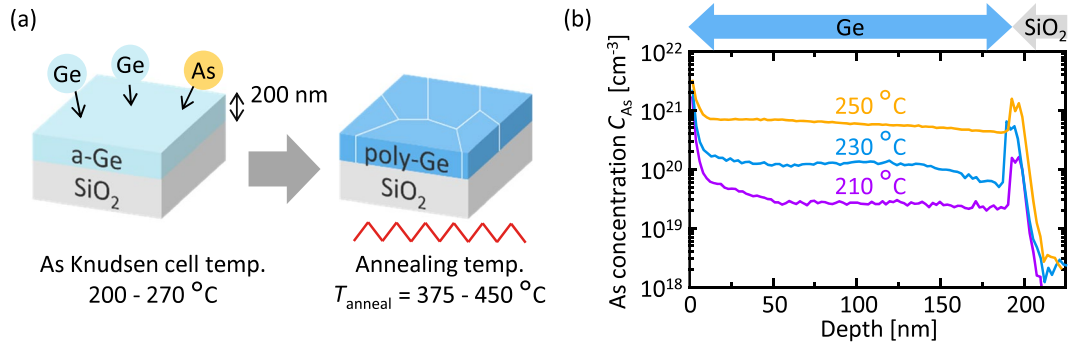

Figure 1. Experimental procedure of SPC of As-doped a-Ge layers. (**a**) Schematic of the sample preparation. (**b**) Representative SIMS depth profiles for the samples with an As Knudsen cell temperature of 210, 230, and 250 °C.

dopant because it has a higher solid solubility in Ge than Sb[36,37]. The As doping in a-Ge significantly changed the subsequent SPC characteristics, including crystallization rate, grain size and electrical properties. By controlling the As amount and SPC conditions, the highest electron mobility among n-type poly-Ge is achieved.

Experimental

As schematically shown in Fig. 1(a), As-doped a-Ge layers were deposited on SiO_2 glass substrates at RT using a Knudsen cell of a molecular beam deposition system (base pressure: 1×10^{-7} Pa). The Ge thickness was 200 nm and the Ge deposition rate was fixed at 1.7 nm/min. The temperature of the As Knudsen cell ranged from 200 to 270 °C to modulate the As concentration C_{As} in Ge. As representatively shown in Fig. 1(b), secondary ion mass spectrometry (SIMS) identified the As concentrations as 1.0×10^{19}, 2.8×10^{19}, 6.2×10^{19}, 1.2×10^{20}, 2.8×10^{20}, 5.9×10^{20}, 1.0×10^{21} and 1.8×10^{21} cm^{-3} at a depth of 100 nm when the As Knudsen cell temperature was 200, 210, 220, 230, 240, 250, 260 and 270 °C, respectively. The samples were then loaded into a conventional tube furnace under a N_2 (99.9%) atmosphere and annealed at a temperature T_{anneal} of 375–450 °C to induce SPC. We performed post annealing (PA) at 500 °C for 5 h on all samples. According to the SIMS measurements, C_{As} remained constant before and after annealing.

Results and Discussion

We examined the C_{As} dependence of the crystal quality of Ge using Raman spectroscopy (JASCO NRS-5100, spot diameter 20 μm, wavelength 532 nm). The samples with $T_{anneal} = 450$ °C exhibit sharp peaks near 300 cm^{-1}, which correspond to crystalline (c-) Ge-Ge bonding in the whole C_{As} range (Fig. 2(a)). As shown in Fig. 2(b), annealing at 375 °C for 150 h crystallized the samples with $C_{As} \leq 2.8 \times 10^{20}$ cm^{-3}, but not those with $C_{As} > 2.8 \times 10^{20}$ cm^{-3}. These results mean that excessive As lowers the crystallization rate. To analyze the Raman shift and the full width at half maximum (FWHM) of crystalline Ge (c-Ge) peaks, each spectrum was fitted as representatively shown in Fig. 2(c). The peak is fitted well enough to correctly calculate the FWHM and peak position. The Raman shift and FWHM results are summarized in Fig. 2(d). All peaks shifted to lower wavenumbers than that of a single-crystal bulk-Ge substrate, originating from the tensile strain. The peak shifts are almost constant with respect to C_{As} while the peaks for $T_{anneal} = 450$ °C shifted to the lower wavenumber than that for $T_{anneal} = 375$ °C. The Raman shift had small variation (<0.5%), and therefore, seems to be the dominant difference with respect to the annealing temperature. This behavior suggests that the strain likely originates from the difference in the thermal expansion coefficients between Ge and the SiO_2 substrate. The FWHM is almost constant for $C_{As} \leq 5.9 \times 10^{20}$ cm^{-3} and significantly increases for $C_{As} > 5.9 \times 10^{20}$ cm^{-3}. This indicates that excessive As negatively influences SPC-Ge crystallinity, as will become clear in the later-mentioned electron backscattering diffraction analyses. Thus, the Raman studies revealed that C_{As} strongly influences the growth rate and crystal quality of SPC-Ge.

The C_{As} dependence of the growth rate was evaluated using *in situ* optical microscopy during annealing. Figure 3(a) shows the typical growth evolution of SPC. Here we chose $T_{anneal} = 400$ °C because it allowed for both domain visibility and practical observation time in a wide range of C_{As}. The micrographs indicate that Ge nucleation occurs and the domain grows laterally with increasing annealing time. Eventually, the entire surface is covered with c-Ge for each sample, indicating that the SPC (lateral growth of domains) is saturated. The domain growth rate and saturated domain size vary significantly with C_{As} (Fig. 3(b)). The medium C_{As} sample ($C_{As} = 1.2 \times 10^{20}$ cm^{-3}) exhibited the highest growth rate and the largest domain size among the three samples. Generally, impurity doping promotes semiconductor atom migration and enhances the recrystallization rate of amorphous films[43]. Conversely, excessive As reduces both nucleation and lateral growth rates (Fig. 3(b)). This is likely because segregation of excessive As suppressed nucleation and growth. These behaviors have also been reported in Sn- and Sb-doped SPC-Ge[42,44,45]. Therefore, As doping in a-Ge greatly influences nucleation and lateral growth in subsequent SPC.

The inverse pole figures (IPFs) with grain boundaries in Ge were obtained using electron backscattering diffraction analyses (JEOL JSM-7001F with the TSL OIM analysis attachment). The grain size dramatically varies with C_{As} (Fig. 4(a–d)). The average grain size increases with increasing C_{As} and then begins to decrease (Fig. 4(e)). This behavior agrees with that of the eventual domain size in optical micrographs (Fig. 3). Additionally, the grain size is significantly degraded by excessive As ($C_{As} = 1.8 \times 10^{21}$ cm^{-3}). This behavior well accounts for the results

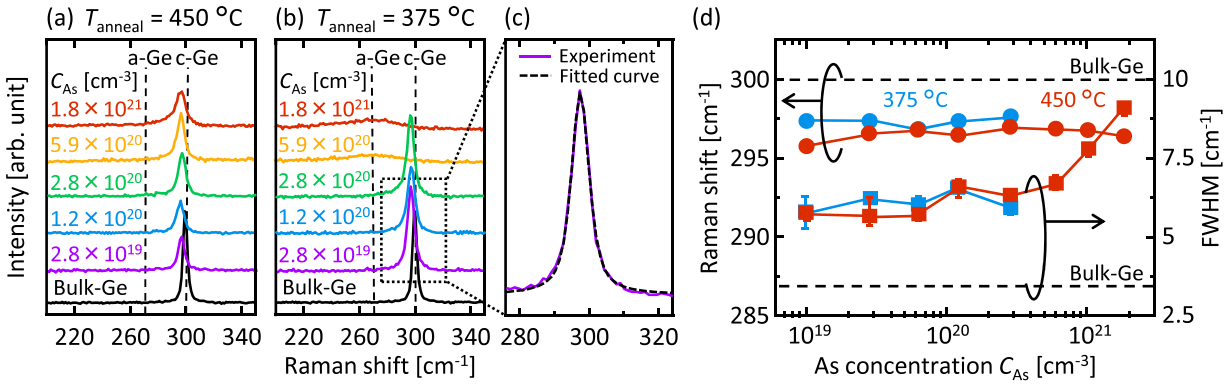

Figure 2. Raman spectroscopy study of the As-doped SPC-Ge layers. (**a**,**b**) Raman spectra of the samples with $C_{As} = 2.8 \times 10^{19}$, 1.2×10^{20}, 2.8×10^{20}, 5.9×10^{20} and 1.8×10^{21} cm^{-3} annealed at (**a**) 450 °C for 5 h and (**b**) 375 °C for 150 h. The spectra for a bulk-Ge wafer are shown for comparison. (**c**) Fitting result of a Raman spectrum. (**d**) Raman shifts and FWHMs of the c-Ge peaks for samples with $T_{anneal} = 375$ °C and 450 °C as a function of C_{As}, where the values were averaged over three measurements for each sample. The data for a bulk-Ge wafer are shown by the dotted lines.

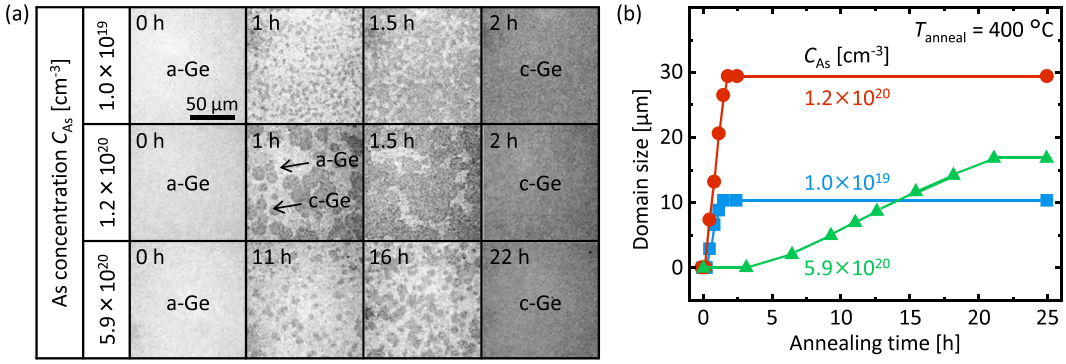

Figure 3. Characteristics of the growth rate of As-doped ($C_{As} = 1.0 \times 10^{19}$, 1.2×10^{20} and 5.9×10^{20} cm^{-3}) SPC-Ge. (**a**) *In situ* optical microscopy observation. The light-colored area indicates a-Ge and the dark-colored area indicates c-Ge. (**b**) Annealing time dependence of the domain size derived from a typical domain in the micrographs for each C_{As}. Here $T_{anneal} = 400$ °C.

of the Raman FWHM (Fig. 2(d)). The lower T_g provides a larger grain size, which agrees with the general tendency of SPC-Ge reflecting the reduction of nucleation frequency[17,39]. The sample with $C_{As} = 1.2 \times 10^{20}$ cm^{-3} and $T_g = 375$ °C exhibited a grain size of approximately 20 μm, which is the largest among poly-Ge formed by SPC.

The electrical properties of the As-doped SPC-Ge layers were evaluated using Hall-effect measurements with the van der Pauw method (Bio-Rad HL5500PC). All samples showed n-type conduction owing to the self-organizing activation of As during SPC. Electron concentration n and electron mobility μ_n depend on both T_{anneal} and C_{As} (Fig. 5(a,b)). We note that the maximum variation between samples prepared under the same conditions is approximately 20% in n and 5% in μ_n, while the measurement variation was smaller than the marks in the figures for each sample. We first discuss the T_{anneal} dependence of the electrical properties. Before PA, n for $T_{anneal} = 450$ °C is higher than that for $T_g = 375$ °C in the whole C_{As} range (Fig. 5(a)). This behavior is consistent with the fact that higher temperatures cause higher solid solubility and activation of As in Ge[36]. $T_{anneal} = 450$ °C exhibits a higher μ_n than $T_{anneal} = 375$ °C (Fig. 5(b)), whereas the grain size shows the opposite trend (Fig. 4(e)). According to the carrier conduction model proposed by Seto for polycrystalline semiconductors[46], the energy barrier of the grain boundary E_B decreases as the carrier density increases. The T_{anneal} dependence of μ_n is likely attributed to the fact that $T_{anneal} = 450$ °C has higher n and therefore lower E_B than $T_{anneal} = 375$ °C. After PA at 500 °C, n for $T_{anneal} = 450$ and 375 °C increases to a similar value for each C_{As} (Fig. 5(a)). These results suggest that the activation rate of As in Ge is determined by the maximum process temperature. μ_n is improved by PA for both T_{anneal} (Fig. 5(b)). In particular, μ_n for $T_{anneal} = 375$ °C is higher than that of $T_{anneal} = 450$ °C, which reflects the grain size (Fig. 4(e)). After PA, both n and μ_n are maximized at around $C_{As} = 1.2 \times 10^{20}$ cm^{-3} where the grain size is maximum (Fig. 4(e)). The C_{As} dependence of n is likely because the larger grain size provides the lower defect-induced acceptors and/or the less As segregation at grain boundaries. Although the C_{As} dependence of μ_n is consistent with the tendency of grain size, the dramatic improvement of μ_n from $C_{As} = 1.0 \times 10^{19}$ cm^{-3} to $C_{As} = 1.2 \times 10^{20}$ cm^{-3} is difficult to explain only in terms of grain size.

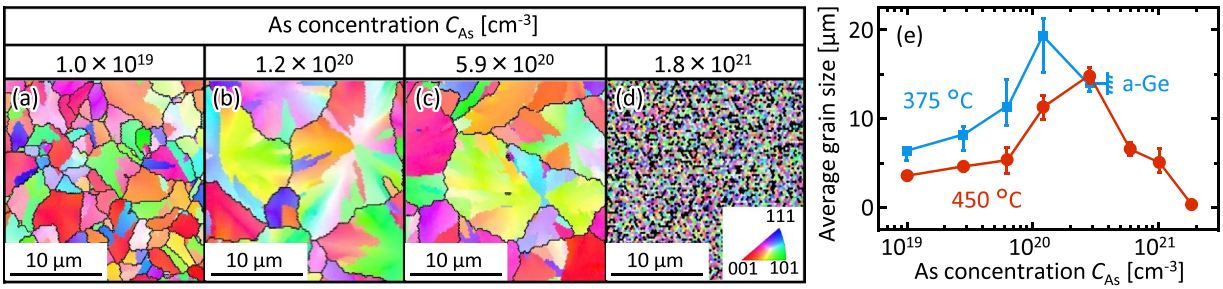

Figure 4. Grain size of the As-doped SPC-Ge layers. (**a**–**d**) IPF images of the samples annealed at 450 °C with C_{As} = (**a**) 1.0 × 10^{19}, (**b**) 1.2 × 10^{20}, (**c**) 5.9 × 10^{20} and (**d**) 1.8 × 10^{21} cm^{-3}. (**e**) Average grain size determined by the IPF analyses for samples with T_{anneal} = 375 °C and 450 °C as a function of C_{As}. For each sample, three IPF images were taken and averaged.

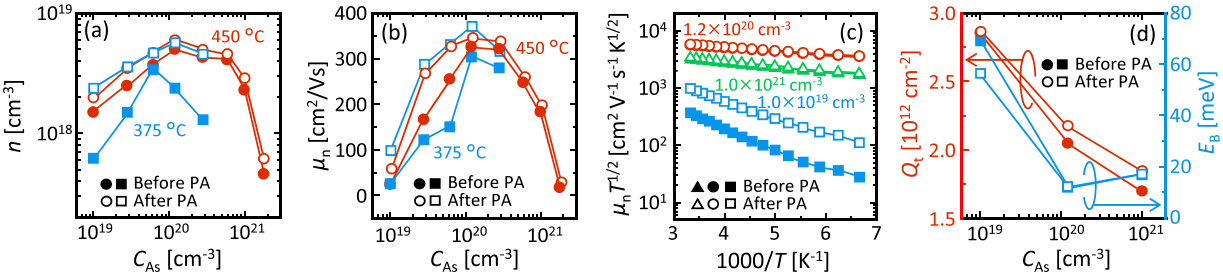

Figure 5. Electrical properties of the As-doped SPC-Ge layers. (**a**) Electron concentration n and (**b**) electron mobility μ_n for T_{anneal} = 375 °C and 450 °C before and after PA (500 °C) as a function of C_{As}. (**c**) Arrhenius plot of $\mu_n T^{1/2}$ for samples with C_{As} = 1.0 × 10^{19}, 1.2 × 10^{20} and 1.0 × 10^{21} cm^{-3} for T_{anneal} = 450 °C before and after PA. (**d**) Trap-state density Q_t and energy barrier height E_B of the Ge grain boundary as a function of C_{As}. Here n and μ_n were averaged over five measurements for each sample, where the variation was smaller than the marks.

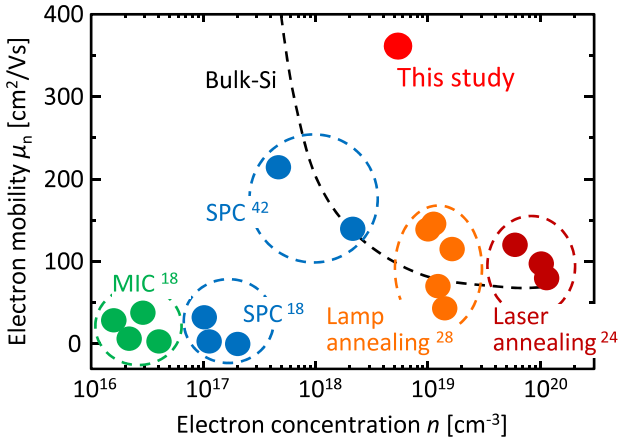

Figure 6. Comparison of the electron mobility μ_n and electron concentration n of n-type poly-Ge layers formed on insulators. The growth method and the reference number are shown near each symbol. The data for single-crystal bulk Si is shown by the dotted line.

To clarify the behavior, we quantified the trap-state density Q_t in the grain boundaries and E_B using the following equations[46]:

$$\mu_n T^{1/2} = \frac{Lq}{\sqrt{2\pi m_* k}} \exp\left(-\frac{E_B}{kT}\right), \quad (1)$$

$$Q_t = \frac{\sqrt{8\varepsilon n E_B}}{q}, \tag{2}$$

where T is the absolute temperature, L is the grain size, q is the elementary charge, m^* is the effective mass, k is the Boltzmann constant and ε is the dielectric permittivity. The Arrhenius plot of $\mu_n T^{1/2}$ makes an almost-downward-sloping straight line for the whole C_{As} region (Fig. 5(c)). Q_t decreases with increasing C_{As}, which suggests that As atoms passivate the grain boundary traps (Fig. 5(d)). Therefore, E_B dramatically decreases by As doping at $C_{As} = 1.2 \times 10^{20}\,cm^{-3}$, which reflects both the decrease of Q_t and increase of n. On the other hand, Q_t slightly increases with PA. This behavior is likely because PA increases lattice substitutional As and therefore reduces the extent to which As passivates the grain boundary. After PA, E_B for $C_{As} = 1.2 \times 10^{20}\,cm^{-3}$ does not change, which reflects the balance between Q_t and n, while μ_n improves slightly (Fig. 5(b)). Considering that PA improves the activation rate of As, the μ_n improvement is likely due to the decrease of carrier scattering by neutral As. The n and μ_n values reached $5 \times 10^{18}\,cm^{-3}$ and $370\,cm^2/Vs$, respectively. The μ_n value further exceeds that of any other n-type poly-Ge layers formed on insulators and even that of single-crystal Si wafers with $n \geq 10^{18}\,cm^{-3}$ (Fig. 6).

Conclusions

As doping into a-Ge significantly influenced the subsequent SPC. Although excessive As doping degraded the crystallinity of poly-Ge, the appropriate amount of As ($\sim 10^{20}\,cm^{-3}$) promoted the SPC and increased the Ge grain size. By combining slow annealing at low temperature (375 °C), the grain size reached approximately 20 μm, which is the largest among SPC-Ge. Moreover, neutral As atoms in Ge reduced Q_t ($2 \times 10^{12}\,cm^{-2}$) and E_B (12 meV). These properties reduced grain boundary scattering and allowed for μ_n of $370\,cm^2/Vs$, which is the highest among n-type poly-Ge formed on insulators. These findings will provide a means for the monolithic integration of high-performance Ge-CMOS onto Si-LSIs and flat-panel displays.

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References

1. Taraschi, G., Pitera, A. J. & Fitzgerald, E. A. Strained Si, SiGe, and Ge on-insulator: review of wafer bonding fabrication techniques. *Solid. State. Electron.* **48**, 1297–1305 (2004).
2. Nayfeh, A., Chui, C. O., Yonehara, T. & Saraswat, K. C. Fabrication of high-quality p-MOSFET in Ge Grown heteroepitaxially on Si. *IEEE Electron Device Lett.* **26**, 311–313 (2005).
3. Brunco, D. P. *et al*. Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance. *J. Electrochem. Soc.* **155**, H552 (2008).
4. Pillarisetty, R. Academic and industry research progress in germanium nanodevices. *Nature* **479**, 324–328 (2011).
5. Takagi, S. *et al*. III–V/Ge channel MOS device technologies in nano CMOS era. *Jpn. J. Appl. Phys.* **54**, 06FA01 (2015).
6. Toriumi, A. & Nishimura, T. Germanium CMOS potential from material and process perspectives: Be more positive about germanium. *Jpn. J. Appl. Phys.* **57**, 010101 (2018).
7. Zhang, R., Iwasaki, T., Taoka, N., Takenaka, M. & Takagi, S. High-Mobility Ge pMOSFET With 1-nm EOT Al_2O_3/GeO_x/Ge Gate Stack Fabricated by Plasma Post Oxidation. *IEEE Trans. Electron Devices* **59**, 335–341 (2012).
8. Yamamoto, K., Sada, T., Wang, D. & Nakashima, H. Dramatic enhancement of low electric-field hole mobility in metal source/drain Ge p-channel metal-oxide-semiconductor field-effect transistors by introduction of Al and Hf into SiO_2/GeO_2 gate stack. *Appl. Phys. Lett.* **103**, 122106 (2013).
9. Mizubayashi, W. *et al*. Impacts of plasma-induced damage due to UV light irradiation during etching on Ge fin fabrication and device performance of Ge fin field-effect transistors. *Appl. Phys. Express* **10**, 026501 (2017).
10. Yu, K. *et al*. Fabrication of high-hole-mobility germanium-on-insulator wafers through an easy method. *J. Alloys Compd.* **750**, 182–188 (2018).
11. Jo, K.-W., Kim, W.-K., Takenaka, M. & Takagi, S. Impact of SiGe layer thickness in starting substrates on strained Ge-on-insulator pMOSFETs fabricated by Ge condensation method. *Appl. Phys. Lett.* **114**, 062101 (2019).
12. Feng, J. *et al*. High-performance gate-all-around GeOI p-MOSFETs fabricated by rapid melt growth using plasma nitridation and ALD Al2O3 gate dielectric and self-aligned NiGe contacts. *IEEE Electron Device Lett.* **29**, 805–807 (2008).
13. Hu, S., Leu, P. W., Marshall, A. F. & McIntyre, P. C. Single-crystal germanium layers grown on silicon by nanowire seeding. *Nat. Nanotechnol.* **4**, 649–53 (2009).
14. Toko, K., Ohta, Y., Tanaka, T., Sadoh, T. & Miyao, M. Chip-size formation of high-mobility Ge strips on SiN films by cooling rate controlled rapid-melting growth. *Appl. Phys. Lett.* **99**, 032103 (2011).
15. Hosoi, T., Suzuki, Y., Shimura, T. & Watanabe, H. Mobility characterization of Ge-on-insulator metal-oxide-semiconductor field-effect transistors with striped Ge channels fabricated by lateral liquid-phase epitaxy. *Appl. Phys. Lett.* **105**, 173502 (2014).
16. Toko, K., Nakao, I., Sadoh, T., Noguchi, T. & Miyao, M. Electrical properties of poly-Ge on glass substrate grown by two-step solid-phase crystallization. *Solid. State. Electron.* **53**, 1159–1164 (2009).
17. Tsao, C.-Y., Huang, J., Hao, X., Campbell, P. & Green, M. A. Formation of heavily boron-doped hydrogenated polycrystalline germanium thin films by co-sputtering for developing p+ emitters of bottom cells. *Sol. Energy Mater. Sol. Cells* **95**, 981–985 (2011).
18. Jung, H.-W., Jung, W.-S., Yu, H.-Y. & Park, J.-H. Electrical properties of phosphorus-doped polycrystalline germanium formed by solid-phase and metal-induced crystallization. *J. Alloys Compd.* **561**, 231–233 (2013).
19. Sadoh, T., Kamizuru, H., Kenjo, A. & Miyao, M. Low-temperature formation (<500 °C) of poly-Ge thin-film transistor with NiGe Schottky source/drain. *Appl. Phys. Lett.* **89**, 192114 (2006).
20. Kabuyanagi, S., Nishimura, T., Nagashio, K. & Toriumi, A. Impacts of oxygen passivation on poly-crystalline germanium thin film transistor. *Thin Solid Films* **557**, 334–337 (2014).
21. Yeh, W., Chen, H., Huang, H., Hsiao, C. & Jeng, J. Superlateral growth of a-Ge film by excimer laser annealing. *Appl. Phys. Lett.* **93**, 94103 (2008).
22. Sakaike, K., Higashi, S., Murakami, H. & Miyazaki, S. Crystallization of amorphous Ge films induced by semiconductor diode laser annealing. *Thin Solid Films* **516**, 3595–3600 (2008).
23. Kasirajan, H. A. *et al*. CO_2 laser annealing of low-hole-concentration polycrystalline germanium for the fabrication of enhancement-mode nMOSFET. *Appl. Phys. Express* **11**, 101305 (2018).

24. Takahashi, K. *et al*. High n-type Sb dopant activation in Ge-rich poly-$Ge_{1-x}Sn_x$ layers on SiO_2 using pulsed laser annealing in flowing water. *Appl. Phys. Lett.* **112**, 062104 (2018).
25. Matsui, T., Kondo, M., Ogata, K., Ozawa, T. & Isomura, M. Influence of alloy composition on carrier transport and solar cell properties of hydrogenated microcrystalline silicon-germanium thin films. *Appl. Phys. Lett.* **89**, 142115 (2006).
26. Tada, M. *et al*. Low Temperature Germanium Growth on Silicon Oxide Using Boron Seed Layer and *In Situ* Dopant Activation. *J. Electrochem. Soc.* **157**, H371–H376 (2010).
27. Kamata, Y. *et al*. Operation of inverter and ring oscillator of ultrathin-body poly-Ge CMOS. *Appl. Phys. Express* **7**, 121302 (2014).
28. Koike, M., Usuda, K., Mori, T., Maeda, T. & Tezuka, T. Formation of n^+ Poly-Ge Films with High Electron Concentration and High Electron Mobility by Flash Lamp Annealing for Poly-Ge nMOSFETs. *Extended Abstracts of the 2015 International Conference on Solid State Devices and Materials* 1102–1103 (2015).
29. Asadirad, M. *et al*. High-Performance Flexible Thin-Film Transistors Based on Single-Crystal-Like Germanium on Glass. *Adv. Electron. Mater*. **2** (2016).
30. Wang, Z. M., Wang, J. Y., Jeurgens, L. P. H., Phillipp, F. & Mittemeijer, E. J. Origins of stress development during metal-induced crystallization and layer exchange: Annealing amorphous Ge/crystalline Al bilayers. *Acta Mater.* **56**, 5047–5057 (2008).
31. Hu, S., Marshall, A. F. & McIntyre, P. C. Interface-controlled layer exchange in metal-induced crystallization of germanium thin films. *Appl. Phys. Lett.* **97**, 82104 (2010).
32. Toko, K. *et al*. Low-temperature (180 °C) formation of large-grained Ge (111) thin film on insulator using accelerated metal-induced crystallization. *Appl. Phys. Lett.* **104**, 22106 (2014).
33. Park, J.-H., Kasahara, K., Hamaya, K., Miyao, M. & Sadoh, T. High carrier mobility in orientation-controlled large-grain ($\geq$50 μm) Ge directly formed on flexible plastic by nucleation-controlled gold-induced-crystallization. *Applied Physics Letters* **104**, 252110 (2014).
34. Higashi, H. *et al*. Electrical properties of pseudo-single-crystalline Ge films grown by Au-induced layer exchange crystallization at 250 °C. *J. Appl. Phys.* **123**, 215704 (2018).
35. Haesslein, H., Sielemann, R. & Zistl, C. Vacancies and Self-Interstitials in Germanium Observed by Perturbed Angular Correlation Spectroscopy. *Phys. Rev. Lett.* **80**, 2626–2629 (1998).
36. Trumbore, F. A. Solid Solubilities of Impurity Elements in Germanium and Silicon. *Bell Syst. Tech. J.* **39**, 205–233 (1960).
37. Koike, M. *et al*. Diffusion and activation of n-type dopants in germanium. *J. Appl. Phys.* **104**, 023523 (2008).
38. Prucnal, S. *et al*. Ultra-doped n-type germanium thin films for sensing in the mid-infrared. *Sci. Rep.* **6**, 27643 (2016).
39. Toko, K., Yoshimine, R., Moto, K. & Suemasu, T. High-hole mobility polycrystalline Ge on an insulator formed by controlling precursor atomic density for solid-phase crystallization. *Sci. Rep.* **7**, 16981 (2017).
40. Moto, K. *et al*. Polycrystalline thin-film transistors fabricated on high-mobility solid-phase-crystallized Ge on glass. *Appl. Phys. Lett.* **114**, 212107 (2019).
41. Imajo, T., Moto, K., Yoshimine, R., Suemasu, T. & Toko, K. High hole mobility ($\geq$500 $cm^2V^{-1}s^{-1}$) polycrystalline Ge films on GeO_2 -coated glass and plastic substrates. *Appl. Phys. Express* **12**, 015508 (2019).
42. Takahara, D., Moto, K., Imajo, T., Suemasu, T. & Toko, K. Sb-doped crystallization of densified precursor for n-type polycrystalline Ge on an insulator with high carrier mobility. *Appl. Phys. Lett.* **114**, 082105 (2019).
43. Miyao, M., Moniwa, M., Kusukawa, K. & Sinke, W. Low-temperature SOI (Si-on-insulator) formation by lateral solid-phase epitaxy. *J. Appl. Phys.* **64**, 3018–3023 (1988).
44. Sadoh, T., Kai, Y., Matsumura, R., Moto, K. & Miyao, M. High carrier mobility of Sn-doped polycrystalline-Ge films on insulators by thickness-dependent low-temperature solid-phase crystallization. *Appl. Phys. Lett.* **109**, 232106 (2016).
45. Moto, K., Yoshimine, R., Suemasu, T. & Toko, K. Improving carrier mobility of polycrystalline Ge by Sn doping. *Sci. Rep.* **8**, 14832 (2018).
46. Seto, J. W. Y. The electrical properties of polycrystalline silicon films. *J. Appl. Phys.* **46**, 5247–5254 (1975).

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Author contributions

K.T. conceived and designed the experiments. M.S., K.M. and T.N. conducted the experiments and analyses. K.T. and T.S. managed the research and supervised the project. All the authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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