Research article

# An efficient new design of nano-scale comparator circuits using quantum-dot technology

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A R T I C L E   I N F O

A B S T R A C T

Traditional semiconductor-based technology has recently faced many issues, such as physical scalability constraints and short-channel properties. Much research on nano-scale designs has resulted in these flaws. Quantum-dot Cellular Automata (*QCA*) is a promising nanotechnology solution for solving *CMOS*-related issues. The *4-dot* squared cell is identified as the main feature of this technology. Also, a comparator is an essential electronic device that compares *2 voltages* or currents. It is frequently employed to confirm whether an input has achieved a predefined value or not. So, the design of the QCA-based comparator is one of the interesting lines in recent studies. However, cell and area consumption limits the circuit design in the most relevant research. As a result, two efficient comparator circuits based on the inherent rules of quantum dots have been presented in this work. The proposed *1-bit* design employs *35* quantum cells in a *0.04* $\mu m^2$ compact layout space. Also, the proposed *2-bit* design uses *173* cells in a *0.19* μm2 compact layout area. These circuits, which are built across three layers of *90-degree* cells, remove the need for coplanar crossovers, ensuring accessible inputs and outputs. The presented *1-bit* comparator circuit uses *3* majority gates with three inputs. The first output signal in *1-bit* comparator is generated after *0.75 clock phases* and in *2-bit* design after *1.25 clock phases*. QCADesigner-E evaluated the suggested circuits' practical accuracy, cost, and power. The results showed that the proposed designs are extremely efficient in cell and area consumption compared to the state-of-the-art designs.

## 1. Introduction

Semiconductor fabrication technology has changed quickly in the last decades, but some applications require less power and more speed [1–3]. These problems motivate scientists to find an alternative technology as a solution [4–6]. Quantum-dot Cellular Automata (*QCA*) is one of the candidate technologies in this field [7]. It is a new nanotechnology that enables low power, high density, and a high-speed structure to design any digital function at a nano-scale [8]. QCA is a technique that can be used to create reliable computer systems in the future [9,10]. Lent et al. presented the first quantum dot model in the early *1990s*. No current conveys information from one cell to another using a polarization state, and all operations rely on quantum phenomena [11,12].

Unlike standard electronics, logic conditions are triggered by a cell rather than voltage levels, which is unique [13,14]. The machine will use a two-electron arrangement to process data. Manufacturing insufficiency and improper structure are essential factors in circuit quality. In QCA, information was sent via clocking technology [15,16]. Much research on QCA-based circuits has been done due to these characteristics [17,18]. Adders, multipliers, memories, multiplexers, and other digital circuits have been designed using this technique [19–23]. In CMOS technology, a comparator comprises a specialized high-gain differential amplifier. It has two input terminals and one binary digital output [24,25]. They're ubiquitous in devices like successive approximation *ADCs* and relaxation oscillators that measure and digitize analog signals [26,27]. Different components, including diodes, transistors, and opamps, can create such devices. They are used to drive logic circuits in various electrical devices. But, in QCA technology, a comparator circuit has 3 3-input majority gates, inverter gates, and cells. This paper presents a comparator circuit designed by QCA nanotechnology [28,29]. When two voltages are compared, a comparator circuit produces a *'1'*(*the voltage on the positive side; VDD in the example*) or a *'0'* (*the voltage on the negative side*) to indicate which is bigger [30,31]. Comparators are often employed to confirm if an input has reached the desired value or not. They play an essential role in digital circuits like microcontrollers in QCA technology [8,32]. As a result, high-performance comparator circuits have gotten much attention, and effort has gone into improving the performance of QCA comparator circuits. This research focuses on efficient multi-layer comparator circuit design using inverter and majority gates to form the foundation of the comparator design. Because of cell and area consumption restrictions in relevant research, the research presents an efficient QCA-based comparator design to solve these shortcomings. This design uses three layers of 90-degree cells in a *0.*04 μm² layout to eliminate coplanar crossovers and ensure accessible inputs and outputs. The three-layer arrangement and lack of coplanar crossovers are a novel approach to ensuring accessible inputs and outputs, which contributes to the design's overall efficiency. Furthermore, leveraging QCA's clocking technique for computational pipelining and signal flow management is new, as it allows the comparator to generate output across three clock phases. *QCADesigner-E* is used to assess practical accuracy, cost, and power, showing that the suggested design is substantially more efficient in terms of cell and area usage than earlier designs. The contributions of the current work are as follows:

- Reducing space consumption and the number of used cells of the comparator circuit;
- Reducing the energy and costs of the comparator circuit;
- Increasing speed and improving the accessibility to inputs and outputs of the comparator circuit.

Section 2 delivers related work on comparator circuits. Section 3 presents the proposed design. Section 4 assesses the performance of the comparator, and the conclusion is presented in the last section.

## 2. Related works

Researchers offered a design for a *1-bit* comparator as well as an innovative design for *2-bit,* and *3-bit* comparators in Ref. [33]. The circuit was built as a multi-layer QCA comparator with an area of *0.*06 μm² and *73* cells. In terms of both size and complexity, the *1-bit* comparator design outperforms earlier designs. The suggested designs' functionality was tested using the QCADesigner program.

Also, in Ref. [34], an optimized *1-bit* comparator architecture based on QCA was proposed. Also, a revolutionary *2-bit* comparator structure was subsequently proposed. The QCADesigner was used to test the simulation and operation of suggested comparators. A comparison with previous designs revealed that the proposed designs are compact and consistent in their performance. The *1-bit and 2-bit* QCA-based comparators have a clock phase latency of *0.75 and 2.75*, respectively, an active area of *0.*04 and *0.*19 μm², and utilize *31* and *125 cells*. However, these circuits cannot easily access output and input cells.

The authors in Ref. [35] proposed a QCA-based cascading serial bit stream comparator with majority and inverter gates. The suggested solution performs better regarding the number of gates and clock phases. Compared to the typical design, the result revealed that *28 %* of the area is attained. Furthermore, cascading requires fewer gates to compare the two n-bit integers.

Also, in Ref. [36], researchers presented a QCA-based *XNOR* gate, and the circuit's dependability and average energy dissipation were investigated. *Multi-bit* comparators were developed using the suggested *XNOR* gate, which has lower complexity than earlier ones. Finally, the simulation results using *QCADesigner* are provided, confirming the circuit's accurate operation.

Researchers used the suggested gate in Ref. [14] to create a 1-bit comparator circuit that requires a multi-layer structure with an area of *0.*04 μm² and *54* cells to construct. Using the QCADesigner program, they confirmed the functioning of the suggested designs, and the simulation results showed the correct circuit operation.

Researchers used QCA nanotechnology in their study [37] to suggest a novel way of designing effective multi-bit binary comparators. The method described in this paper enabled cutting-edge rivals to perform better in terms of average energy usage and computing complexity. For instance, the *32-bit* comparator was constructed and saved the occupied area, used cells, and energy consumption compared to its direct counterparts.

Also, researchers proposed a five-input majority gate design for a QCA comparator [38]. QCADesigner simulated the suggested comparator, and the simulation demonstrated that the suggested comparator's logic function was valid. The suggested comparator had the low latency when compared to earlier comparator designs. The circuit was constructed as a QCA comparator with *100* cells and an area of *0.*11 μm².

In [39], an effective coplanar *1-bit* comparator circuit was shown and assessed using QCA technology. The carefully designed majority, *XNOR*, and inverter gates formed the foundation of the coplanar *1-bit* QCA comparator circuit. Using QCADesigner *2.0.3*, the operation of the coplanar *1-bit* QCA comparator circuit was confirmed. The results showed that *38* cells and *0.03* μm² *of area* were needed for the *1-bit* QCA comparator circuit. It also had a delay of *0.5 clock cycles*. In terms of effective area, cell count, delay, and cost,
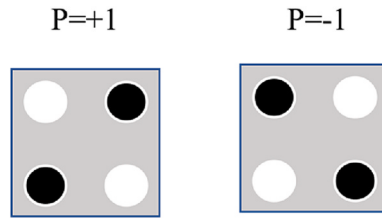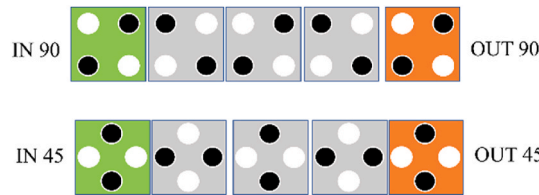
P=+1      P=-1

**Fig. 1.** QCA cells.

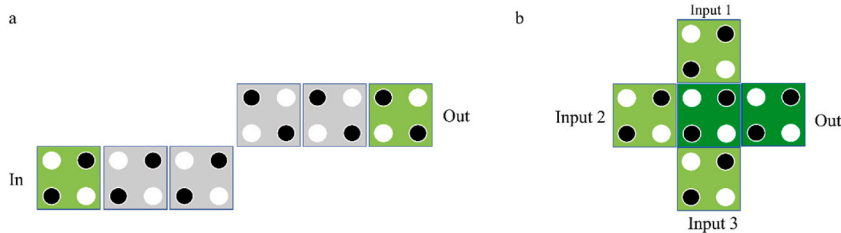**Fig. 2.** *90-degree and 45-degree* wires.

**Fig. 3.** (a) QCA presentation of inverter gate, (b) QCA presentation of inverter majority gate.

the comparison showed that the developed QCA comparator circuit performed better than other QCA comparator circuits.

Also, in Ref. [40], researchers proposed three unique *XNOR* gate architectures in the QCA technology. The structures that were being presented relied on the built-in capabilities of the new technology rather than adhering to traditional methods for designing logic gates. The suggested structures had served as the fundamental components of a comparator with one bit. For verification purposes, the generated circuits had been simulated, and their results had been compared with those of their existing equivalents in the literature.

*1-bit, 4-bit, and 8-bit* comparators were designed using QCA [41]. The circuits were simulated using QCADesigner. The findings demonstrated that the suggested comparators had the right logic function. According to the analysis, the suggested circuits' delay had not grown linearly with bit size. The suggested circuit, therefore, had good delay properties.

Finally, the logic design of a *1-bit* comparator based on the QCA wasprovided [42]. A comparator was the fundamental forming element in the digital logic outline that performed the similarity of two numbers. An evaluation and comparison of the proposed circuit's power consumption showed that the QCA design had lower power consumption than standard designs. The suggested comparator used 52 % less energy and took up *57.2 % less space*.

## 3. Proposed design

Recently, nano-technologies have gotten much attention in many fields [43,44]. In QCA, each nano-cell is distinguished by placing four quantum dots at each square's four corners. This unique structure is intended to use Coulombic repulsion, guaranteeing that electrons are deliberately positioned diagonally apart, increasing the distance between them. It is critical for the appropriate operation of the QCA cell, allowing for effective modulation of electron polarization and, as a result, enabling the necessary QCA processes [45]. The cell's polarization state is determined by the placements of the dots containing extra electrons. *P = -1 and P = +1*, as shown in Fig. 1, encode binary *0* and binary *1*.

Also, Fig. 2 depicts the QCA wire [27,46]. The QCA wire is a critical component for data transmission within nano-scale circuitry. Unlike traditional wires in classical computing, QCA wires transmit data using the principles of quantum-dot interactions. A wire in QCA technology typically comprises a series of QCA cells arranged in a specific configuration to allow for efficient signal propagation. Fig. 2 visually represents the QCA wire's layout and structure. QCA wires' unique properties contribute to their versatility in applications, such as interconnecting various components in a QCA circuit, allowing for the seamless flow of quantum information. QCA wire design and layout are critical considerations in optimizing the performance of QCA-based circuits. A complementary polarization
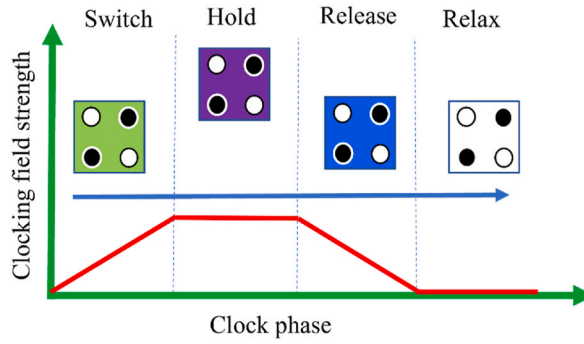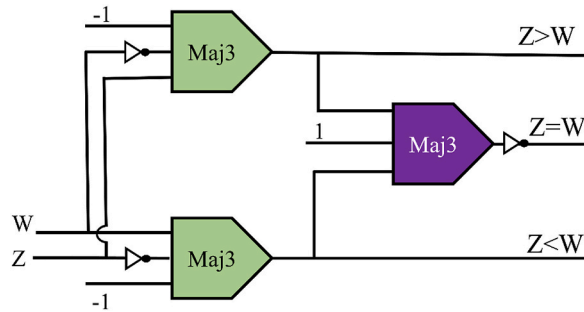
**Fig. 4.** Clocking in QCA technology in four phases.



**Fig. 5.** Logic diagram of the comparator in QCA.

**Table 1**
The comparator architecture truth table.

| Inputs | | Outputs | | |
|---|---|---|---|---|
| *Z* | *W* | *Z > W* | *Z=W* | *Z < W* |
| *0* | *0* | *0* | *1* | *0* |
| *0* | *1* | *0* | *0* | *1* |
| *1* | *0* | *1* | *0* | *0* |
| *1* | *1* | *0* | *1* | *0* |

effect occurs when a QCA cell is positioned diagonally to another cell. This phenomenon is the foundation for QCA inverters, as shown in Fig. 3 (a), where this understanding is used to achieve inversion. Implementing the Majority gate in QCA is based on the electrostatic interaction qualities of neighboring cells, as shown in Fig. 3 (b). The driver cell transmits information, which is reflected in the polarization state of the output cell. The effective energy generated by Coulombic interactions with neighboring cells within the radius of influence is critical in determining the polarization state of a cell.

Additionally, in the context of QCA clocking, a specialized mechanism enables signal propagation synchronization and control inside the QCA circuit. Clocking is accomplished by precisely timing input signals and activating specific cells, allowing for the sequential advancement of computing tasks [47]. This synchronized timing is critical for QCA circuits to operate reliably and efficiently, providing a structured framework for data processing and guaranteeing that the appropriate logical processes occur coordinated, as shown in Fig. 4.

A comparator is an electrical device that compares 2 binary integers and decides whether one is larger than, less than, or equal to the other. Comparators are generally utilized in *CPUs*, so nanotechnology has focused on researching and optimizing them. Fig. 5 depicts the block diagram of a single-bit comparator. *Z and W* are two signals that the circuit receives. One of the majority gates outputs is high when $Z < W$ (*logic 1*). The other majority gate provides a "greater output" when $Z > W$. The third majority gate output is only high if both signals are high ($Z = W$). The comparator circuit's truth table is shown in Table 1. Fig. 6 depicts the proposed comparator layout in QCA [48,49]. The suggested design uses *35* QCA cells and takes up *0.*04 µm$^2$ layout space. The circuit comprises three layers of *90-degree* QCA cells, with no requirement for a coplanar crossover and convenient access to the circuit's inputs and outputs. This comparator really consists of three three-input majority gates. The output can be attained after three clock phases in this architecture. Based on the QCA, the clocking zone has been utilized to identify computational pipelining and regulate the direction of signal flow [50,51].
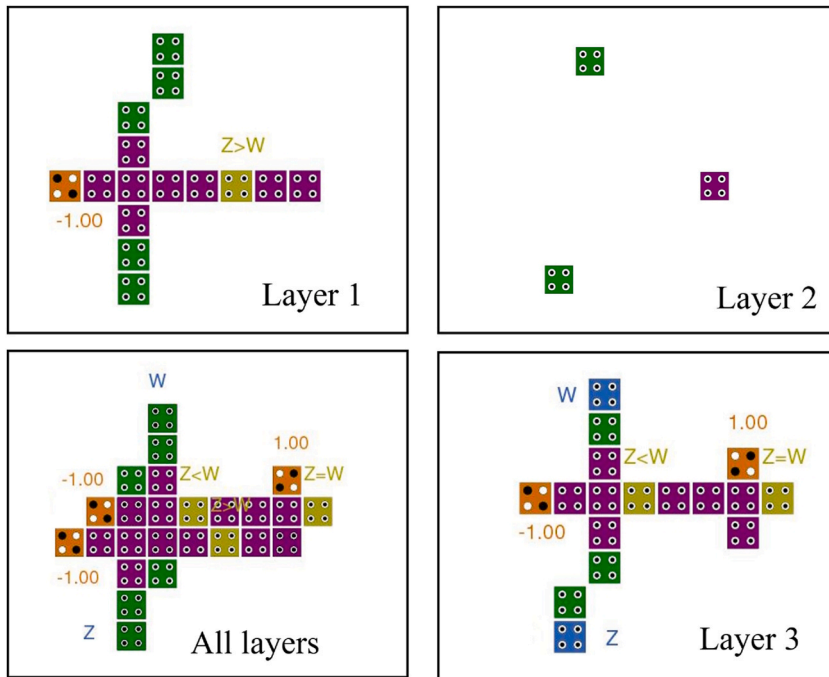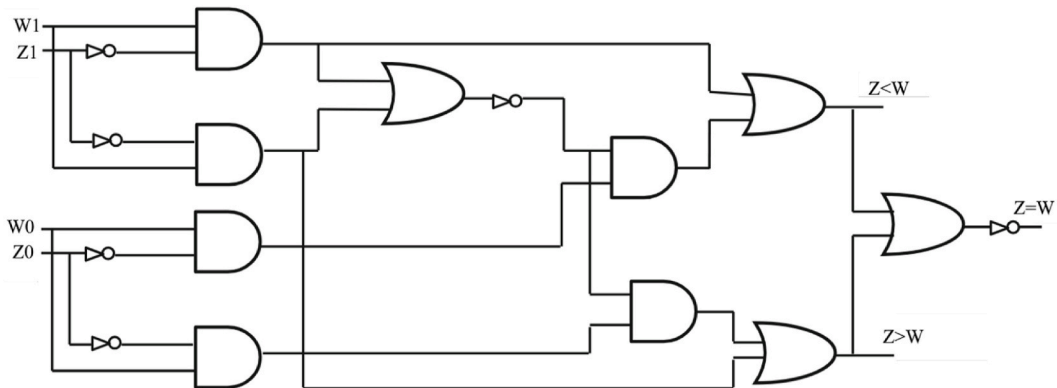
**Fig. 6.** The proposed comparator layout in QCA.



**Fig. 7.** Logic diagram of the *2-bit* comparator in QCA.

It is simple to expand the proposed *1-bit* comparator to an n-bit comparator. Two *2-bit* numbers are compared to each other in a 2-bit comparator. Fig. 7 shows the schematic depiction of a *2-bit* comparator utilizing logic gates. The six *AND* gates, four *OR* gates, and six inverters make up the suggested 2-bit comparator. Two bits of *W* and two bits of *Z* will be compared in accordance with Fig. 8. Fig. 8 shows the QCA realization of the proposed *2-bit* comparator with two *2-bit* numbers, $W=W1 \times W0$ and $Z=Z1 \times Z0$. Three layers are required, and it is designed using a multi-layer technique based on various clock zones. Only normal cells and fixed polarization cells are employed in this arrangement. This design, as can be seen, consists of *173 cells* totaling $0.19 \ \mu m^2$. The *1.25 clock cycle* delay between inputs and how they affect the outputs should be noted. The *2-bit* comparator circuit's truth table is shown in Table 2.

## 4. Comparison and discussion

In this section, we show the simulation results of the suggested designs, juxtapose them with earlier studies, and examine the suggested circuits' costs.

### 4.1. Simulation tools and results

Researchers at the University of Calgary/University of Bremen produced *QCADesigner-E*. This product's most often used version is
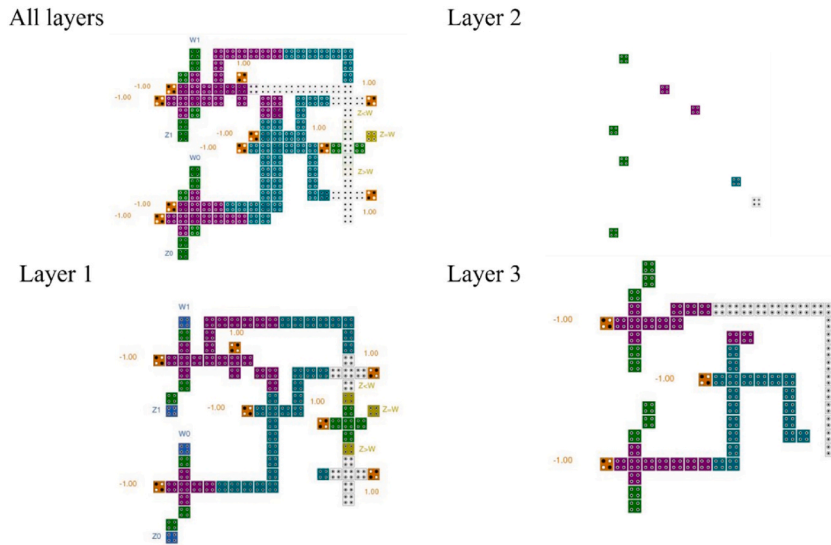
**Fig. 8.** The proposed *2-bit* comparator layout in QCA.

**Table 2**
The *2-bit* comparator architecture truth table.

| Inputs | | | | Outputs | | |
|---|---|---|---|---|---|---|
| Z1 | Z0 | W1 | W0 | Z > W | Z=W | Z < W |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

*2.2.* All of the parameters in the *QCADesigner-E* simulation engines *("Bistable Approximation" and "Coherence Vector")* are considered as default [52].

The parameters used for a simulation are as follows:
*Cell size:* 18 nm × 18 nm,
*Temperature = 1 K*.
*Dot diameter = 5 nm*.
*The number of samples: 220,000*.
*Clock high: 9.8e−22*.
*The radius of effect*: 41 nm
*Clock low: 3.8e−22*
*Lower threshold: −0.5*.
*Upper threshold: 0.5*.

Fig. 9 shows the examined input waveforms, which are *Z and W* for *2-bit* comparator. *Z=W, Z > W, and Z < W* are the three outputs of the comparator circuit. In this design, the outputs *Z < W and Z>W* are generated after *0.25 clock phases*, whereas *Z=W* is produced after *0.75* clock phases. The suggested comparator considered all of the inputs and produced accurate results. Only *35* QCA normal cells are employed in this circuit. Table 3 compares QCA-based comparator designs regarding cell number, area, access to inputs and outputs, and clock phases. *173* cells totaling *0.19* μm$^2$ are employed for *the 2-bit* design. The first output in this circuit is produced after
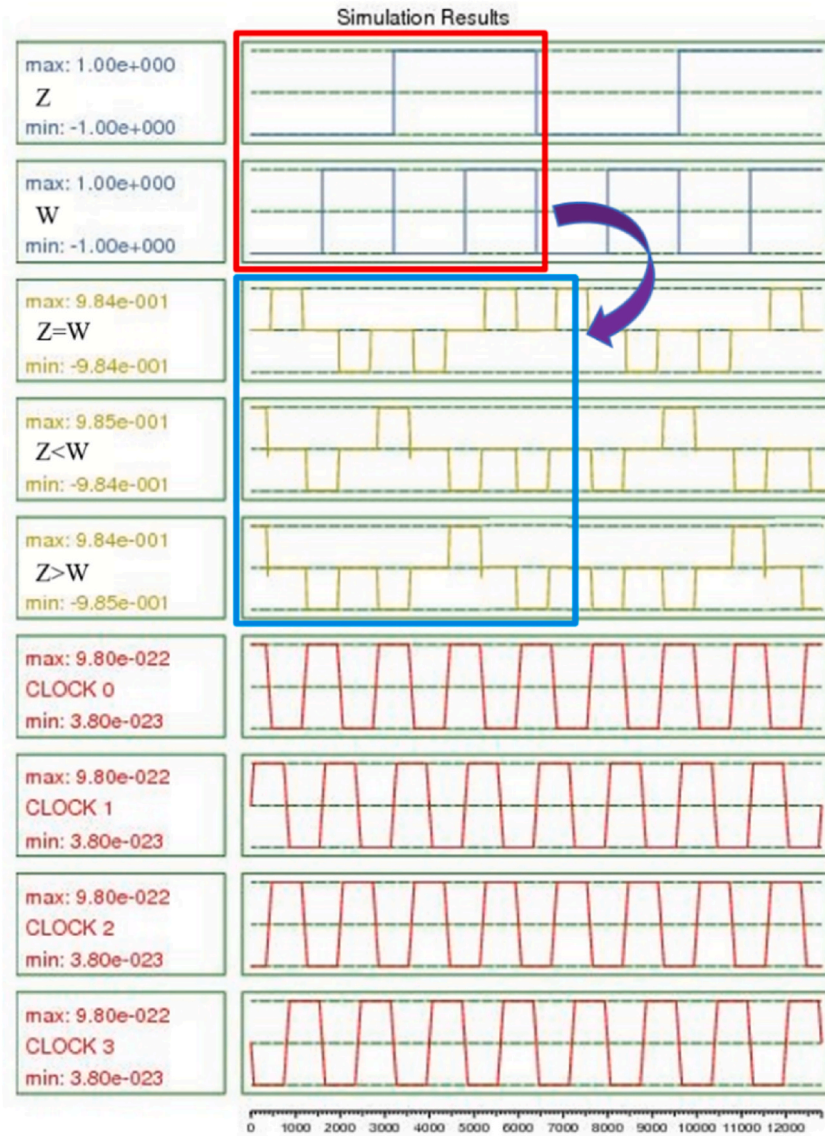
**Fig. 9.** Simulation result of proposed comparator circuit in QCA technology.

**Table 3**
Comparison of QCA-based comparator designs.

| Designs | Area ($\mu m^2$) | Cells | Latency | Cost (Area $\times$ latancy$^2$) | Easy access to inputs and outputs |
|---|---|---|---|---|---|
| *1-bit design* [35] | *0.06* | *81* | *0.75* | *0.033750* | *No* |
| *1-bit design* [36] | *0.05* | *42* | *0.75* | *0.028125* | *No* |
| *1-bit design* [37] | *0.028* | *37* | *1.00* | *0.028000* | *No* |
| *1-bit design* [38] | *0.11* | *100* | *0.75* | *0.061875* | *Yes* |
| *1-bit design* [39] | *0.03* | *38* | *0.5* | *0.007500* | *No* |
| *1-bit design* [40] | *0.05* | *40* | *0.75* | *0.028125* | *No* |
| *1-bit design* [41] | *0.14* | *97* | *1.00* | *0.140000* | *Yes* |
| *1-bit design* [42] | *0.06* | *85* | *1.25* | *0.093750* | *No* |
| *1-bit design* [54] | *0.07* | *79* | *1.00* | *0.070000* | *No* |
| *1-bit design* [33] | *0.06* | *73* | *1.00* | *0.060000* | *No* |
| *1-bit design* [14] | *0.04* | *54* | *1.00* | *0.040000* | *No* |
| *1-bit design* [55] | *0.08* | *43* | *1.25* | *0.125000* | *No* |
| *Proposed 1-bit design* | *0.04* | *35* | *0.75* | *0.022500* | *Yes* |
| *2-bit design* [56] | *0.38* | *203* | *1.25* | *0.593750* | *No* |
| *Proposed 2-bit design* | *0.19* | *173* | *1.25* | *0.296875* | *Yes* |

**Table 4**
Energy dissipation and comparison of the best QCA-based comparator designs.

| Design | Average energy dissipation | Total energy dissipation |
|---|---|---|
| *Proposed circuit* | *2.56e*-002 eV | *2.33e*-003 eV |
| *Gao*, et al. [34] | *2.80e*-002 eV | *2.75e*-003 eV |
| *Bahrepour* [55] | *2.97e*-002 eV | *3.05e*-003 eV |
| *Ajitha*, et al. [35] | *2.98e*-002 eV | *3.45e*-003 eV |
| *Deng*, et al. [36] | *3.10e*-002 eV | *3.79e*-003 eV |
| *Jun-wen and Yin-shui* [38] | *2.87e*-002 eV | *3.25e*-003 eV |
| *Shiri*, et al. [39] | *2.94e*-002 eV | *3.03e*-003 eV |
| *Majeed*, et al. [40] | *2.82e*-002 eV | *3.15e*-003 eV |
| *Xia and Qiu* [41] | *3.27e*-002 eV | *3.75e*-003 eV |
| *Erniyazov and Jeon* [42] | *2.96e*-002 eV | *2.93e*-003 eV |
| *Hayati and Rezaei* [54] | *3.07e*-002 eV | *3.97e*-003 eV |
| *Ghosh*, et al. [33] | *3.09e*-002 eV | *3.55e*-003 eV |
| *Roohi*, et al. [14] | *2.76e*-002 eV | *3.04e*-003 eV |
| *Roy*, et al. [37] | *3.01e*-002 eV | *3.203e*-003 eV |

a *1.25* clock phase delay. Additionally, the costs of the suggested architecture and the current models were contrasted in Table 3. The following formula is used to calculate the cost value [53]:

$$Cost = Area \times Latancy^2 \tag{1}$$

Compared to current schemes, the new design conducts calculations with the least amount of circuit complexity, the fewest number of cells, the lowest cost, and easy access to inputs and outputs. This is where the design stands apart from the competition.

Three-layer crossover techniques are used to construct the three-layered comparator circuits. Researchers use the *QCADesigner-E* tool to model circuits and compute energy dissipation for various crossings. Consequently, the *QCADesigner-E* tool determines the comparator circuit's energy dissipation. Table 4 shows the average and total energy dissipation of the recommended comparator circuit, which is constructed using conventional gates and cells, and its energy dissipation is shown as *2.56e-002 (eV)* and the QCA-based comparator designs.

## 5. Conclusion and future works

QCA technology is a promising technique for implementing digital circuits on a nano-scale. In digital circuits, comparator circuits play a significant function. Therefore, two efficient QCA comparator circuits were devised and analyzed in this work. The intended *1-bit* and *2-bit* comparators were built using the modified majority and inverter gates. The suggested circuits were compared to existing comparator circuits. Also, simulations of the suggested designs were performed utilizing *QCADesigner-E ("Bistable Approximation" and "Coherence Vector")* engines. In the *1-bit* circuit, just *35* QCA normal cells are used; in the *2-bit* design, *173* cells totaling *0.*19 μm² are used. This circuit's initial output is generated after a *1.25 clock phase* delay. The comparison findings showed that the suggested comparator circuits significantly improve the area, latency, and power consumption. The findings demonstrate the suggested design's correctness, and these structures might be helpful components in constructing bigger QCA circuits.

In future works, it is possible to design the circuit with higher bit numbers, such as *4-bit, 8-bit, or even higher*. It is also possible to increase the speed of the circuit and reduce the cost of implementation, study the design of circuits with fault tolerance, and combine this method with the method of the article. By examining and addressing the mentioned issues, new opportunities can be created for the design of nanocircuits.

**Data availability statement**

All data are reported in the paper.

**CRediT authorship contribution statement**

**Mehdi Darbandi:** Writing – original draft, Software, Resources, Data curation. **Saeid Seyedi:** Writing – review & editing, Writing – original draft, Supervision, Funding acquisition, Data curation. **Hamza Mohammed Ridha Al-Khafaji:** Writing – review & editing, Writing – original draft, Software, Formal analysis.

**Declaration of competing interest**

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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