

Received: 23 August 2017 Accepted: 9 October 2017

Published online: 27 October 2017

OPEN A Hybrid Gate Dielectrics of Ion Gel with Ultra-Thin Passivation Layer for High-Performance Transistors **Based on Two-Dimensional** Semiconductor Channels

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We propose a hybrid gate structure for ion gel dielectrics using an ultra-thin Al₂O₃ passivation layer for realizing high-performance devices based on electric-double-layer capacitors. Electric-double-layer transistors can be applied to practical devices with flexibility and transparency as well as research on the fundamental physical properties of channel materials; however, they suffer from inherent unwanted leakage currents between electrodes, especially for channel materials with low off-currents. Therefore, the Al₂O₃ passivation layer was introduced between the metal electrodes and ion gel film as a leakage current barrier; this simple approach effectively reduced the leakage current without capacitance degradation. In addition, we confirmed that a monolayer MoS₂ transistor fabricated with the proposed hybrid gate dielectric exhibited remarkably enhanced device properties compared to a transistor using a normal ion gel gate dielectric. Our findings on a simple method to improve the leakage current properties of ion gels could be applied extensively to realize high-performance electric-double-layer transistors utilizing various channel materials.

Ionic liquids provide the advantage of very large capacitances by the formation of nanogap capacitors at solidliquid interfaces^{1,2}, and electric double-layer-transistors (EDLTs) using ionic liquids have received significant attention because they show ultra-high capacitance and potential applicability in both practical flexible and transparent devices and studies on the fundamental physical properties of channel materials, including carrier transport phenomena, superconductivity, and thermoelectricity³⁻¹³. Despite this broad applicability, ionic liquids are limited in application to practical devices because of fluidity-related instability; however, this problem can be solved by introducing an ion gel, comprising a mixture of an ionic liquid and a polymer network, which maintains both the mechanical flexibility of the polymer and the large specific capacitance of the ionic liquid 14-19. As demonstrated by printable and photo-patternable ion gels, large-area device integration and the realization of practical applications of stretchable and flexible devices have become possible^{20,21}.

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Figure 1. (a) Molecular structures of the triblock copolymer (PS-PMMA-PS) and ionic liquid ([EMIM] [TFSI]) used for preparation of ion-gel film. (b) Schematic and (c) optical micrograph of the two-terminal device for characterization of electrical properties of hybrid dielectrics. (d) Current–voltage characteristics of hybrid dielectrics with various Al_2O_3 layer thicknesses. Inset: log-scale plot. (e) The variation of current density measured at 1 V as a function of Al_2O_3 layer thickness.

Meanwhile, in recent years, thin-film transistors (TFT) based on two-dimensional (2D) materials, such as hexagonal metal dichalcogenides, have been extensively studied for their potential applicability in emerging electronic and optoelectronic devices^{22–25}. 2D material-based TFTs using ion gels as gate dielectrics have been reported to exhibit superior electrical properties, such as low threshold voltages, high carrier mobilities, transparency, and flexibility²⁶⁻²⁹. Braga et al. realized ambipolar transistors fabricated using exfoliated WS₂ flakes with ionic liquid and proposed a method to determine the bandgap size directly³⁰; Zhang et al. demonstrated the formation and detection of field-induced p-n junctions in MoS₂ EDLTs³¹. Thus, ion gels as gate dielectrics for 2D material-based devices have several advantages, but their practicality must be improved to realize high-performance devices. Electric double-layer dielectrics, including ion gels, exhibit high leakage current levels between the gate and source/drain electrodes compared to those in inorganic-based gate dielectric³². For channel materials with greater gate leakage currents than intrinsic off-current levels leakage not only degrades the on/ off characteristics of the devices but also increases the threshold voltage. For example, the off-current level of previously reported monolayer MoS₂ transistors was in the range of 10^{-10} – 10^{-12} A^{33–36}, which is less than the gate leakage current level of several nano-amperes at the operating voltage in ion-gel-gated devices^{32,37}. Most reported ion-gel-gated transistors with 2D materials exhibit off-current levels exceeding the nano-ampere range, which might be greater than the intrinsic properties of the channel materials; in such cases, the transfer curves are expressed on linear rather than logarithmic scales. Therefore, it is important to reduce the leakage current through ion-gel dielectrics between the gate and source/drain electrodes to achieve higher-performance devices, particularly for channel materials with low off-current levels.

In this study, we propose a hybrid gate dielectric structure composed of an ion-gel film and ultra-thin Al_2O_3 passivation layer deposited by atomic layer deposition (ALD) to improve the electrical properties of the ion-gel-based 2D transistor, because Al_2O_3 films exhibit good leakage current properties and the ultra-thin Al_2O_3 layer can act as a leakage current barrier without causing significant capacitance drops^{38–40}. Moreover, it is known that the ultra-thin Al_2O_3 films formed by ALD exhibit flexibility and transparency^{35,41}, and therefore the hybrid dielectric structure could be suitable for application to flexible and transparent devices. To optimize the structure of the hybrid dielectrics, the variations in the electrical properties of the Al_2O_3 layer-modified ion gel film were systemically investigated as a function of the thickness of the Al_2O_3 passivation layer. Finally, the optimized dielectric structure was applied to a monolayer MoS_2 transistor and compared to a transistor using a normal ion-gel gate dielectric to confirm the effect of the proposed hybrid dielectrics on the transistor performance.

Results and Discussion

The ion gel films were prepared from a solution of the triblock copolymer poly(styrene-block-methyl methacrylate-block-styrene) (PS-PMMA-PS) and the ionic liquid 1-ethyl-3-methylimi dazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]), in ethyl propionate as an organic solvent. The PS-PMMA-PS and [EMIM][TFSI], with molecular structures as shown in Fig. 1a, are commonly used base materials to fabricate ion gels for EDLTs^{28,29}. First, we fabricated simple two-terminal devices, as shown in Fig. 1b,c, to investigate the effect of Al₂O₃ passivation on the electrical properties of the ion-gel films. The ultra-thin Al₂O₃ layers were deposited by thermal ALD using H₂O as an oxidant at the temperature of 350 °C. The reasons for determining the deposition conditions of ALD-Al₂O₃ will be discussed later. Figure 1d shows the current (I)-voltage (V) characteristics of the two-terminal devices according to the thicknesses of the inserted Al₂O₃ layers between the metal electrodes and ion gels. With the insertion of the Al₂O₃ passivation layer, the leakage current is remarkably decreased. When the dielectric film comprises only the ion gel without a passivation layer, the current level at 1 V is $\sim 10^{-9}$ A, indicating difficulty in accurately measuring the on/off characteristics for EDLTs devices with off-current levels below the nano-ampere scale. As shown in Fig. 1e and the inset of Fig. 1d, the current levels through the hybrid dielectric films exponentially decrease as the Al₂O₃ thickness is increased to 10 nm. This confirms that the leakage current can be effectively reduced by more than two and three orders of magnitude by inserting Al₂O₃ layers of only 3 and 5 nm in thickness, respectively.

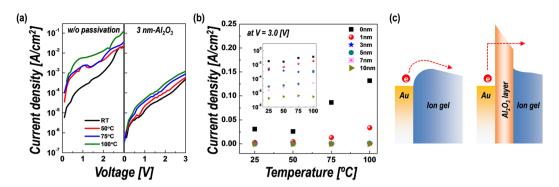


Figure 2. (a) J-V characteristics of ion gel film without passivation and with 3-nm-thick Al_2O_3 passivation layer, measured from room temperature to 100 °C. (b) Temperature-dependent current density of hybrid structure with various thicknesses of Al_2O_3 passivation layer, measured at 3 V bias. Inset: log-scale plot. (c) Schematics of current mechanism at metal—ion gel and metal— Al_2O_3 —ion gel interfaces.

Furthermore, we investigated the temperature dependence of the leakage current through the hybrid ion-gel films to study the change of current mechanism caused by the insertion of the Al₂O₃ layer. Figure 2a shows the current density (J)-voltage (V) characteristics of the ion gel-based dielectric films without and with a 3-nm-thick Al₂O₃ passivation layer measured at the temperature range of room temperature to 100 °C. With the insertion of the ultra-thin Al₂O₃ layer, not only the overall leakage current level decreases, but also the temperature dependency of the current is decreased (data for samples with different passivation thicknesses is shown in Fig. S2 of the Supplementary Information). As indicated in Fig. 2b, the temperature dependency of the leakage current tends to decrease with increasing thickness of the Al₂O₃ passivation layer. Based on these observations, the current mechanism and the cause of the decrease in the leakage current by Al₂O₃ passivation can be explained as follows: In the absence of a passivation layer, the leakage current flows mainly by a thermionic mechanism, in which electrons flow over a specific barrier height between the metal electrode and the ion-gel dielectrics. However, the thin but large-bandgap (~8.9 eV) Al₂O₃ passivation layer located between the metal electrode and the ion gel acts as a leakage current barrier, preventing the flow of a direct thermionic current. Therefore, as the thickness of the passivation layer increases, the main current mechanism through the metal electrode to the ion gel-based dielectrics changes to electric field-induced tunneling, which is relatively insensitive to temperature, as indicated in the schematics in Fig. 2c. The results confirm that the leakage current characteristics are effectively improved by reducing the thermionic current in the dielectric structure with the placement of a large-bandgap Al₂O₃ passivation layer.

Meanwhile, although the leakage current characteristics of the device using a hybrid dielectric structure of ion gel with an Al₂O₃ passivation layer can be improved, the dielectric constant of Al₂O₃ is relatively low (~9), which can degrade the dielectric properties of the device. Therefore, we investigated the dielectric properties of ion gel-based hybrid dielectrics as a function of the thickness of the inserted Al₂O₃ layer. The capacitance density of the ion gel without passivation layer was $\sim 10.8 \,\mu\text{F/cm}^{-2}$, which is comparable to those of previously reported gels $(\sim 5-10 \,\mu\text{F/cm}^{-2})^{\frac{4}{3},29,37}$. The capacitance slightly increased by the insertion of an Al₂O₃ layer with the thickness of ~3 nm and then continuously decreased with further increases in the inserted Al₂O₃ thickness. The decrease in capacitance for relatively thick (>5 nm) Al₂O₃ layers can be explained by the relatively small dielectric constant of Al₂O₃ films, but it is difficult to understand the increase in capacitance for 3-nm-thick Al₂O₃-inserted ion-gel films. However, it was previously reported that self-discharge at the charged state in electric double-layer capacitors, caused by high leakage currents, could cause capacitance drops 42,43. Therefore, the increase in capacitance for the sample with the 3-nm-thick Al₂O₃ layer was attributed to the decrease in leakage current by the insertion of the leakage current barrier. It is also observed that the frequency dependence of the capacitance tends to decrease with increases in the thickness of the Al₂O₃ passivation layer (see inset of Fig. 3). The most important point is that, although the low-dielectric-constant layer is inserted, the capacitance is not degraded until the Al₂O₃ thickness is increased to ~5 nm. Therefore, it can be expected that the hybrid gate structure of ion-gel dielectrics with ultra-thin Al₂O₃ passivation layers could effectively improve the transistor characteristics of EDLTs by reducing the gate leakage current without inducing capacitance drops.

Finally, the hybrid gate dielectric of ion-gel film with an ultra-thin Al₂O₃ passivation layer was applied to MoS₂ EDLTs to confirm the effect of the proposed gate structure on the performance of the MoS₂ transistors. Figure 4a,b show the schematic and optical micrograph of the fabricated MoS₂ EDLT structure using the hybrid gate dielectric, respectively. Monolayer MoS₂ crystals directly grown on a SiO₂/Si substrate by chemical vapor deposition (CVD) were used as a transistor channel; source/drain and side gate electrodes were defined by the lift-off method. After formation of electrodes, 3-nm-thick Al₂O₃ layers were deposited by thermal ALD at 350 °C. ALD Al₂O₃ films are usually obtained using H₂O, O₃, or O₂ plasma as the oxidant at the temperature range of 50 to 400 °C. In our case, we used H₂O vapor as an oxidant to prevent damage to the MoS₂ channel by ozone or O₂ plasma. In addition, because ideal van der Waals 2D materials do not have dangling surface bonds, the precursor molecules for ALD growth were infrequently adsorbed on the 2D materials, so that thin film growth by ALD could be suppressed on the 2D materials. Therefore, the ALD-Al₂O₃ layer could be selectively deposited except on the 2D material surface without additional etching processes. However, the CVD-grown MoS₂ could contain defect sites where the precursor can chemosorb; therefore, the ALD process for depositing the Al₂O₃ passivation layer was conducted at the temperature of 350 °C to minimize the chemisorption of precursors on the MoS₂

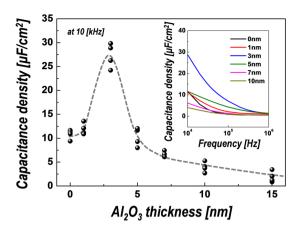


Figure 3. The variation of the capacitance density of two-terminal device with hybrid dielectrics depending on Al_2O_3 layer thickness with frequency of $10\,\mathrm{kHz}$. Inset: frequency dependence of the capacitance for different Al_2O_3 thickness.

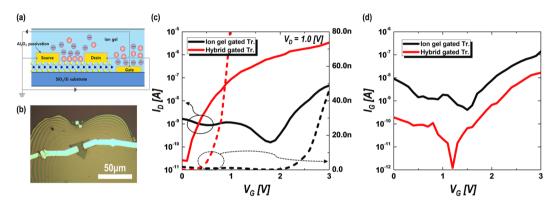


Figure 4. (a) Schematic and (b) optical micrograph of the hybrid-structure EDLTs fabricated using monolayer single-crystalline MoS_2 . (c) Transfer curve and (d) gate leakage current (absolute values) of the MoS_2 EDLTs without passivation (ion gel gated Tr.) and with 3-nm-thick Al_2O_3 passivation layer (Hybrid gated Tr.) measured at drain voltage of 1.0 V under room temperature. Solid line and dashed line in transfer graph indicate the logarithmic-scale (left-side axis) and linear-scale (right-side axis) value of drain current, respectively.

surface⁴⁴. After the deposition of the 3-nm-thick Al₂O₃ layer by ALD on the MoS₂ crystals, it was confirmed that the Al₂O₃ layer was rarely deposited on the surface of the MoS₂ crystals by atomic force microscopy analysis (see Fig. S3 of the Supplementary Information). In fact, since no degradation of capacitance was observed for inserted Al₂O₃ layer thicknesses below ~5 nm, it can be expected that even if the ultra-thin Al₂O₃ is partially deposited on MoS,, the transistor performance would not be negatively affected. The room-temperature transfer characteristics $(I_D - V_G)$ of the MoS₂ EDLTs measured at the source-drain voltage (V_D) of 1.0 V with and without Al₂O₃ passivation are indicated in Fig. 4c. For comparison, regardless of with and without passivation, the channel length and width were fixed at 10 and 10 µm, respectively. Whereas the on/off ratio of the ion gel-only gated transistor is $\sim 10^2$ because of the relatively high off-current level of $\sim 10^{-9}$ A, the on/off ratio of the hybrid-gated transistor is remarkably increased to $\sim 10^5$. Moreover, it is observed that the threshold voltage is decreased by more than 2 V, and the subthreshold swing (SS) is also improved by inserting the ultra-thin Al₂O₃ layer between the electrodes. These improvements in the electrical properties of the transistor by the Al₂O₃ passivation layer are mainly attributed to the reduction of the leakage current between the gate and source/drain electrodes. By applying the hybrid gate structure of ion-gel dielectrics with 3-nm-thick Al₂O₃ passivation layers, as shown in Fig. 4d, the gate leakage current is significantly decreased by about two orders of magnitude (from several nano-amperes to several tens of pico-amperes at $I_D = 1.0 \,\mathrm{V}$), which well corresponds with the off-current level of each transistor. In addition, the on-current level of the hybrid gated EDLTs was also greatly increased by Al₂O₃ passivation, which might be attributed to the reduced dielectric loss from the reduced gate leakage current.

Conclusions

In this study, we systematically investigated the effect of inserting an Al_2O_3 passivation layer between the ion-gel dielectric film and metal electrode on the electrical properties of a transistor to propose a hybrid ion gel-based gate structure with improved properties. As the thickness of the inserted Al_2O_3 layer was increased, the leakage current through the ion gel-based dielectrics was exponentially decreased (more than two orders of magnitude even with an ultra-thin Al_2O_3 layer of 3 nm in thickness). Moreover, no degradation of capacitance was observed for

inserted Al_2O_3 layer thicknesses below ~5 nm. The hybrid structured gate dielectric based on the ion-gel film with a 3-nm-thick Al_2O_3 layer was applied to a monolayer MoS_2 transistor. The performance of the transistor was compared to that of another transistor using a normal ion-gel gate dielectric. Most transistor properties, such as the on/off ratio, threshold voltage, and subthreshold swing, were improved by the remarkable decrease of the gate leakage current. The proposed hybrid-structured gate dielectrics could be applied to versatile devices, especially with transparency and flexibility, based on EDLTs using various channel materials, as well as 2D material-based transistors.

Methods

Preparation of ion gel. The ion gel was prepared from a solution of a triblock copolymer, poly(styrene-block-methyl methacrylate-block-styrene) (PS-PMMA-PS, Polymer Source Inc.), and an ionic liquid, 1-ethyl-3-methylimi dazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI], Merck), in ethyl propionate as the organic solvent^{28,29}. The polymer, ionic liquid, and solvent were mixed with the weight ratio of 0.5:9.5:20, and then the mixture was sonicated to obtain a homogeneous solution. This solution was drop-casted onto the metal electrodes of the device. Through annealing at 120 °C for 10 min, the solvent was evaporated and an ion gel film was formed through the physical association of the polymer blocks in the ionic liquid.

Deposition of ultra-thin Al_2O_3 layer. To enhance the electrical properties of the gate dielectric based on the ion gel, an ultra-thin Al $_2$ O $_3$ layer, deposited by ALD at 350 °C, was introduced between the metal electrode and ion-gel interface. Trimethylaluminum (TMA, Al(CH $_3$) $_3$) and water vapor (H $_2$ O) were used as precursor and oxidant, respectively; both canisters containing TMA and H $_2$ O were maintained at the temperature of 10 °C. The deposition process was performed under saturation conditions. One deposition cycle consisted of the exposure of TMA for 0.5 s, purging with N $_2$ for 5 s, exposure of H $_2$ O for 0.5 s, and purging with N $_2$ for 5 s.

Device fabrication and characterization. To investigate the effect of Al_2O_3 passivation on the electrical properties, a simple two-terminal device was fabricated on SiO_2/Si substrate. First, two electrodes were formed from 10-nm Ti/50-nm Au layers via a lift-off method using photolithography (Photo resist: AZ5214, AZ Electronic Materials) and e-beam evaporation. The hybrid gate dielectric was formed via the deposition of ultra-thin Al_2O_3 layers with thicknesses of 0–10 nm, followed by the drop-casting of the ion gel. Meanwhile, to apply the hybrid gate dielectric to field-effect transistor (FET) devices, MoS_2 transistors were fabricated using monolayer crystals synthesized by CVD (see Fig. S1 of the Supplementary Information for more details on the synthesis process). Similar to the above method, source/drain and side gate electrodes were formed from 10-nm Ti/50-nm Au layers by a lift-off method. In this case, however, electron-beam lithography using poly(methyl methacrylate) (PMMA) was used instead of photolithography, because the source/drain electrodes required greater accuracy in formation on the MoS_2 crystal. Finally, for comparison, two types of ion gel-based gate dielectrics were formed, one without passivation and the other with a 3-nm-thick Al_2O_3 passivation layer. After the device fabrication, capacitance–voltage (C-V), current–voltage (I-V), and FET transfer characteristics measurements were performed in a dark probe station using a semiconductor characterization system (Keithley, 4200-SCS).

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Acknowledgements

This work was supported by National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2016R1C1B2007336 and No. 2017R1A2B4004560). This work was also supported by New Technology Commercialization Support Program for Young Researchers (2016) funded by the Busan metropolitan city and Busan Institute of S&T Evaluation and Planning (BISTEP).

Author Contributions

S.-H.K. and J.-H.A. conceived the idea, designed the experiments. C.-M.H. prepared the CVD-grown MoS_2 sample. D.Y.K. and C.-M.K. deposited ultra-thin ALD Al_2O_3 layers. H.J., J.-H.C., S.-Y.S., M.-J.L. and J.-D.K. fabricated the ion gel devices and performed the electrical measurement. H.J., J.-H.C. and H.-S.M. analyzed the data under the supervision of J.-H.A. The manuscript was written by H.J., J.-H.C., C.-M. H. and J.-H.A. All the authors reviewed and commented on the manuscript.

Additional Information

Supplementary information accompanies this paper at https://doi.org/10.1038/s41598-017-14649-6.

Competing Interests: The authors declare that they have no competing interests.

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